Two-phase Clocking for Medium to Large RSFQ Circuits

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Abstractã In this article a novel two-phase clocking scheme applicable to RSFQ circuits of any complexity is introduced. We show that high performance, robustness, and design simplicity may justify two-phase clocking despite the area overhead inherent in this scheme.

I. INTRODUCTION

Complex RSFQ circuits operate at clock frequencies of tens of gigahertz in simulation. Maximum experimental frequencies have been considerably lower than simulated; this is largely due to variations in the fabrication process [1]. Two-phase clocking, a common approach in semiconductor circuit design, can be used to relax the timing constraints in the circuit, and thus increase circuit tolerance to parameter variations [2], [3].

An initial attempt to apply two-phase clocking to RSFQ circuits was reported in [4]. In this paper, two-phase clocking was used to drive a long linear shift register. The motivation was to assure that the circuit worked correctly at the very low clock frequency applied during functional testing, independent of the parameter variations in the circuit. No attempt was made to optimize the performance of the circuit. Two phases of the clock are generated using complementary DC/SFQ converters, and distributed independently along the data path of the shift register. As a result, the design is vulnerable to independent local parameter variations occurring in the two parallel clock paths used to distribute each phase of the clock.

In this article we present a novel *two-phase concurrent clocking* scheme applicable to RSFQ circuits of arbitrary complexity. The performance of this scheme is analyzed, and its advantages and disadvantages are compared to single-phase clocking schemes.

II. FEATURES OF THE SCHEME

In RSFQ two-phase clocking, two sequentially adjacent cells are driven using two different phases of the clock. The phases of the clock are shifted from each other by half of the clock period, as shown in Fig. 1 a. Both phases of the clock denoted as Φ_1 and Φ_2 can be generated from one signal with twice the clock frequency, Φ_{12}, using a T flip-flop working as a frequency divider, as shown in Fig. 1 b. A separate T flip-flop is associated with each clocked cell in the circuit as shown in Fig. 2. Signal Φ_{12} is distributed using a *single* clock path, while two phases of the clock are generated locally using T flip-flops associated with every cell in the circuit. If the first cell of a pair of adjacent cells is driven using first phase of the clock (output *out* of the T flip-flop), the second cell is driven using the second phase of the clock (output *out* of the T flip-flop), and vice versa.

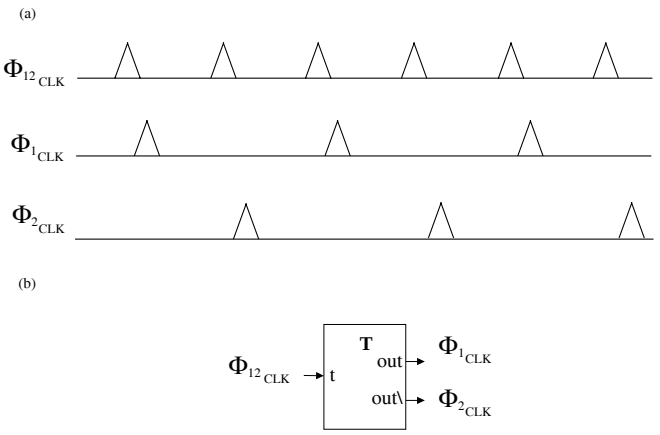

Fig. 1. Two-phase clocking in RSFQ logic. (a) phases of the clock; (b) method of generating both phases from a single signal operating at twice the clock frequency using a T flip-flop.

An important parameter describing the data path between two sequentially adjacent cells is the *clock skew*. In two-phase clocking, clock skew (denoted $skew_{ij}$) is defined as the difference between the arrival time of the signal Φ_{12} at the inputs of T flip-flops at the beginning and at the end of data path (t_{CLKi} and t_{CLKj}, respectively). The clock skew between cells *i* and *j* is

$$skew_{ij} = t_{CLKi} - t_{CLKj} . \quad (2)$$

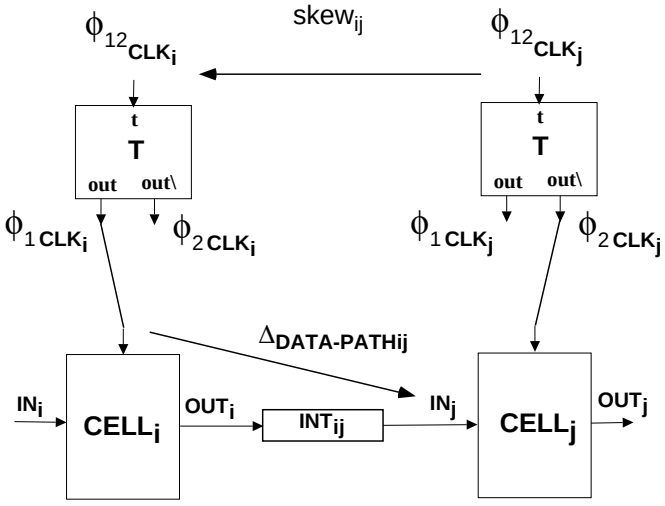

Fig. 2. Data path between two physically adjacent RSFQ cells in two-phase clocking. Notation: INT_{ij} - interconnection between cells i and j, $CELL_i$, $CELL_i$ - RSFQ cells i and j, T - T flip-flop.

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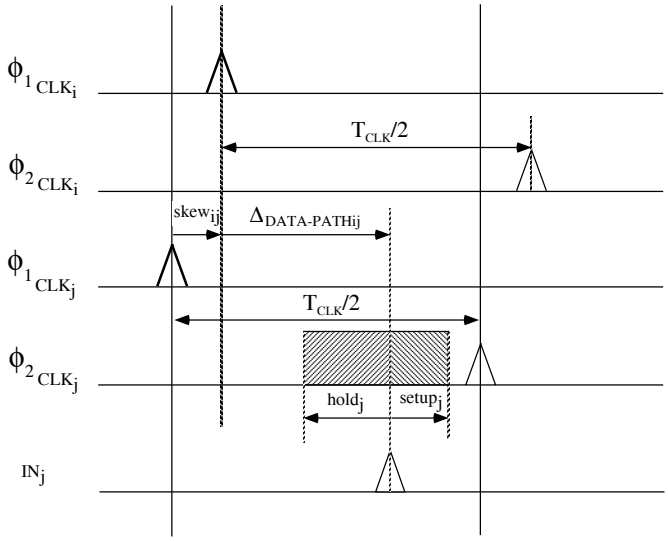

Fig. 3. Exchange of data between two physically adjacent cells in two-phase clocking.

Similarly, the *data path delay* (denoted $\Delta_{DATA\text{-}PATHij}$) is defined as the interval between the moment when the clock (phase Φ_1) arrives at the *clock* input of the first cell (t_{CLKi}), and the moment when the data appears at the *data* input of the second cell (t_{INj}):

$$\Delta_{DATA\text{-}PATHij} = t_{INj} - t_{CLKi} \ . \tag{2}$$

Timing diagrams depicting the exchange of data between two sequentially adjacent cells are given in Fig. 3. Conditions for the correct operation of the circuit are

$$T_{CLK}/2 \ \geq skew_{ij} + \Delta_{DATA\text{-}PATHij} + setup_j \ , \tag{3}$$

$$skew_{ij} \ + \Delta_{DATA\text{-}PATHij} + T_{CLK}/2 \ \geq hold_j \ . \tag{4}$$

$Hold_j$ and $setup_j$ denote the hold and setup time of the CELL j. The exact meaning of these timing parameters, as well as

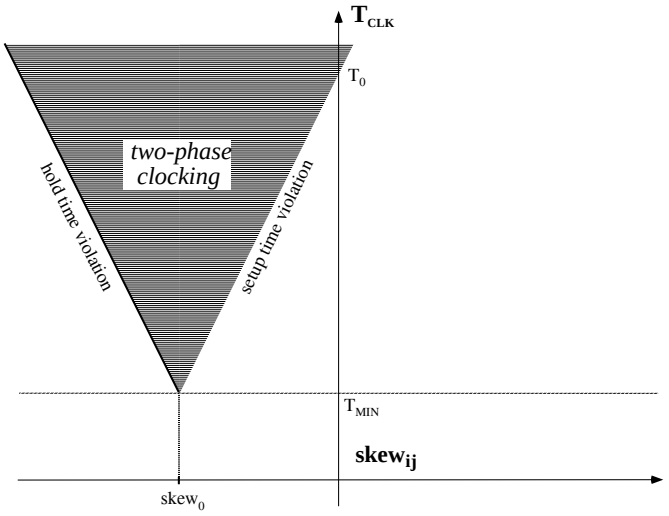

Fig. 4. Operating region for two phase clocking of a circuit composed of two sequentially adjacent cells, as a function of the clock period and the clock skew.

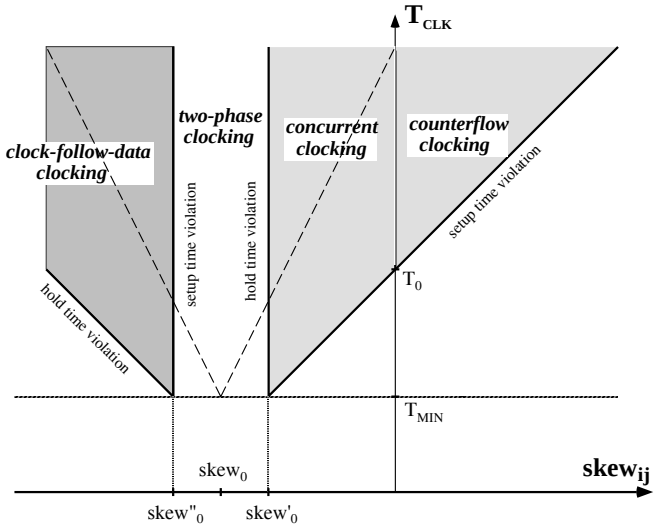

Fig. 5. Operating region for single-phase clocking of the data path between two sequentially adjacent cells as a function of the clock period and the clock skew.

other terminology used throughout this paper are defined in detail in [5].

In Fig. 4, the operating region of the circuit as a function of the clock skew and the clock period is shown. By comparing the shape of this operating region with the regions for single-phase clocking schemes [5] presented in Fig. 5, it can be concluded that for two-phase clocking:

a) There is no value of clock skew for which the circuit fails at low frequency. For any possible value of clock skew, the circuit works correctly at some minimum clock period and at all longer clock periods. In contrast, Fig. 5 shows that for single phase clocking there exists a region of the values of clock skew (from $skew''_0$ to $skew'_0$) where the circuit does not work for any (even extremely low) clock frequency.

b) The minimum clock period in the circuit is limited by

$$T_{MIN} = hold_j + setup_j \ , \tag{5}$$

and the optimal choice of the clock skew is

$$skew_0 \ = -\Delta_{DATA\text{-}PATHij} - setup_j /2 + hold_j/2 \ . \tag{6}$$

The optimum clock skew in two-phase clocking, $skew_0$, is related to the optimum clock skew for single-phase concurrent clocking, $skew'_0$, and single-phase clock-follow-data clocking, $skew''_0$, according to

$$skew_0 = \frac{skew'_0 + skew''_0}{2} \ . \tag{7}$$

The minimum clock period, without taking parameter variations into account, is identical for all three clocking schemes. The position of the data pulse within the clock period for the optimum value of the clock skew in two-phase clocking is shown in Fig. 6.

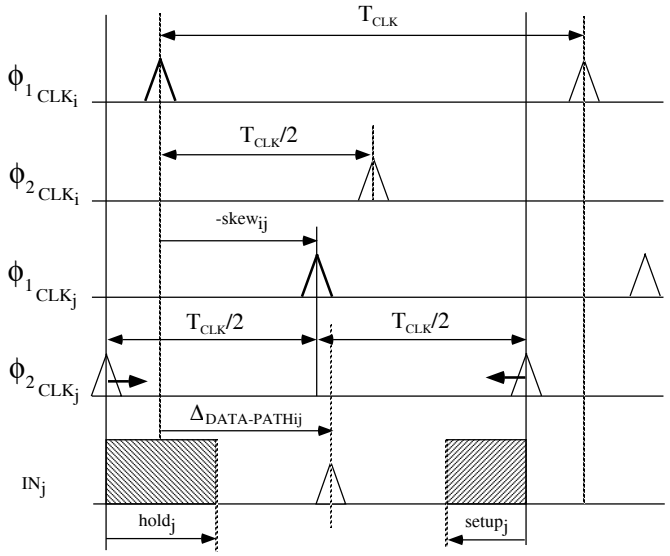

Fig. 6. The position of the data pulse within the clock period in two-phase clocking for the optimum value of the clock skew.

c) The optimal value of the clock skew is identical regardless of whether parameter variations are considered. In other words, the inaccuracies in the fabrication process will change the desired value of clock skew between any two sequentially cells. This change is equally likely to increase or decrease the desired value. Therefore, since the operating region in Fig. 4 is symmetric about $skew_0$, the optimal value to choose to design $skew_{ij}$ is equal to $skew_0$ regardless of the magnitude of those inaccuracies. This feature simplifies considerably the design of the circuit by eliminating the need for the computationally intensive Monte Carlo simulations necessary to determine the optimal clock skew in single-phase concurrent clocking.

d) The *expected* value of the minimum clock period is the same with or without taking parameter variations into account. As a result, the expected value is smaller than in single-phase concurrent clocking. The worst case value of the clock period in both schemes is comparable.

III. Summary

A novel two-phase clocking scheme applicable to RSFQ circuits of arbitrary complexity is proposed and analyzed. The advantages of two-phase synchronous clocking are high-performance, design procedure simplicity, and robustness. The expected value of maximum clock frequency, taking parameter variations into account, is greater than in any known single-phase clocking scheme. The design procedure is extremely simple, because the optimal value of the clock skew is identical regardless of whether parameter variations are considered or not. The scheme is very robust in that for any possible value of the clock skew, there exists a clock frequency below which the circuit works correctly. The only obvious disadvantage of two-phase clocking is the overhead of additional circuitry required to generate and distribute the second phase of the clock.

References

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