Interconnect Coupling Noise in CMOS VLSI Circuits

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Abstract— **Interconnect between a CMOS driver and receiver can be modeled as a lossy transmission line in high speed CMOS VLSI circuits as transition times become comparable to or less than the time of flight delay of the signal through the low resistivity interconnect. In this paper, closed form expressions for the coupling noise between adjacent interconnect are presented to estimate the coupling noise voltage on a quiet line. These expressions are based on an assumption that the interconnections are loosely coupled, where the effect of the coupling noise on the waveform of the active line is small and can be neglected. It is demonstrated that the output impedance of the CMOS driver should preferably be comparable to the interconnect impedance in order to reduce the propagation delay of the CMOS driver stage.**

I. Introduction

A trend in modern high speed, high density CMOS VLSI circuits is decreasing feature sizes as well as increasing chip dimensions. The delay of these highly scaled circuits is now dominated by the interconnect [1]. Furthermore, up to 30% of the dynamic power is consumed by the interconnect [2]. In addition to the interconnect delay and power consumption, coupling noise (or crosstalk) between adjacent interconnect lines is also a primary concern for present and future generations of CMOS VLSI circuits [3], [4], [5].

Coupling noise between adjacent interconnect can cause disastrous effects on the logical functionality and long-term reliability of a VLSI circuit [6]. Coupling effects have become more significant as the feature size is decreased to deep submicrometer dimensions because the spacing between conductor lines is decreased and the thickness of the high level conductor lines is increased in order to reduce the parasitic resistance of the conductors.

If the peak noise voltage at the receiver is greater than the threshold voltage, it may cause a circuit to malfunction. Furthermore, the induced noise voltage may cause extra power to be dissipated on the quiet line due to momentary glitches within the logic gates. Carrier injection or collection into the substrate may occur as the coupling noise voltage rises above the power supply voltage V_{dd} or falls below ground [7]. These deleterious effects caused by the coupling noise voltage become aggravated as the relaxation time, the time for the coupling noise to reach a steady state voltage, increases. The effect of the coupling noise is also important in dynamic CMOS circuits, which are more sensitive to noise than static CMOS circuits.

In the design of high speed VLSI circuits, it is therefore important to be able to predict coupling noise at the system (or chip) level [8]. This information permits circuit malfunctions or extra power consumption caused by the coupling noise to be avoided [9]. The design cycle and cost can therefore be reduced as well as the circuit reliability improved.

An analysis of coupling noise can be performed in both the frequency domain and the time domain, but most of these analyses result in numerical solutions [10], [11] or an equivalent circuit simulation [12]. A numerical solution is not convenient at the system (or chip) level to predict noise effects since it requires excessive simulation time and computer memory. The analytical analysis of coupled *lossless* transmission lines in the time domain has been addressed in [13]. A lossless model is not appropriate for interconnect in CMOS VLSI circuits since the parasitic interconnect resistance cannot be neglected.

An analysis of coupled interconnect in CMOS VLSI circuits is presented in this paper. For simplicity, the interconnect is modeled as a uniform transmission line [14] and the coupled interconnect lines are assumed to be in parallel. Although with interspersed contacts the interconnect lines are not uniform and coupled interconnect lines are not often parallel over long distances in practical VLSI layouts, a uniform transmission line is used to model the distributed interconnect impedance. Also, coupling effects are typically more pronounced in parallel structures than in crossover structures [15].

Analytical equations are derived from time domain differential equations using Laplace transforms and the assumption of a loosely coupled condition, in which the coupling capacitance and the mutual inductance are assumed to be less than 30% of the self-capacitance and the self-inductance, respectively. The accuracy of the predicted peak noise voltage based on these closed form expressions is within 20% for the driver end coupling noise voltage and 15% for the receiver end coupling noise voltage. The dependency of the propagation delay of the CMOS driver stage on the driver impedance and the relationship between the relaxation time of the coupling noise voltage and the driver impedance are also investigated. Note that the shortest propagation delay and relaxation time occur when the driver output impedance matches the interconnect impedance.

An analytical model of a CMOS driver and receiver structure, as well as closed form expressions of the coupling noise voltage at both ends of the quiet interconnect line are addressed in Section II. The predicted peak coupling noise voltage based on the analytical equations is compared with simulation in Section III. A discussion of

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the coupling noise voltage of lossy interconnect and the effect of the coupling noise on CMOS VLSI circuits, the driver output impedance, and the relaxation time of the coupling noise voltage are discussed in Section IV followed by some concluding remarks in Section V.

II. Noise Coupling Equations

Consider a typical CMOS driver and receiver structure in a high speed VLSI circuit, an example of which is schematically shown in Fig. 1a. $Inv1$ is the active driver and $Inv3$ is the quiet driver, and $Inv2$ and $Inv4$ are the receivers. The interconnect between the CMOS driver and receiver is modeled as a lossy transmission line. In order to analyze the coupling noise, the CMOS drivers are modeled as a linear resistor (R_1 and R_2) and the receivers are modeled as a capacitive load (C_{l1} and C_{l2}). The interconnect between the active driver Inv_1 and the receiver Inv_2 is the active line, and the interconnect between the quiet driver Inv_3 and the receiver Inv_4 is the quiet line.

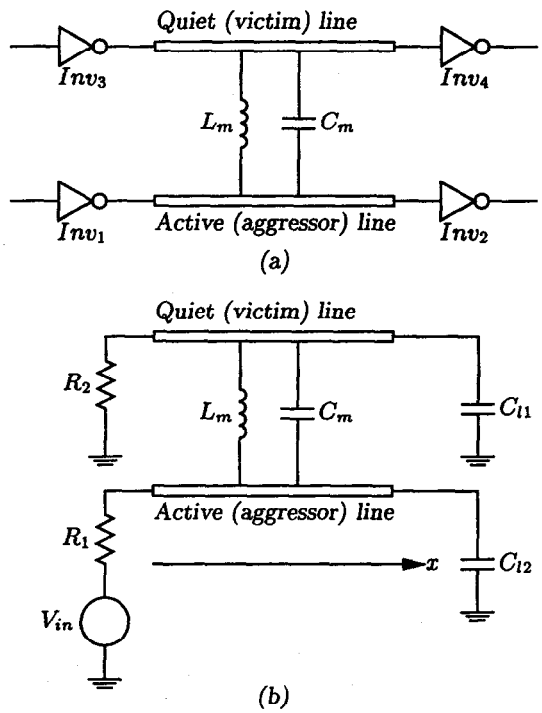

Fig. 1. An example of a CMOS driver and receiver structure. a) Two adjacent CMOS drivers and receivers. b) A simplified circuit model of the structure.

The equivalent circuit model is shown in Fig. 1b, where two coupled lossy transmission lines have similar impedance characteristics, *i.e.*, R, L, and C are the same for each line. Line 1 is the active (or aggressor) line and line 2 is the quiet (or victim) line.

Laplace transforms are used to solve the time domain differential equations characterizing this structure. The resulting formulation is

$$\frac{\partial^2}{\partial x^2}V_1(x,s) = A_1V_1(x,s) + B_1V_2(x,s), \tag{1}$$

$$\frac{\partial^2}{\partial x^2}V_2(x,s) = A_2V_1(x,s) + B_2V_2(x,s), \tag{2}$$

where

$$A_1 = B_2 = sRC + s^2LC - s^2L_mC_m, \tag{3}$$

$$B_1 = A_2 = s^2L_mC - s^2LC_m - sRC_m. \tag{4}$$

R, L, and C are the line resistance, inductance, and capacitance per unit length, respectively. L_m and C_m are the coupling inductance and capacitance per unit length between line 1 and line 2. The minus sign in (3) and (4) occurs since C_m is a positive value [11], [16]. $V_1(x,s)$ and $V_2(x,s)$ are the Laplace transform of the voltages between line 1 and line 2, respectively, and ground.

In order to simplify this analysis, a condition that the interconnect lines are loosely coupled is assumed, implying that L_m and C_m are small as compared to L and C such that the third term in (3) can be neglected. To quantify this assumption,

$$\frac{L_m}{L}\frac{C_m}{C} < 0.1. \tag{5}$$

The error of neglecting the last term in (3) is less than 5% with this assumption. Only first order effects are considered, where the voltage on line 1 affects the voltage on line 2 and $V_2(x,s)$ is too small to have an effect on line 1. This situation occurs because the voltage on line 2 is coupled from the voltage on line 1. This assumption requires that those terms in (4) containing L_m and C_m are small, *i.e.*, both L_m/L and C_m/C are small. Combining with (3), the loosely coupled condition can be restated as

$$L_m/L < 0.33 \quad \textit{and} \quad C_m/C < 0.33. \tag{6}$$

Based on this loosely coupled assumption, (1) and (2) are simplified to

$$\frac{\partial^2}{\partial x^2}V_1(x,s) = \gamma^2V_1(x,s), \tag{7}$$

$$\frac{\partial^2}{\partial x^2}V_2(x,s) = \gamma^2V_2(x,s) + \alpha V_1(x,s), \tag{8}$$

where

$$\gamma = \sqrt{sRC + s^2LC}, \tag{9}$$

$$\alpha = s^2L_mC - sRC_m - s^2LC_m. \tag{10}$$

The solution of (7) is

$$V_1(x,s) = V_+e^{-\gamma x} + V_-e^{+\gamma x}. \tag{11}$$

V_+ and V_- can be solved based on the terminal condition of line 1. The general solution of (8) is

$$V_2(x,s) = (a_1x + c_1)e^{-\gamma x} + (a_2x + c_2)e^{+\gamma x}. \tag{12}$$

a_1 and a_2 are determined by solving the non-homogeneous differential equation, (8).

$$a_1 = -\frac{s^2L_mC - sRC_m - s^2LC_m}{2\gamma}V_+, \tag{13}$$

$$a_2 = \frac{s^2L_mC - sRC_m - s^2LC_m}{2\gamma}V_-. \tag{14}$$

c_1 and c_2 are calculated by using the boundary conditions of line 2. Therefore, all of these coefficients are determined based on boundary conditions, permitting the general closed form solutions of $V_1(x,s)$ and $V_2(x,s)$ to be determined.

The time domain solutions of $V_1(x,s)$ and $V_2(x,s)$ can be obtained by using an inverse Laplace transform. However, in many of these cases, a numerical solution results because the inverse Laplace transform of $\frac{1}{1+e^{-2\gamma x}}$ cannot be derived explicitly. In order to determine a closed form analytical expression for use in chip level noise analysis, some approximating assumptions are necessary.

The propagation factor γ, defined in (9), is

$$\begin{aligned}\gamma &= \sqrt{sRC + s^2LC} = s\sqrt{LC}(1+\frac{R}{sL})^{\frac{1}{2}} \\ &\approx s\sqrt{LC}(1+\frac{R}{2sL}) \qquad sL \gg R.\end{aligned} \tag{15}$$

The assumption of $sL \gg R$ is equivalent to $\omega L \gg R$ in the frequency domain, *i.e.*, the losses are small but not necessary negligible. If the driver output impedances of line 1 and line 2 match the line impedance, no reflections will occur at each of the driver ends. V_+ and V_- can be determined as

$$V_+ = V_{in}(s)/2, \tag{16}$$

$$V_- = e^{-2\gamma l}V_{in}(s)/2, \tag{17}$$

where l is the length of the transmission line. c_1 and c_2 can be calculated based on V_+ and V_- as well as a_1 and a_2,

$$c_1 = \frac{Z(a_1+a_2) + sL_m(V_+ - V_-)}{2(R+sL)}, \tag{18}$$

$$c_2 = a_1 l e^{-2\gamma l} - a_2 l + c_1 e^{-2\gamma l}. \tag{19}$$

By inserting (13), (14), (18), and (19) into (12), the coupling noise voltage on the quiet line for the matched driver condition is determined.

A. Coupling noise voltage at the driver end

For the near end coupling noise voltage V_{NE} on the quiet line, *i.e.*, $x = 0$ in (12),

$$\begin{aligned}\frac{V_{NE}(s)}{V_{in}(s)} &= -\frac{l}{2}e^{-2\gamma l}\frac{s^2L_mC - s^2LC_m - sRC_m}{\gamma} \\ &\quad + \frac{1}{8}(1-e^{-4\gamma l})(\frac{sL_m}{R+sL} + \frac{C_m}{C}).\end{aligned} \tag{20}$$

Assuming the input is a fast ramp signal,

$$V_{in}(t) = \frac{V_{dd}}{\tau_r}[tu(t) - (t-\tau_r)u(t-\tau_r)], \tag{21}$$

where τ_r is the rise time of the input signal. The first constraint for τ_r is $\tau_r \le \tau_0$, where τ_0 is the time of flight delay of the signal through the transmission line, $\tau_0 = l\sqrt{LC}$. This constraint requires that the interconnect inductance not be neglected [17], [18]. The second constraint is from the assumption of $\omega L \gg R$. The frequency corresponding to this rise time is $\omega = 2\pi * 0.33/\tau_r = 2.0/\tau_r$ [19]. This requirement becomes $2\tau_1/\tau_r \gg 1$, where $\tau_1 = L/R$. $e^{-2\gamma l} \approx e^{-2s\tau_0 l - Rl/Z_0}$, where Z_0 is $\sqrt{L/C}$ – the characteristic impedance of a lossless transmission line. Using the approximation of γ in (15) and an inverse Laplace transform, the driver end coupling noise voltage $V_{NE}(t)$ in the time domain is

$$\begin{aligned}
V_{NE}(t) &= -\frac{\tau_0 e^{-\frac{Rl}{Z_0}}V_{dd}}{2\tau_r}V_{n1}(t) + \frac{V_{dd}}{8\tau_r}V_{n2}(t), \\
V_{n1}(t) &= \frac{L_m}{L}V_{n3}(t) - \frac{C_m}{C}V_{n4}(t) - \frac{C_mR}{2CL}V_{n5}(t), \\
V_{n3}(t) &= e^{-\frac{t-2\tau_0}{2\tau_1}}u(t-2\tau_0) - e^{-\frac{t-2\tau_0-\tau_r}{2\tau_1}}u(t-2\tau_0-\tau_r), \\
V_{n4}(t) &= u(t-2\tau_0) - u(t-2\tau_0-\tau_r), \\
V_{n5}(t) &= V_{n8}(t-2\tau_0), \\
V_{n2}(t) &= V_{n6}(t) - e^{-\frac{2Rl}{Z_0}}V_{n6}(t-4\tau_0), \\
V_{n6}(t) &= \frac{L_m}{L}(V_{n7}(t) - V_{n7}(t-\tau_r)) + \frac{C_m}{C}V_{n8}(t), \\
V_{n7}(t) &= \tau_1(1-e^{-\frac{t}{\tau_1}})u(t), \\
V_{n8}(t) &= tu(t) - (t-\tau_r)u(t-\tau_r).
\end{aligned} \tag{22}$$

Each term in $V_{n1}(t)$ is due to the first reflection at the receiver end, where the reflection coefficient is one. $V_{n1}(t)$ is the difference between the inductive coupling noise voltage and the capacitive coupling noise voltage. There are two terms in $V_{n2}(t)$, one term occurs at the same time as when the active driver begins to transition and the other term lags by $4\tau_0$ and is attenuated by $e^{-\frac{2Rl}{Z_0}}$, which is due to the second reflection at the receiver end. $V_{n6}(t)$ is the summation of the inductive coupling noise voltage and the capacitive coupling noise voltage. The steady state voltage of the driver end coupling noise signal is zero. The time for the driver end coupling noise voltage to reach a steady state voltage is approximately $4\tau_0 + \tau_r$.

B. Coupling noise voltage at the receiver end

For the far end noise voltage V_{FE} on the quiet line, where $x = l$ in (12),

$$\begin{aligned}\frac{V_{FE}(s)}{V_{in}(s)} &= -\frac{l}{2}e^{-\gamma l}\frac{s^2L_mC - sRC_m - s^2LC_m}{\gamma} \\ &\quad + \frac{1}{4}(e^{-\gamma l} - e^{-3\gamma l})(\frac{sL_m}{R+sL} + \frac{C_m}{C}).\end{aligned} \tag{23}$$

For a fast ramp input signal, the approximation of γ in (15) and $V_{in}(s)$ are inserted into (23), permitting an inverse Laplace transform to be used to determine the receiver end coupling noise voltage $V_{FE}(t)$ in the time domain.

$$\begin{aligned}
V_{FE}(t) &= -\frac{\tau_0 e^{-\frac{Rl}{2Z_0}}V_{dd}}{2\tau_r}V_{f1}(t) + \frac{V_{dd}}{4\tau_r}V_{f2}(t), \\
V_{f1}(t) &= \frac{L_m}{L}V_{f3}(t) - \frac{C_m}{C}V_{f4}(t) - \frac{C_mR}{2CL}V_{f5}(t), \\
V_{f3}(t) &= e^{-\frac{t-\tau_0}{2\tau_1}}u(t-\tau_0) - e^{-\frac{t-\tau_0-\tau_r}{2\tau_1}}u(t-\tau_0-\tau_r), \\
V_{f4}(t) &= u(t-\tau_0) - u(t-\tau_0-\tau_1), \\
V_{f5}(t) &= (t-\tau_0)u(t-\tau_0) - (t-\tau_1-\tau_0)u(t-\tau_0-\tau_1), \\
V_{f2}(t) &= e^{-\frac{Rl}{2Z_0}}V_{f6}(t-\tau_0) - e^{-\frac{3Rl}{2Z_0}}V_{f6}(t-3\tau_0), \\
V_{f6}(t) &= \frac{L_m}{L}(V_{f7}(t) - V_{f7}(t-\tau_r)) + \frac{C_m}{C}V_{n8}(t),
\end{aligned} \tag{24}$$

and $V_{f7}(t) = V_{n7}(t)$.

$V_{f1}(t)$ represents the difference between the inductive coupling noise voltage and the capacitive coupling noise voltage. The summation of the inductive coupling noise voltage and the capacitive coupling noise voltage is described by $V_{f6}(t)$. The second term in $V_{f2}(t)$ lags the first term by $2\tau_0$ and is also attenuated by e^{-Rl/Z_0}. The steady state voltage of the receiver end coupling noise voltage is also zero. The time for the receiver end coupling noise voltage to reach a steady state voltage is approximately $3\tau_0 + \tau_r$.

III. Comparison with Simulation

To verify the accuracy of the analytical expressions, (22) and (24), that describe the coupling noise voltage at both ends of a quiet line, a criterion is defined to measure the error of these closed form approximations. This criterion quantifies the error between the predicted peak noise voltage and the simulated peak noise voltage, permitting the accuracy of these analytical equations to be determined. The criterion is defined as

$$\epsilon_{peak} = |V_p - V_s|/|V_s|, \tag{25}$$

where V_p is the value of the peak noise voltage predicted by the analytical expressions, and V_s is the peak noise voltage obtained by a circuit simulator (SPICE).

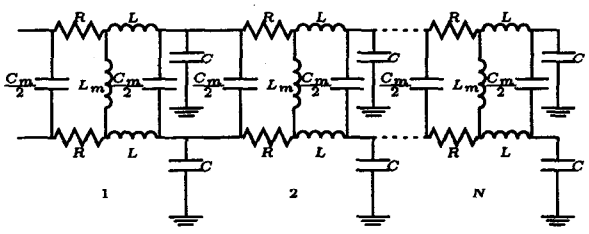

Fig. 2. The SPICE equivalent circuit of a coupled interconnect

The equivalent circuit used in the SPICE simulation analysis is shown in Fig. 2, where N sections of coupled RLC subcircuits are used to approximate two coupled lossy transmission lines. A mutual inductor is used to approximate the coupling inductance. A π model is used to model the coupling capacitance. The parameters used in the SPICE simulation are $R = 3\ \Omega/cm$, $C = 1\ pF/cm$, $L = 2\ nH/cm$, $L_m/L = 0.2$, $C_m/C = 0.1$, $l = 2\ cm$, $V_{dd} = 5.0\ V$, $\tau_r = 120\ ps$, and $N = 20$. The value of two linear resistors, which are used to approximate the driver output impedance, is $R_1 = R_2 = \sqrt{L/C} = 44.72\ \Omega$. Both the analytical and simulation results are depicted in Figs. 3 and 4 for the driver end and the receiver end coupling noise voltage, respectively. The error of the peak noise voltage is within 6.0% at the driver end and less than 1.0% at the receiver end. The initial condition of the quiet line is assumed to be 0 volts, therefore the NMOS transistor is on and the quiet line is connected to ground. The coupling noise voltage at the driver end is momentarily below ground. If the initial condition of the quiet line is V_{dd} (the PMOS transistor is on and the interconnect is connected through the transistor to the power supply), the coupling noise voltage at the driver end may rise above the power supply voltage V_{dd}.

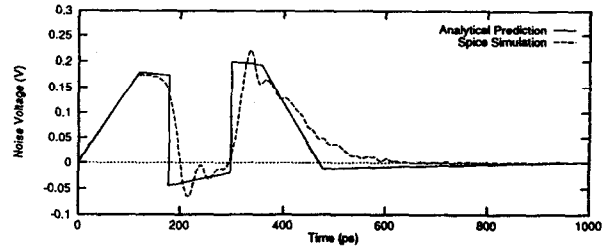

Fig. 3. Coupling noise voltage at the driver end

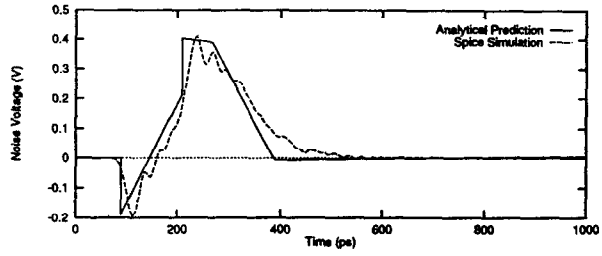

Fig. 4. Coupling noise voltage at the receiver end

The analytically derived noise waveform deviates from the simulated waveform at both ends since the phase difference is neglected, but the predicted waveform follows the shape of the simulated coupling noise voltage. The phase difference due to the signal traveling along the interconnect line can be described in the frequency domain. In the time domain, only the numerical solution can predict the effect of the phase difference. This approach, however, requires significant computation time and computer memory. It is typically prohibitive at the system (or chip) level to predict the effects of the phase difference on the coupling noise.

IV. Discussion

The loosely coupled assumption permits ignoring the effect of the quiet line voltage on the signal waveform on the active line. Both of the capacitive and inductive coupling factors, *i.e.*, C_m/C and L_m/L, are calculated based on different geometric parameters [20]. These results are shown in Fig. 5. The horizontal axis represents the ratio of the spacing between two interconnect lines over the line width. The coupling factors of a non-overlapping line structure are shown in the first two groups. The third group represents the capacitive coupling factor between two coplanar lines. Each group is composed of three different aspect ratios of the interconnect thickness-to-width, *i.e.*, 0.5 (lower line), 1.0 (middle line), and 1.5 (upper line). The line width of the interconnect is 1.6 μm. The loosely coupled assumption is satisfied for most conditions except for a coplanar line structure with a narrow space and high thickness-to-width ratio. However, the distance between the high aspect ratio lines are typically greater than the line width in most practical VLSI circuits.

The validity of these analytical expressions are investigated in this section based on certain assumptions. The fast ramp input constraint, *i.e.*, the high frequency assumption, permits the interconnect to be modeled as a

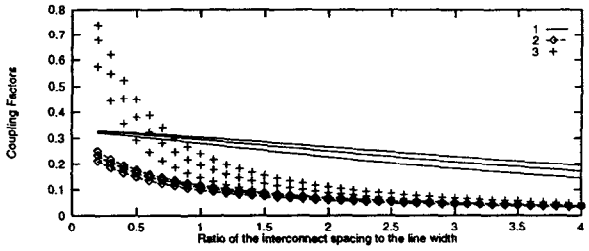

Fig. 5. Coupling factors. Group 1 is the inductive coupling factor and Group 2 is the capacitive coupling factor for a non-overlapping line structure. Group 3 is the capacitive coupling factor between two coplanar lines.

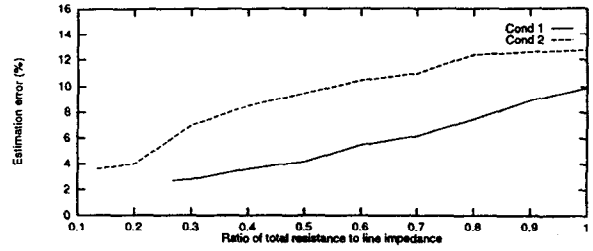

Fig. 7. Estimation of the peak noise voltage of different lossy interconnect lines at the receiver end. The solid line (Cond 1) is the condition τ_1/τ_r=2, and the dashed line (Cond 2) is the condition τ_1/τ_r=4.

low loss transmission line, and the matched load condition at the driver end permits the use of an inverse Laplace transform to obtain explicit solutions in the time domain.

A. Low loss or high frequency assumption

The rise time constraint, *i.e.*, $\tau_r < \tau_0$, is the condition that the interconnect inductance must be included in the interconnect model. If $2\tau_1/\tau_r \gg 1$, *i.e.*, $\omega L > R$ – the assumption made in (15), the interconnect should be modeled as a low loss transmission line under the high frequency condition. Two different regions of operation are defined for medium and high frequencies: condition 1 – medium frequency: $\tau_1/\tau_r \geq 2$, and condition 2 – high frequency: $\tau_1/\tau_r \geq 4$. The total line resistance (Rl) is varied from 0 to $1.0Z_0$ to test for the low and high loss conditions. The error of the peak noise voltage calculation as compared to SPICE is shown in Figs. 6 and 7 at the driver end and the receiver end, respectively. The horizontal axis is the ratio of Rl/Z_0. The error is within 20% at the driver end and 15% at the receiver end for the worst case, *i.e.*, $Rl/Z_0 = 1.0$. If the interconnect is modeled as a high loss transmission line ($Rl \leq 1.0Z_0$), these analytical equations can accurately predict the peak noise voltage.

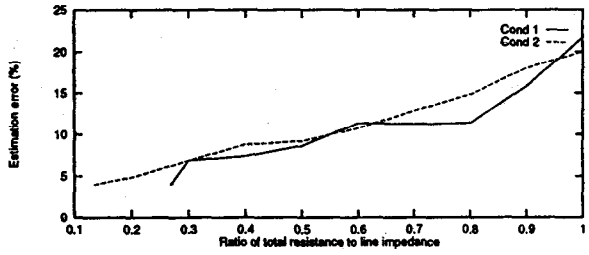

Fig. 6. Estimation of the peak noise voltage of different lossy interconnect lines at the driver end. The solid line (Cond 1) is the condition τ_1/τ_r=2, and the dashed line (Cond 2) is the condition τ_1/τ_r=4.

B. Output impedance of a CMOS driver stage

A second assumption is that the driver impedance matches the line impedance. The following analysis investigates the coupling noise voltage under the condition of a varying driver to load impedance ratio.

B.1 Propagation delay versus driver impedance

Before discussing the relationship between the driver impedance and the coupling noise voltage, the propagation delay of the driver stage is investigated with respect to the active driver impedance. The driver impedance in terms of the propagation delay is shown in Fig. 8. Note that the smaller the driver impedance, the shorter the propagation delay. However, if the driver impedance is less than the interconnect impedance, a negative reflection occurs at the active driver end, and overshoots (the signal rises above the power supply voltage V_{dd}) or undershoots (the signal falls below ground) occur. The overshoot (undershoot) may cause the PN junction of the drain of the PMOS (NMOS) transistor to be forward biased, collecting (injecting) electrons into the substrate, dissipating extra power [7], and delaying the time response. The output voltage of the active driver stage oscillates due to reflections at both ends of the active line before a final steady state voltage is reached.

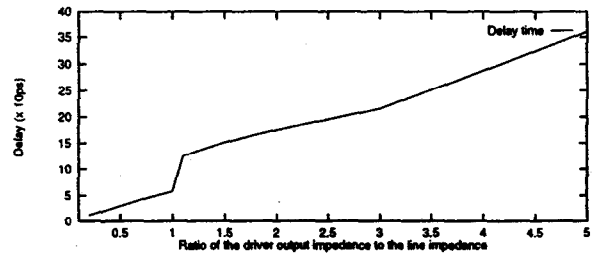

Fig. 8. Propagation delay of the active CMOS driver stage versus the driver impedance

B.2 Relaxation time versus driver impedance

Another effect of low driver impedance is that the relaxation time, the time required for a signal to reach the steady state voltage of the coupling noise voltage on the quiet line, increases. The relationship between the relaxation time of the coupling noise voltage and the active driver impedance is shown in Fig. 9. The waveform of the coupling noise voltage on the quiet line is strongly dependent on the signal transition occurring on the active line. The shortest relaxation time occurs when the active driver impedance matches the line impedance, where no reflections occur at the driver end on the active line. The relaxation time of the coupling noise voltage increases

as the driver impedance deviates from the matched load condition.

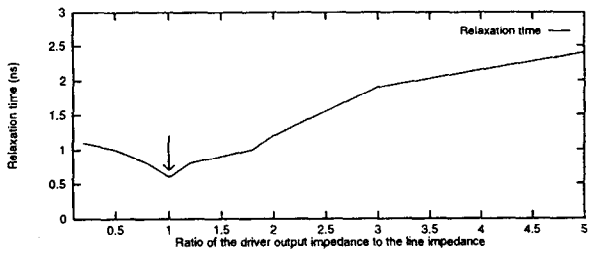

Fig. 9. Relaxation time of the coupling noise on the quiet line versus the driver impedance. Note that when the ratio is equal to one, the relaxation time is at a minimum.

B.3 Power consumption due to the coupling noise

The coupling noise voltage at the driver end of the quiet line causes the NMOS or PMOS transistor to begin operating in the linear region. In order to reduce the propagation delay of the driver stage in high speed CMOS VLSI circuits and decrease the relaxation time of the coupling noise voltage on the quiet line, the driver impedance should be similar in magnitude to the line impedance, permitting the negative reflection at the driver end to be minimized.

B.4 Non-matching driver impedance

The peak noise voltage for a variety of driver impedances is shown in Fig. 10. The peak noise voltage decreases as the driver impedance increases. The maximum error of the peak noise voltage as compared to SPICE simulation is less than 15% at the driver end and within 20% at the receiver end of the quiet line where the driver impedance is in the range of $0.8Z_0$ to $2.0Z_0$. These analytical equations, (22) and (24), can therefore be used as a first order approximation to predict the coupling noise voltage in high speed CMOS VLSI circuits.

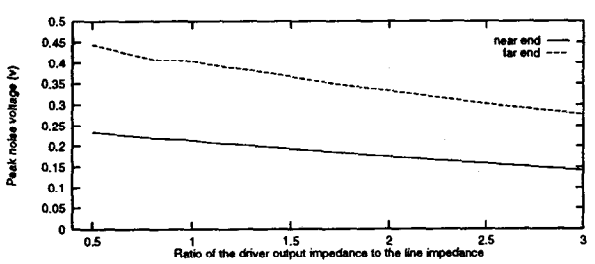

Fig. 10. Peak noise voltage versus the driver impedance

V. Conclusions

Closed from expressions for the peak coupling noise voltage between two neighboring interconnect lines in CMOS VLSI circuits have been presented for different load and waveform conditions. These equations provide an estimate of the coupling noise voltage with an error within 20% at both ends of the quiet line.

In the design of high speed CMOS VLSI circuits, the driver impedance should be comparable to the line impedance in order to reduce the propagation delay of the CMOS driver stage, minimize the reflection at the driver end, and decrease the relaxation time of the coupling noise voltage on the quiet line. The closed form expressions presented in this paper can be used to estimate the peak value of the coupling noise voltage for lossy interconnect in CMOS VLSI circuits.

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