The Behavior of Digital Circuits under Substrate Noise in a Mixed-Signal Smart-Power Environment

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Abstract—**The behavior of digital circuits in a noisy environment in mixed-signal smart-power systems is described in this paper. Several models and mechanisms explaining the process in which substrate noise affects on-chip digital circuits as well as the noise immunity behavior of digital circuits are presented and discussed. The models and mechanisms are demonstrated by simulations and by extensive test chip-based experimental data.**

I. Introduction

The proper operation of integrated circuits can be greatly affected by noise, and in mixed-signal circuits in particular, by on-chip substrate coupling noise [1]. Existing research in substrate coupling noise in mixed-signal circuits has concentrated on the problem of the digital circuitry influencing the highly sensitive analog circuitry [2–7]. The interaction between the high power analog drivers and the digital latches where both are on the same monolithic substrate is schematically shown in Fig. 1 and is the topic of this paper. The analog power drivers generate substrate noise that is transmitted through the common substrate and received by the sensitive digital latches. The objective of this paper is to present the principal models and mechanisms that explain the process in which substrate noise affects the digital circuits in a smart-power environment. These models and mechanisms permit the development of reliable circuit and noise immune design techniques.

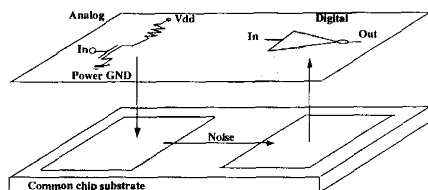

Fig. 1. Noise coupling in smart-power circuits

Specific details of the test circuits are discussed in Section II. The principal aspects of the generation, transmission, and reception of on-chip noise in a mixed-signal smart-power environment are reviewed. In Section III, several models and mechanisms that explain the process in which substrate noise affects on-chip digital circuits are presented and discussed. Circuit simulations characterizing these models and mechanisms for an NMOS static inverter and latch are presented in Section IV. The experimental data (see [8] for additional data) derived from evaluating a large number of test circuits designed and fabricated in a high voltage NMOS process [9] confirm the expected behavior of the digital circuits according to the models, mechanisms, and simulations described in this paper. Finally, some conclusions are drawn in Section V.

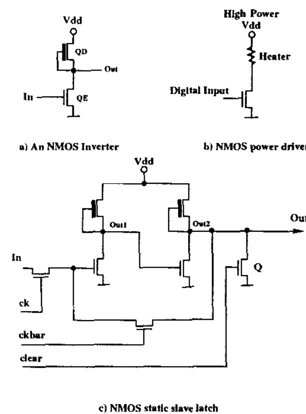

Fig. 2. Circuit schematic of primary NMOS circuit blocks

II. Basic elements

The sensitive circuitry consists primarily of latched inverters (see Figs. 2a and c). The noise source consists of analog power drivers (see Fig. 2b). The noise behavior of dynamic as well as static NMOS circuits is experimentally analyzed. A microphotograph of a test circuit from the main group of test circuits [8] is shown in Fig. 3 and of the latch-predriver-driver interface in Fig. 4.

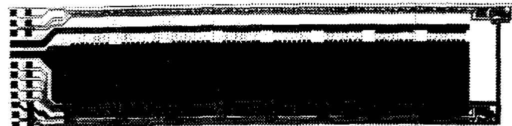

Fig. 3. Microphotograph of the primary mixed-signal test circuit

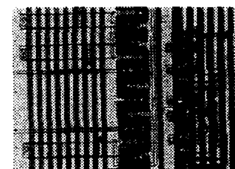

Fig. 4. Microphotograph of the latch-predriver-driver interface

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The generation, transmission, and reception of substrate noise depends upon issues such as the implementing technology, substrate doping and thickness, the distance between the noise source and the noise receptor, the presence and placement of substrate contacts, guard rings, and wells, the backplane substrate contact, circuit switching speed and transition times, the routing of the power lines, inductive effects, and circuit placement and orientation [2–7]. It is experimentally demonstrated in [8] that for a smart-power application, the generated noise is strongly dependent upon the supply voltage, the switched current of the power driver, the duration of the noise pulse, and the number of drivers that are active at any one time. The effect of the received noise is also shown in [8] to depend upon the clock and signal conditioning of the digital circuits, chip temperature, and the common or separated grounds between the analog and digital blocks.

In a smart-power application, due to the high voltages and currents that are switched by the analog power driver, a significant substrate noise is generated. However, for a logic element, only the amount of noise that induces a change of state at the output is important. The objective of the research presented in this paper is to describe the noise behavior of digital circuits for a standard high voltage, low cost semiconductor process which has not been optimized to provide low substrate noise levels. Based on this behavior, circuit and physical design techniques are developed to improve the noise immunity of the digital circuits. In a more complex semiconductor process, where the substrate noise levels are lower, these design techniques can be used to significantly reduce the probability that the digital circuits are affected by noise.

III. Models and mechanisms

Several models and mechanisms are proposed and discussed in this paper that explain the process in which substrate coupling noise affects on-chip digital circuits. The principal mechanism is that the transmitted substrate noise affects different transistors of a logic element at different times. The noise affects each transistor depending upon the *noise transmission* process, the *body effect*, the *operating point and region of operation* of a transistor, the *noise induced forward biasing effects*, the *logic family*, and the *voltage transfer characteristic*, all of which are reviewed below.

1. **Noise transmission** through the substrate:

(a) The negative and positive substrate voltage transients generated during the on–off switching of the power drivers are transmitted through the substrate.

(b) The substrate, in the direction of the transmitted noise signal, can be modeled as a distributed RC line.

(c) The noise signal delay between two substrate points depends upon the RC characteristics of the substrate.

The noise through the substrate can be non-uniform. Depending upon the position and orientation of the sensitive circuitry with respect to the noise source(s), each transistor can receive similar or different amounts of noise.

2. **Body effect.** The threshold voltage (V_T) variations induced by the negative and positive noise voltage transients within the substrate create a noise spike V_{pp} at the output of an analog element [2, 4, 5] as depicted in Fig. 5. The noise induced V_T variations can also affect the output state of a digital element.

3. **The operating point and region of operation of a transistor.** For the same bias (V_{GS}), geometric size, and noise conditions, a transistor operating in the linear region is less sensitive to noise than a transistor operating in saturation. If both transistors are saturated, V_{pp} increases as I_{DS} increases and the smaller the geometric size and/or the larger V_{GS} is, the smaller V_{pp} is.

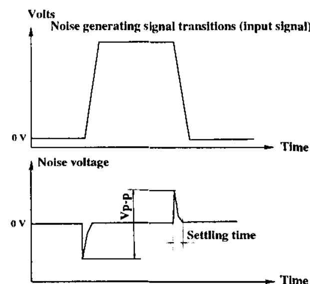

Fig. 5. Characteristic noise waveform caused by digital switching

4. **Noise induced forward biasing effects.** If the inverter shown in Fig. 2a is driven by $In = high$, then Q_E is in the linear region and $Out = low$. A positive substrate voltage transient greater than about 0.7 V can forward bias the substrate-to-drain, substrate-to-source, and substrate-to-channel junctions. A current I_{vn} which depends upon the amplitude of the transient substrate voltage is injected from the substrate into the forward biased junctions. The current injected by Q_D will decrease, and accordingly, V_{out} will increase. The equivalent schematic of the inverter in the final state is shown in Fig. 6, where, depending upon the value of V_n, one to k diodes, D1...Dk, are connected between the source of Q1 and ground. Q1, which is geometrically smaller than Q_E, operates in most cases in the linear region, satisfying the conditions, $I_{dtx} = I_{etx}$ and $I_{etx} + I_{vnk} = I_k$.

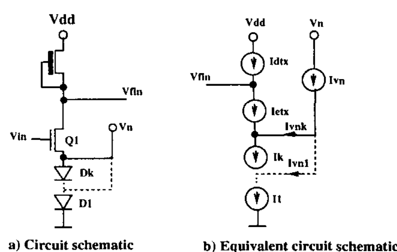

Fig. 6. The equivalent circuit schematic of the NMOS inverter shown in Fig. 2a for a large positive substrate noise transient

5. **The importance of the logic family.** The sensitivity of a logic element to noise depends upon the logic family in which it is implemented through issues such as the type of transistors that constitute the logic element, the presence and magnitude of a DC current during any of the states, the transistor size, and the voltage transfer characteristic of the logic family.

6. **The Voltage Transfer Characteristic (VTC).** A VTC is characterized by the V_{OH} (the maximum output voltage when the output level is logic "1"), V_{OL} (the minimum output voltage when the output level is logic "0"), V_{IL} (the maximum input voltage which can be interpreted as a logic "0"), and V_{IH} (the minimum input voltage which can be interpreted as a logic "1"). For two serially connected logic elements, such as two inverters forming a latch (see Fig. 2c), the possible conditions under which a parasitic glitch induced by noise at *Out*1 can be transmitted to *Out*2 are listed in Table I. V_{TEN} and V_{TDN} are the enhancement and depletion threshold voltages under the influence of noise while *fb* signifies *forward biasing effects*. Note that different families with different VTCs require different values of V_{out1} to transmit a parasitic voltage glitch.

All of the six issues contribute to the noise behavior of a digital logic family in a smart-power mixed-signal environment. Consider the circuit shown in Fig. 7 in which two inverters are connected as an open loop static latch. The distributed RC substrate impedance models the transmission medium among the four transistors in the direction of the traveling noise signal. Each transistor is affected by a different noise amplitude at different times depending upon the circuit placement (or the noise input node, defined as the closest point to the noise source) and the RC elements (see Table II).

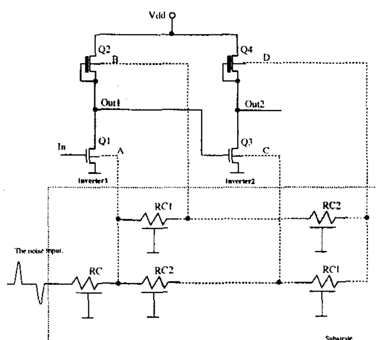

Fig. 7. Two NMOS inverters with substrate noise. The noise path is shown. The substrate is modeled as a distributed RC mesh.

IV. Simulations and Experimental Results

An NMOS inverter and static latch have been analyzed according to these models using Cadence Spectre [10]. Pulse voltage sources with values between +5 and -5 V are connected at the A, B, C, and D nodes shown in Fig. 7 to simulate different substrate noise conditions listed in Table II, and the C and D substrate noise inputs.

For an NMOS inverter, the conditions shown in Table I to induce a parasitic transition are satisfied only for $In = high$ (the input of the inverter) and for positive substrate voltage transients. The output swing of the parasitic transition depends upon the duration and magnitude of the noise pulse, the transistor size, and the capacitive load of the inverter. The minimum noise amplitude for $k_E/k_D = 4$ and $C_L = 10$ fF, necessary to induce a significant parasitic transition (see Table I), is ≈ 1.7 V. If Q_D is affected by noise before Q_E, the source-to-substrate junction of Q_D is forward biased, and the output is ≈ 0.6 V below the substrate bias at Q_D.

TABLE I
The possible conditions under which a parasitic glitch at Out1 is transmitted to Out2

Input	Condition
High	$V_{out1} \geq V_{IH}(V_{TEN}, V_{TDN}, fb)$ $V_{out1}(V_{TEN}, V_{TDN}, fb) \geq V_{IH}$ $V_{out1}(V_{TEN}, V_{TDN}, fb) \geq V_{IH}(V_{TEN}, V_{TDN}, fb)$
Low	$V_{out1} \leq V_{IL}(V_{TEN}, V_{TDN}, fb)$ $V_{out1}(V_{TEN}, V_{TDN}, fb) \leq V_{IL}$ $V_{out1}(V_{TEN}, V_{TDN}, fb) \leq V_{IL}(V_{TEN}, V_{TDN}, fb)$

TABLE II
Different situations for the noise signal affecting the threshold voltage of Q1, Q2, Q3, and Q4 (see Fig. 7)

No.	Situation	Comments
1.	RC1, RC2 negligible	The noise signal affects all transistors at the same time
2.	RC1 negligible	Q1, Q2 are affected first, then Q3, Q4 after a delay
3.	RC2 negligible, A input	The affected order is Q1 and Q3, than Q2 and Q4
4.	RC2 negligible, B input	The affected order is Q2 and Q4, than Q1 and Q3
5.	A input	The affected order is Q1, Q2, Q3, Q4 or Q1, Q2 and Q3, Q4 or Q1, Q3, Q2, Q4
6.	B input	The affected order is Q2, Q1, Q4, Q3 or Q2, Q1 and Q4, Q3 or Q2, Q4, Q1, Q3

An open loop analysis of an NMOS static latch shown in Fig. 7 for each of the conditions listed in Tables I and II has been performed. Combinations of the amplitude of the substrate voltage, transistor size, and capacitive load are considered for each condition. All situations can be described by two major cases: the noise at inverter1 and inverter2 is "*in phase*" (as shown in Fig. 8), meaning that all transistors are affected by noise at the same time, or the noise *is not in phase* (as shown in Fig. 9).

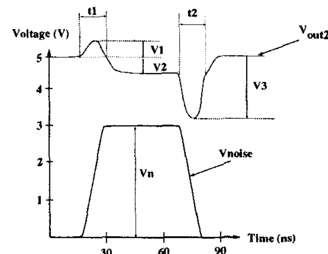

Fig. 8. A typical waveform representing Out2 when the noise voltages at A, B, C, and D for the circuit shown in Fig. 7 are in phase

Note that when the noise is in phase, V_3 may be significant and can be interpreted as a logic low. V_3 can reach a maximum of 2.6 V for $V_n = 4$ V, $k_E/k_D = 4$, and $C_L = 10$ fF, which is greater than V_{IL}. If inverter1 is loaded significantly more than inverter2 (1 pF vs. 10 fF), V_3 can reach 5 V (for $V_n = 4$ V) which is smaller than V_{IL} (see Table I). Also, V_3 increases as k_E/k_D increases.

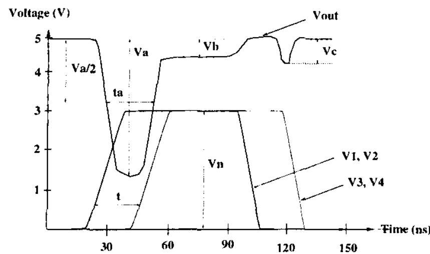

Fig. 9. A typical waveform representing Out2 when the noise voltages at A, B, C, and D for the circuit shown in Fig. 7 are not in phase

When the noise is not in phase, inverter1 is affected by noise while inverter2 is not affected, inducing a significant parasitic transition at Out2. Note that for $In = low$ and therefore $Out1 = high$, inverter2 is susceptible to noise.

For a closed loop static latch (the pass transistors are on in Fig. 2c), a parasitic transition at Out2 for $In = low$ is latched only for large phase differences between the noise at inverter1 and inverter2. This behavior is unlikely in practical applications since inverter1 and inverter2 are typically physically close on-chip. Accordingly, for a static NMOS latch, a parasitic transition induced by noise will be latched only if $In = high$.

Extensive experimental data as described in [8] confirm that

- A parasitic transition can be latched only for $In = high$. For a dynamic register, the experimental data verifies the theory showing that a parasitic transition can be latched for both $In = high$ and $In = low$.
- The Q transistor (see Fig. 2c) in the slave latch is responsible for the dependency of the noise tolerance as a function of the clock state [8] due to the increased *forward biasing effects* at the output of the slave latch. Also, the nonuniformities of the substrate noise affect a specific register location as a function of the clocking regime.
- It is experimentally shown that particular registers can be randomly affected from one noise pulse to another. Per the previous comment, the noise phase between inverter1 and inverter2 for a register may be at the limit of producing a significant transition.
- Some of the experimental data shown in [8] characterize the behavior of a digital circuit under noise as a function of distance, substrate contact placement, register position and orientation, power supply voltage and current of the power drivers, and the number of active drivers. This data can also be explained by the variation of the noise magnitude, the phase, and any substrate noise nonuniformities.

The noise immunity of a digital logic family and, in particular, of a static NMOS logic family can be improved by employing several noise mitigation techniques, such as

- The output of each logic element should have equal loads (preferably large capacitive loads if a slower speed is acceptable).
- A physical design style with substrate contacts for each transistor together with a low resistivity metal layer connecting all the substrate contacts and grounds is beneficial since the noise remains in phase for all of the logic elements. Accordingly, the noise wave affects all of the latch elements simultaneously, therefore no effect is noted, independent of the magnitude of the noise.
- A compact layout is beneficial since the RC delays between the transistors of each latch are minimized.
- A symmetric floorplan with respect to the noise source, if possible, will permit each logic element to receive a similar amount of noise.
- A substrate with a reduced capacitance or with a low resistance (a high doping concentration) is beneficial. However, a high voltage process necessitates a low doping concentration in the substrate. A non-epitaxial process is preferable due to the lower capacitance.

V. Conclusions

Fundamental questions with respect to the noise behavior of digital circuitry in a smart-power mixed-signal environment are discussed. Several physical models and mechanisms are confirmed by simulations and extensive experimental data for both static and dynamic NMOS registers. Good agreement is obtained among the model analysis, simulation results, and experimental data, permitting the development of several noise mitigation techniques and design guidelines.

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