Inductive Characteristics of Power Distribution Grids in High Speed Integrated Circuits

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Abstract— **The inductive characteristics of several types of gridded power distribution networks are described in this paper. The inductance extraction program FastHenry is used to evaluate the inductive properties of grid structured interconnect. In power distribution grids with alternating power and ground lines, the inductance is shown to vary linearly with grid length and inversely linearly with the number of lines in the grid. The inductance is also relatively constant with frequency in these grid structures. These properties provide accurate and efficient estimates of the inductance of power grid structures with various dimensions.**

Keywords —**inductance, mutual inductance, partial inductance, power distribution networks, power grids**

I. Introduction

THE ongoing miniaturization of integrated circuit (IC) feature size has placed significant requirements on the power and ground distribution network. Circuit integration densities rise with every technology generation due to smaller devices and larger dies; the current density and the total current increase accordingly. At the same time, the higher speed switching of smaller transistors produces faster current transients in the power distribution network. The higher currents cause larger ohmic IR voltage drops while fast current transients cause large inductive $L\frac{di}{dt}$ voltage drops (ΔI noise) in the power distribution networks. Power distribution networks are therefore designed to minimize these current transients, maintaining the local supply voltage within specified design margins.

To satisfy these tight specifications, a power distribution network should be low impedance as seen from the power terminals of the circuit elements. With transistor switching times as low as a few picoseconds, the on-chip signals typically contain significant harmonics at frequencies as high as ~ 100 GHz. For on-chip wires, the inductive reactance ωL dominates the overall wire impedance beyond ~ 10 GHz. The on-chip inductance affects the integrity of the power supply through two phenomena. First, the magnitude of the ΔI noise is directly proportional to the power network inductance as seen at the current sink. Second, the network resistance, inductance, and decoupling capacitance form an RLC system with multiple resonances.

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Power distribution networks in high performance digital ICs are commonly structured as a multilayer grid, as shown in Fig. 1. In such a grid, straight power/ground (P/G) lines in each metalization layer span the entire die (or a large functional unit) and are orthogonal to the lines in the adjacent layers. The power and ground lines are typically interdigitated within each layer. Vias are used to connect a power (ground) line to other power (ground) lines in the adjacent metal layers.

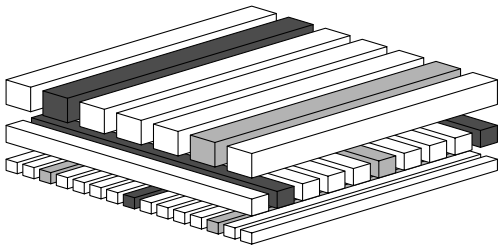

Fig. 1. A multilayer interconnect with the power distribution grid highlighted; the ground lines are light grey, the power lines are dark grey, and the signal lines are white.

The paper is organized as follows. Existing work on the design of power distribution networks in high complexity digital circuits is surveyed in Section II. The relationship between the inductive characteristics in a general power transmission structure is established in Section III. The three types of grid structures analyzed in this paper are described in Section IV. The dependence of the inductance characteristics on the line width is discussed in Section V. The differences in the inductive properties among the three types of grids are reviewed in Section VI. The dependence of the grid inductance on grid dimensions is described in Section VII. The dependence of the grid inductance on frequency is discussed in Section VIII. Specific conclusions are summarized in Section IX.

II. Background

The problem of optimizing on-chip multilevel power distribution grids has been considered by Song and Glasser [1]. In their early work published in 1986, a simple model is presented to estimate the maximum on-chip IR drop as a function of the number of metal layers and the metal layer thickness. The optimal thickness of each metal layer to produce minimum IR drops is determined. Design guidelines are provided to maximize signal wiring area while maintaining a constant IR drop. Application of these results to current high

complexity integrated circuits is, however, limited.

An alternative approach for on-chip power distribution called a "cascaded power/ground ring" has been proposed by Cao and Krusius [2]. This approach focuses on maximizing the amount of wiring resources available for signal routing.

The inductance of on-chip power distribution networks has traditionally been neglected because the network inductance has been dominated by the parasitic inductance of the package pins, traces, and bond wires. The situation is rapidly changing due to increasing die size (and length of the on-chip power lines) and the lower inductance of flip chip packaging. Priore noted in [3] that replacing wide power and ground lines with narrower interdigitated power and ground lines reduces the self inductance of the supply network. He also suggested an approximate expression for the time constant of the response of a power supply network to a voltage step input signal. Zheng and Tenhunen [4] proposed replacing the wide power and ground lines with an array of interdigitated narrow power and ground lines with the purpose of reducing the switching voltage transients on the power bus by decreasing the characteristic impedance of the power network.

The construct of a partial self and mutual inductance is useful in evaluating the inductive properties of high speed circuits. The concept of a partial inductance was first developed by Rosa in 1908 in application to linear conductors [5]. The partial (self and mutual) inductance is intended to represent the inductance that a circuit segment contributes *as a part of a closed loop circuit*. A rigorous theoretical treatment of the subject was first provided by Ruehli in [6], where a general definition of the partial inductance of an arbitrarily shaped conductor is given in terms of the magnetic vector potential. Analytical expressions characterizing the self and mutual partial inductance of straight line segments as a function of the line dimensions are presented in [7] for various cross section shapes and mutual orientations.

The inductance extraction program FastHenry [8] is used in this work to explore the inductive properties of these interconnect structures. A conductivity of 58 $S/\mu\text{m} \simeq (1.72\ \mu\Omega \cdot cm)^{-1}$ is assumed for the interconnect material. A wire thickness of 1 μm is assumed for the wire structures.

The inductance of the on-chip structures can decrease significantly with signal frequency. It is, therefore, important to choose the relevant frequency when evaluating the inductance. This decrease in inductance with frequency is due to several effects. With the onset of the skin effect the wire current concentrates near the wire surface, reducing the internal inductance of the wire. In closely placed wires, the proximity effect shifts the current distribution profile across the wire cross section so as to minimize the circuit inductance, as shown in Fig. 2. These mechanisms have, however, an insignificant effect on the effective inductance in integrated circuit structures. The primary cause of the decrease in inductance with frequency is the variability of the current return path.

In this investigation, a frequency of 1 GHz is used to analyze the low frequency case, where the reactance is comparable to the resistance but does not yet dominate the interconnect impedance for typical on-chip wires. A frequency of 100 GHz is used to analyze the high frequency case, where the wire reactance completely dominates the impedance and the wire resistance has a minimal effect on the inductive properties of the circuit.

Fig. 2. Current density distribution in the cross section of two closely spaced wires. Darker shades of gray indicate higher current densities. In wires carrying current in the same direction (parallel currents), the current concentration is shifted away from the parallel current, minimizing the circuit inductance. In wires carrying current in opposite directions (antiparallel currents), the current concentrates toward the antiparallel current, also minimizing the circuit inductance.

III. Power transmission circuit

Consider the simple power transmission circuit shown in Fig. 3a. The circuit consists of a power line and a ground line forming a transmission path between the power supply at one end of the path and a power consuming circuit at the other end. The circuit dimensions are assumed to be sufficiently small for the lumped circuit approximation to be valid. The inductance of both terminating devices is assumed negligible as compared to the inductance of the power lines. The inductive characteristics of the circuit can therefore be determined by the inductive properties of the transmission wires.

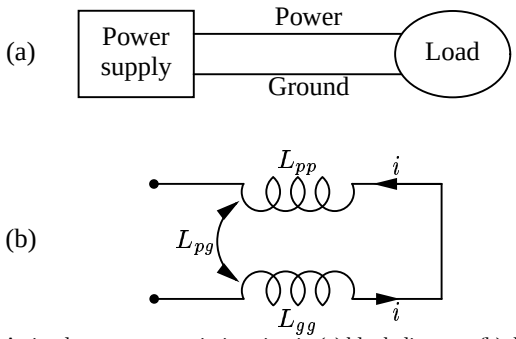

Fig. 3. A simple power transmission circuit; (a) block diagram, (b) the equivalent inductive circuit.

The power transmission loop consists of two wires. The equivalent inductive circuit is depicted in Fig. 3b. The inductance matrix for this circuit is

$$L_{ij} = \begin{bmatrix} L_{pp} & -L_{pg} \\ -L_{gp} & L_{gg} \end{bmatrix}, \tag{1}$$

where L_{pp} and L_{gg} are the partial self inductances of the power and ground lines, respectively, and L_{pg} is the absolute value of the partial mutual inductance between the lines. The loop inductance is

$$L_{loop} = L_{pp} + L_{gg} - 2L_{pg}. \tag{2}$$

The mutual coupling L_{pg} between the power and ground lines reduces the loop inductance. This behavior can be formulated

more generally: *the greater the mutual coupling between antiparallel (flowing in opposite directions) currents, the smaller the loop inductance of a circuit*. The effect is particularly significant when the wire separation is comparable to the dimensions of the wire cross section and the mutual inductance is comparable to the self inductance of the wires.

The effect of the coupling is reversed when the current in the elements flows in the same direction. For example, in order to reduce the partial inductance L_{11} of wire segment 1, another wire segment 2 with self inductance L_{22} and coupling L_{12} is placed in parallel with segment 1. A schematic of the equivalent inductance is shown in Fig. 4. The resulting inductance of the current path is

$$L_{1\|2} = \frac{L_{11}L_{22} - L_{12}^2}{L_{11} + L_{22} - 2L_{12}}. \quad (3)$$

For the limiting case of no coupling, this expression simplifies to $\frac{L_{11}L_{22}}{L_{11}+L_{22}}$. In the opposite case of full coupling of segment 1, $L_{11} = L_{12}$ ($L_{11} \leq L_{22}$) and the total inductance becomes L_{11}. For two identical parallel elements, (3) simplifies to $L_{\|} = (L_{self} + L_{mutual})/2$. In general, *the greater the mutual coupling between parallel (flowing in the same directions) currents, the greater the loop inductance of a circuit*. To present this concept in an on-chip perspective, consider a 1000 μm long power line with a $1\,\mu\text{m} \times 3\,\mu\text{m}$ cross section, and a partial self inductance of 1.342 nH (at 1 GHz). Adding another identical power line in parallel with the first line with a 17 μm separation (20 μm line pitch) results in a mutual line coupling of 0.725 nH and a net inductance of 1.033 nH ($\sim 55\%$ higher than $L_{self}/2 = 0.671$ nH).

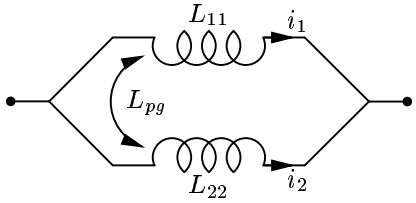

Fig. 4. Two parallel coupled inductors.

To minimize the circuit inductance, the coupling of wires carrying unidirectional current can be reduced by increasing the distance between the lines. The coupling of wires carrying current in opposite directions should be increased by physically placing the lines closer to each other.

This optimization naturally occurs in grid structured power distribution networks with interdigitated power and ground lines. To demonstrate this effect, the following three types of power/ground grid structures composed of coplanar parallel lines are described in the following section.

IV. Grid types

To assess the dependence of the inductive properties on the power and ground lines, the coupling characteristics of three types of power/ground grid structures have been analyzed. In the grids of the first type, called *non-interdigitated grids*, the power lines fill one half of the grid and the ground lines fill the other half of the grid, as shown in Fig. 5a. In *interdigitated grids*, the power and ground lines are alternated and equidistantly spaced, as shown in Fig. 5b. The grids of the third type are a variation of the interdigitated grids. The power and ground lines are interdigitated, but rather than placed equidistantly, the lines are placed in equidistantly spaced pairs of adjacent power and ground lines, as shown in Fig. 5c. These grids are henceforth called *paired grids*.

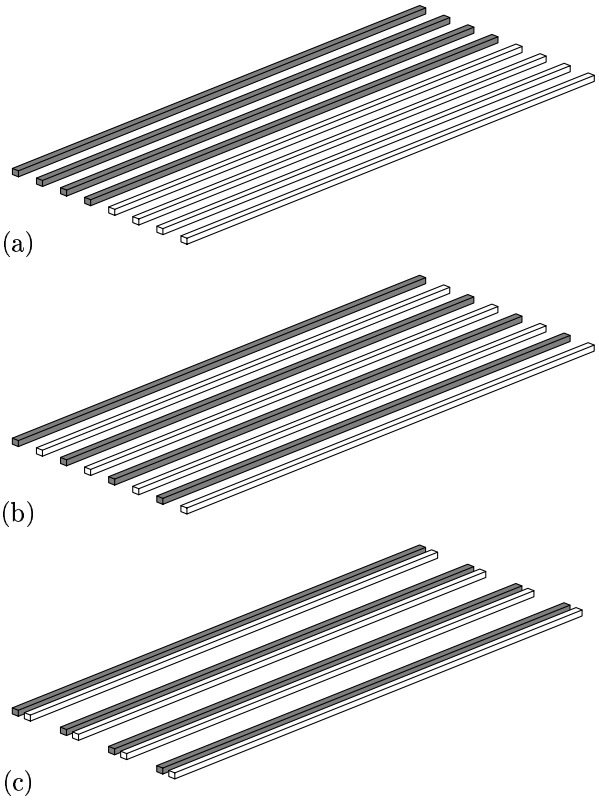

Fig. 5. Power/ground grid structures under investigation; (a) a non-interdigitated grid, (b) a grid with the power lines interdigitated with the ground lines, (c) a paired grid, the power and ground lines are in close pairs. The power lines are grey colored, the ground lines are white colored.

The number of power lines matches the number of ground lines in all of the grid structures. The number of power/ground line pairs is varied from one to ten (the structures of the two types are identical with only one power/ground line pair). The grid lines are assumed to be 1 mm long and are placed on a 20 μm pitch. The specific line length is unimportant since at these high length to cross-sectional dimension ratios the inductance scales nearly linearly with the line length.

An analysis of these structures has been performed for two line cross sections, $1\,\mu\text{m} \times 1\,\mu\text{m}$ and $1\,\mu\text{m} \times 3\,\mu\text{m}$. For each of these structures, the following characteristics have been determined: the partial self inductance of the power (forward current) and ground (return current) paths L_{pp} and L_{gg}, respectively, the power to ground path coupling L_{pg}, and the

loop inductance L_{loop}. Due to the symmetry of the power and ground paths, $L_{gg} = L_{pp}$ and the relation of the loop inductance to the partial inductance simplifies to

$$L_{loop} = L_{pp} + L_{gg} - 2L_{pg} = 2(L_{pp} - L_{pg}). \qquad (4)$$

The loop inductance of the three types of grid structures operating at 1 GHz is displayed in Fig. 6 as a function of the number of lines in the grid. The partial self and mutual inductance of the power and ground current paths is shown in Fig. 7 for grid structures with $1\,\mu\text{m} \times 1\,\mu\text{m}$ cross section lines and in Fig. 8 for grids with $1\,\mu\text{m} \times 3\,\mu\text{m}$ cross section lines. The data shown in Figs. 6, 7, and 8 are discussed in the following three sections.

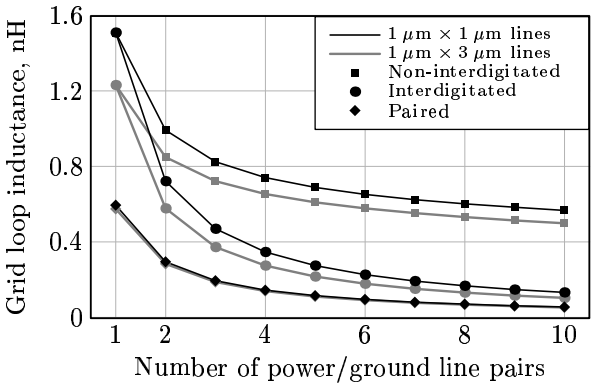

Fig. 6. Loop inductance of the power/ground grids as a function of the number of power/ground line pairs (at a 1 GHz signal frequency).

V. Inductance versus line width

The loop inductance of the grid depends relatively weakly on the line width. Grids with $1\,\mu\text{m} \times 3\,\mu\text{m}$ cross section lines have a lower loop inductance than grids with $1\,\mu\text{m} \times 1\,\mu\text{m}$ cross section lines but this decrease in inductance is dependent upon the grid type, as shown in Fig. 6. The largest decrease, approximately 21%, is observed in interdigitated grids. In non-interdigitated grids, the inductance decreases by approximately 12%. In paired grids, the decrease in inductance is limited to 3% to 4%.

This behavior can be explained in terms of the partial inductance, L_{pp} and L_{pg}. According to (4), L_{loop} increases with larger L_{pp} and decreases with larger L_{pg}. Increasing the line width affects both L_{pp} and L_{pg}. The self inductance of a single wire is a weak function of the wire cross-sectional dimensions [7]; this behavior is also true for the complex structures under investigation. Comparison of the data shown in Fig. 7 with the data shown in Fig. 8 demonstrates that changing the wire cross section from $1\,\mu\text{m} \times 1\,\mu\text{m}$ to $1\,\mu\text{m} \times 3\,\mu\text{m}$ decreases L_{pp} by 4% to 6% in all of the multiwire structures. The impact on L_{pg} is less uniform: in those structures where the line spacing is much larger than the line width (non-interdigitated and interdigitated grids), L_{pg} changes insignificantly; in paired grids with adjacent lines, L_{pg} decreases by

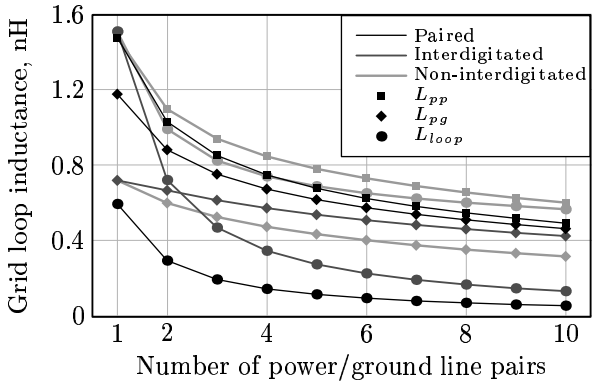

Fig. 7. Loop and partial inductance of the power/ground grids with $1\,\mu\text{m} \times 1\,\mu\text{m}$ cross section lines (at a 1 GHz signal frequency).

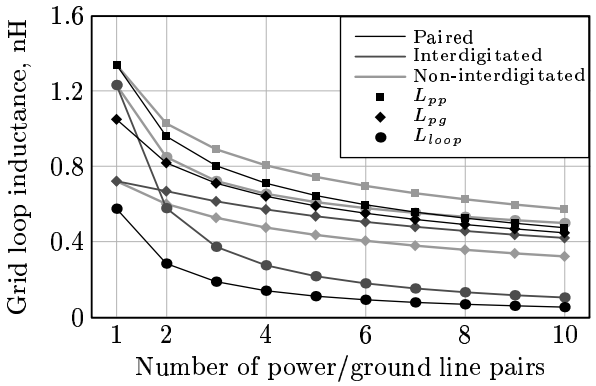

Fig. 8. Loop and partial inductance of the power/ground grids with $1\,\mu\text{m} \times 3\,\mu\text{m}$ cross section lines (at a 1 GHz signal frequency).

4% to 6%, as quantified by comparison of the data shown in Fig. 7 with the data shown in Fig. 8. Therefore, the loop inductance L_{loop} in the non-interdigitated and interdigitated grids with a $1\,\mu\text{m} \times 3\,\mu\text{m}$ cross section is primarily reduced by decreasing L_{pp} while for paired grids, a reduction in L_{pp} is significantly offset by a decrease in L_{pg}.

VI. Dependence of inductance on grid type

The grid inductance varies with the configuration of the grid. With the same number of power/ground rails, grids with interdigitated power and ground lines exhibit a lower inductance than non-interdigitated grids; this behavior is discussed in subsection VI-A. The inductance of the paired grids is lower than the inductance of the interdigitated grids; this topic is discussed in subsection VI-B.

A. Non-interdigitated versus interdigitated grids

The difference in inductance between non-interdigitated and interdigitated grids increases with the number of wires, reaching an approximately 4.2 difference for ten power/ground line pairs for the case of a $1\,\mu\text{m} \times 1\,\mu\text{m}$ cross section line, as shown in Fig. 6 (~ 4.7 difference for the case of a $1\,\mu\text{m} \times 3\,\mu\text{m}$ cross section line). This difference is due to two factors.

First, in non-interdigitated grids the lines carrying current in the same direction (forward or return) are spread over half the width of the grid, while in the interdigitated (and paired) grids both the forward and return paths are spread over the entire width of the grid. The smaller the separation between the lines, the greater the mutual inductive coupling between the lines and the partial self inductance of the forward and return paths, L_{pp} and L_{gg}. This trend is confirmed by the data shown in Figs. 7 and 8, where interdigitated grids have a lower L_{pp} as compared to non-interdigitated grids.

Second, each line in the interdigitated structures is surrounded with lines carrying current in the opposite direction, creating strong coupling between the forward and return currents and increasing the partial mutual inductance L_{pg}. Alternatively, in the non-interdigitated arrays (see Fig. 5a), all of the lines (except for the two lines in the middle of the array) are surrounded with lines carrying current in the same direction. The power-to-ground inductive coupling L_{pg} is therefore lower in non-interdigitated grids, as shown in Figs. 7 and 8.

Thus, the interdigitated grids exhibit a lower partial self inductance L_{pp} and a higher partial mutual inductance L_{pg} as compared to non-interdigitated grids. Therefore, the interdigitated grids have a lower loop inductance L_{loop} as described by (4).

B. Paired versus interdigitated grids

The loop inductance of paired grids is 2.3 times lower than the inductance of the interdigitated grids for the case of a $1\,\mu\text{m} \times 1\,\mu\text{m}$ cross section line and is 1.9 times lower for the case of a $1\,\mu\text{m} \times 3\,\mu\text{m}$ cross section line, as shown in Fig. 6. The reason for this difference is described as follows in terms of the partial inductance. The structure of the forward (and return) current path in a paired grid is identical to the structure of the forward path in an interdigitated grid (only the relative position of the path differs). The partial self inductance L_{pp} is therefore the same in the paired and interdigitated grids; the two corresponding curves completely overlap in Figs. 7 and 8. The values of L_{pp} and L_{gg} for the two types of grids are equal within the accuracy of the analysis. In contrast, due to the immediate proximity of the forward and return current lines in the paired grids, the mutual coupling L_{pg} is lower as compared to the interdigitated grids, as shown in Figs. 7 and 8. Therefore, the difference in the loop inductance between the paired and interdigitated grids is caused by the difference in the mutual inductance.

VII. Dependence of Inductance on Grid Dimensions

Apart from a lower loop inductance, the paired and interdigitated grids have an additional desirable property as compared to non-interdigitated grids. The loop inductance of the paired and interdigitated grids depends inversely linearly with the number of lines as shown in Fig. 6. That is, for example, the inductance of a grid with ten power/ground line pairs is half of the inductance of a grid with five power/ground line pairs, all other factors being the same. For paired grids, this inversely linear dependence is exact (*i.e.*, the deviation is well within the accuracy of the inductance extraction by FastHenry). For interdigitated grids, the inversely linear dependence is exact within the extraction accuracy at high number of power/ground line pairs. As the number of line pairs is reduced to two or three, the accuracy deteriorates to 5% to 8% due to the "fringe" effect, *i.e.*, the electrical environment of the lines at the edges of the grid, where a line has only one neighbor, is significantly different from the environment within the grid, where a line has two neighbors. The fringe effect is insignificant in paired grids because the electrical environment of a line is dominated by the pair neighbor, which is physically much closer as compared to other lines in the paired grid.

As discussed in Section III, the inductance of conductors connected in parallel decreases slower than inversely linearly with the number of conductors if inductive coupling of parallel conductors is present. The inversely linear decrease of inductance with the number of lines may seem to contradict the fact that significant inductive coupling exists among the lines in a grid. Computationally, this effect can be explained by (4). While the partial self inductance of the power and ground paths L_{pp} and L_{gg} indeed decreases slowly with the number of lines so does the power to ground coupling L_{pg}, as shown in Figs. 7 and 8. The nonlinear behavior of L_{pp} and the nonlinear behavior of L_{pg} effectively cancel each other [see (4)], resulting in a loop inductance with an approximately inversely linear dependence on the number of lines.

From a circuit analysis point of view this behavior can be explained as follows. Consider a paired grid. The coupling of a distant line to a power line in any power/ground pair is nearly the same as the coupling of the same distant line to a ground line in the same pair due to the close proximity of the power and ground lines within the same pair. The coupling to the power line counteracts the coupling to the ground line. As a result, the two effects cancel each other. Applying the same argument in the opposite direction, the effect of the coupling of any given line to a power line is canceled by the line coupling to the ground line immediately adjacent to the power line. Similar reasoning is applicable to the interdigitated grids, however, due to the equidistant spacing between the lines, the degree of coupling cancellation is lower for the lines at the periphery of the grid. The lower degree of cancellation is the cause of the aforementioned "fringe" effect.

The grid loop inductance is also found to increase linearly with grid length. The linear dependence of inductance on length can be explained similarly to the preceding discussion describing the dependence of the inductance on the number of lines.

The linear dependence of inductance on the grid length and width (*i.e.*, the number of lines) has a convenient implication. The inductance of a large paired or interdigitated grid can be extrapolated with good accuracy from the inductance of a grid consisting of only several power/ground pairs. For an accurate extrapolation of the interdigitated grids, the line width and pitch of the original and extrapolated grids should be main-

tained the same. In the case of paired grids, only the physical spacing between the adjacent power and ground lines should be maintained the same, as the effective inductive coupling between power/ground pairs is negligible. Alternatively, in paired grids the effective width of the current loop is primarily determined by the power to ground line separation within a pair. The spatial separation between pairs has (almost) no effect on the grid loop inductance.

VIII. Dependence of inductance of power distribution grids on frequency

As mentioned in Section II, the circuit inductance decreases with frequency due to the skin effect, proximity effect, and the redistribution of the return current. The decrease in loop inductance for the three types of grid structures with a $1\,\mu\text{m} \times 1\,\mu\text{m}$ line cross section operating at 100 GHz as compared to a frequency of 1 GHz is plotted in Fig. 9. Note that, as

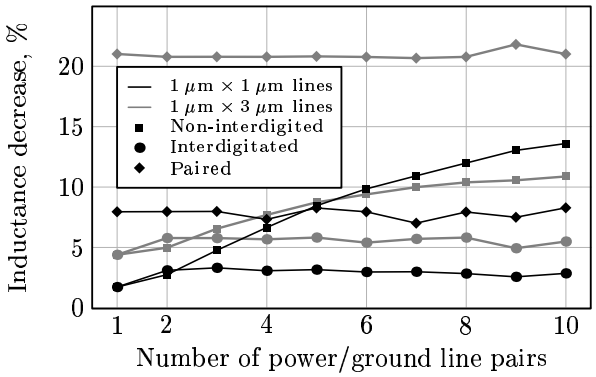

Fig. 9. Decrease in loop inductance with the change in frequency from 1 GHz to 100 GHz versus the number of P/G line pairs in the grid. The decrease is expressed as a per cent of the inductance at 1 GHz. The line cross section is $1\,\mu\text{m} \times 1\,\mu\text{m}$.

shown in Fig. 9, the inductance decreases with frequency. The difference between the high and low frequency loop inductance is less than 6% for paired grids with a $1\,\mu\text{m} \times 1\,\mu\text{m}$ cross section and for interdigitated grids with both $1\,\mu\text{m} \times 1\,\mu\text{m}$ and $1\,\mu\text{m} \times 3\,\mu\text{m}$ cross sections. The change in inductance of this magnitude is insignificant for most digital applications since the circuit propagation delay is fairly insensitive to inductance as demonstrated in [9].

This relative independence of inductance with frequency is explained in the following way. In regular power grids with interdigitated power and ground lines (such as the interdigitated and paired grid structures discussed here), each line has the same resistance and inductance per length, and almost the same coupling to the rest of the grid (as discussed above in relation to the dependence of inductance on the number of lines). As a result, the distribution of current among the wires at low frequencies (where the current flows through the path of lowest resistance) practically coincides with the current distribution at high frequencies (where the current flows through the path of lowest inductance). That is, the wire resistance has a negligible effect on the distribution of current in the grid. Consequently, the decrease in inductance at high frequencies is caused by skin and proximity effects which only depend on the wire size, spacing, and material resistivity. Such a decrease, as shown in Fig. 9, is typically insignificant. The grid inductance varies little with frequency unless several wide wires are placed in close proximity and carry very high frequency signals. This behavior is illustrated by the example of paired grids with wide $1\,\mu\text{m} \times 3\,\mu\text{m}$ lines. In this case, the decrease in inductance is greater, approximately 22%, due to the proximity effect in adjacent wide lines.

In non-interdigitated grids, the decrease in loop inductance is limited to 11%, but increases with the number of lines in the grid. As the number of lines increases, the current distribution at low frequencies, uniform among the wires, changes at high frequencies, where the current crowds toward the central wires which provide the lowest inductance path.

IX. Conclusions

The inductive characteristics of power distribution grids are investigated in this paper. Paired grids are shown to have the lowest inductance as compared to interdigitated and non-interdigitated grids. The grid inductance is moderately dependent on the width of the power and ground lines. The inductance of the grids with interdigitated power and ground lines is shown to vary linearly with grid length and to vary inversely linearly with the number of power/ground lines. The inductance of the grids with interdigitated power and ground lines decreases relatively little with frequency; the decrease in inductance from 1 GHz to 100 GHz is less than 10% for most practical geometries. These properties facilitate the efficient estimation of the inductive characteristics of power distribution grids of various dimensions.

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