Pessimism Reduction In Static Timing Analysis Using Interdependent Setup and Hold Times

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***Abstract*— A methodology is proposed for interdependent *setup time* and *hold time* characterization of sequential circuits. Integrating the methodology into an industrial sign-off static timing analysis tool is described. The proposed methodology prevents optimism and reduces unnecessary pessimism, both of which exist due to independent characterization. Furthermore, the tradeoff between interdependent setup and hold times is exploited to significantly reduce slack violations. These benefits are validated using industrial circuits and tools.**

I. INTRODUCTION

The accuracy of the data in cell timing libraries is an important factor in determining maximum clock frequencies. Specifically, the setup and hold time constraints of sequential circuits are used to verify the timing of a synchronous circuit. If characterization of the timing constraints is inaccurate, the results can be either highly optimistic or pessimistic. The optimistic case can cause a fabricated circuit to fail whereas the pessimistic case can unnecessarily degrade circuit performance, making it more difficult to achieve a target frequency.

Although the importance of library data accuracy is well known [1], [2], [3], current constraint characterization practices suffer from both optimism and unnecessary pessimism. These problems are mostly due to the *independent* characterization of constraints; however, these constraints are *interdependent*. The constraints should therefore be characterized interdependently to improve accuracy.

When these constraints are characterized interdependently, multiple constraint pairs, which are interchangeable, are obtained. These pairs can be utilized to reduce violations in static timing analysis (STA). These multiple valid pairs, however, are currently not exploited in STA.

In this paper, a comprehensive methodology and algorithm to interdependently characterize setup and hold times and exploit the resulting multiple pairs in STA are proposed. The methodology is validated using high performance industrial circuits and an industrial sign-off STA tool. In particular, STA results demonstrate up to a 50% reduction in the number of constraint violations as well as up to a 50% reduction in the worst negative slack.

The rest of the paper is organized as follows. Relevant background material is provided in Section II. In Section III, current approaches are described, the concept of interdependency is presented, and the problem is formally defined. The proposed characterization methodology and algorithm are explained in Section IV. STA results are presented in Section V and the paper is concluded in Section VI.

II. PRELIMINARIES

Some basic background information about sequential circuits is introduced in Section II-A. The fundamentals of STA and setup and hold times are reviewed in Sections II-B and II-C, respectively.

A. Sequential Circuits

A simplified sequential circuit is illustrated in Fig. 1(a), and consists of a data input D, a clock input CLK, and an output Q. Examples of sequential circuits are registers and latches.

A sequential circuit has two timing arcs: one arc from the CLK input to the D input to annotate the setup and hold times and another arc from the CLK input to the Q output to annotate the CLK-to-Q delay. In STA, D and CLK are referred to, respectively, as an endpoint and a startpoint. This implication is because a timing path starts at CLK and ends at D.

B. Static Timing Analysis

A basic STA tool reads in a circuit netlist, a cell library, and a clock period T. The tool reports whether the circuit performs as intended. This analysis is accomplished by computing the worst setup slack (SS) and worst hold slack (HS) at every endpoint. Referring to Fig. 1(b), these slacks are computed as follows,

$$SS = \min(tC + T) - \max(tL + tD + tS), \tag{1}$$

$$HS = \min(tL + tD) - \max(tC + tH), \tag{2}$$

where tC, tL, tD, tS, and tH refer, respectively, to the capture path delay, launch path delay, data path delay, setup time, and hold time, as illustrated in Fig. 1(b).

If a slack is negative or nonnegative, it is said to be *violated* or *satisfied*, respectively. If a setup slack is violated, the circuit can operate correctly by slowing the circuit down, *i.e.*, by increasing T. If a hold slack is violated, the circuit will not function correctly.

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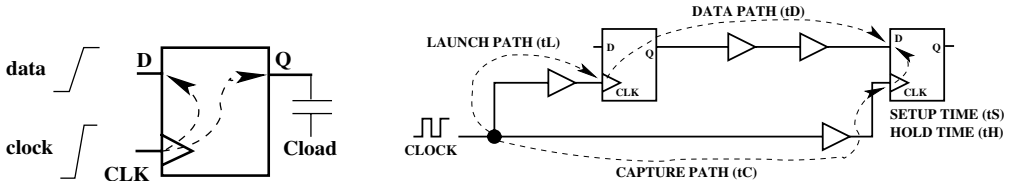


(a) (b)

Fig. 1. Register with a synchronous circuit: (a) simplified register, (b) conceptual computation of setup and hold slack in STA on an example synchronous data path.

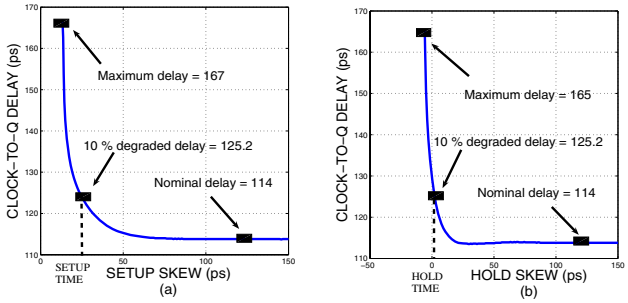


Fig. 2. Independent constraint characterization for sequential circuits: (a) setup skew vs. CLK-to-Q delay for setup time characterization, (b) hold skew vs. CLK-to-Q delay for hold time characterization.

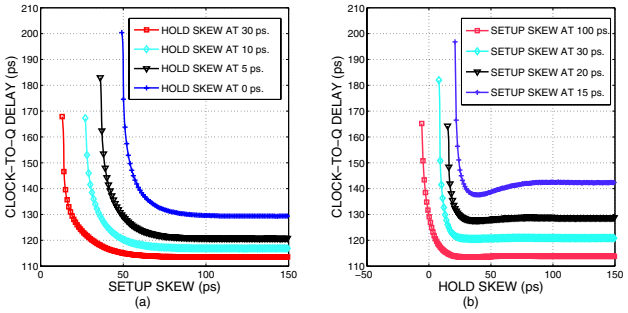


Fig. 3. Constraint characterization for sequential circuits at different counterpart skews: (a) setup skew vs. CLK-to-Q delay at different hold skews, (b) hold skew vs. CLK-to-Q delay at different setup skews.

C. Setup / Hold Times and Skews

Since nonnegative slacks are required not to have violations, (1) and (2) can also be written, respectively, as follows:

$$\min(tC+T)-\max(tL+tD)\geq\max(tS), \tag{3}$$

$$\min(tL+tD)-\max(tC)\geq\max(tH). \tag{4}$$

These inequalities require a difference, called a *skew*, to be larger than or equal to a number, called a *constraint*. These inequalities, therefore, can be rewritten as

$$\min(\text{setup skew})\geq\max(\text{setup time}), \tag{5}$$

$$\min(\text{hold skew})\geq\max(\text{hold time}). \tag{6}$$

Note that the setup and hold skews refer to the time difference between the data and clock signals whereas the setup and hold times refer to the minimum required time difference such that the data is reliably captured and stored.

III. PROBLEM FORMULATION

Current setup and hold time characterization approaches are described in Section III-A. The concept of interdependency and related issues are explained in Section III-B.

A. Existing Characterization Approaches

A common approach to characterize setup time is to examine the setup skew versus CLK-to-Q delay relationship [4], [5] at a fixed hold skew, which is called here the *counterpart skew*. The process is similar for hold time. These approaches are shown in Fig. 2. According to [4], three regions can be determined for both plots: stable, metastable, and failure regions. The stable region is defined as the region in which the CLK-to-Q delay is independent of the setup or hold skew. As the skew decreases, the CLK-to-Q delay starts to rise in an exponential fashion [6]. If the skew is excessively small, the register fails to latch the data. This region is called the failure region. The region between the stable and failure regions is referred to as the metastable region.

The setup and hold times cannot fall in the failure region since the register is unable to latch the data in that region. The setup (hold) time is usually set to the setup (hold) skew where the stable region crosses over into the metastable region. There are different approaches to identify this *crossover point* [4]. In some approaches, the crossover point is the time where a certain amount of degradation in the CLK-to-Q delay occurs. For example, a 10% degradation is assumed in Fig. 2. In some other approaches, the crossover point is the time where the sum of the setup skew and CLK-to-Q delay is minimized.

B. Interdependency Between Setup and Hold Times

The setup and hold times are not independent [7]; rather, these constraints are a function of the counterpart skews (hold skew for setup time and setup skew for hold time). These dependences are shown in Fig. 3. Note that the setup time decreases as the hold skew increases and the hold time decreases as the setup skew increases. Thus, the smallest setup and hold times occur when the counterpart skews are the largest.

The interdependence between the setup and hold times can intuitively be explained as follows. Since the CLK-to-Q delay is dependent of both the setup and hold skews, it can be allocated to either the setup or hold side. For example, if the setup skew is small, this skew dominates the degradation in the CLK-to-Q delay; hence, the hold skew must be relatively large. The same reasoning applies to the hold side.

Existing characterization approaches typically ignore the interdependence of the setup and hold times. This strategy leads to two main issues:

Issue 1. If the counterpart skews are assumed to be unnecessarily large, the resulting setup and hold times are optimistic. If, however, the data waveform does not satisfy large counterpart skews, optimistic setup and hold times cause the circuit to fail despite not violating any of the individual constraints. Alternatively, if the counterpart skews are assumed to be unnecessarily small, the resulting setup and hold times are pessimistic. Both cases should be avoided as the optimistic case can cause circuit failures after fabrication whereas the pessimistic case can cause false violations during STA.

Issue 2. If this dependence is considered but not exploited, an opportunity to reduce the number of timing violations and improve the slack is missed.

In [7], the first issue is resolved by considering this interdependence. However, only one interdependent pair of setup and hold times is considered; therefore, the interdependence is not exploited to improve slacks. In this paper, a methodology is proposed that solves both issues.

IV. PROPOSED METHODOLOGY

The proposed methodology is described in six steps. Each step is explained in a separate subsection.

- **Step 1.** For each data and clock slew combination, the circuit is simulated to obtain CLK-to-Q delay surfaces, each a function of *independently varying* setup and hold skews.
- **Step 2.** A contour, set to a constant CLK-to-Q delay, is obtained for each surface. Each point on the contour represents an *interdependent* pair of setup and hold times.
- **Step 3.** Critical pairs are identified on each contour. A cell library is created for each of these pairs.
- **Step 4.** The critical pairs are connected based on a piecewise linear (PWL) curve. This curve approximates the contour with slightly pessimistic setup and hold times.
- **Step 5.** A library is used for STA. If violations occur, the existence of other libraries and the PWL curve is utilized to resolve the violations.

Limitations of this methodology are discussed in the last subsection.

A. CLK-to-Q Delay Surface

For a given data and clock slew combination, the CLK-to-Q delay is a function of both the setup skew and hold skew. A typical delay surface is shown in Fig. 4(a). Note that in this figure, the CLK-to-Q delay increases when the skews either independently or simultaneously decrease. The multiple peaks on the surface mark the boundary beyond which the skews are excessively small and the register can no longer latch the data.

A delay surface is generated by independently varying the setup and hold skews. Independent variation allows the generation of the *actual* delay surface and simplifies the library characterization process at the expense of additional circuit simulations.

Every point on the CLK-to-Q delay surface corresponds to a skew pair, denoted as (setup skew, hold skew). If a particular pair on this surface is identified as the final (setup time, hold time) pair, Issue 1 in Section III-B is resolved because the setup and hold times at this point are now interdependent.

Different approaches exist to select a final pair on the surface depending upon the definition of the crossover point [7]. Irrespective of the approach used, it is highly likely that there will be multiple final pairs that satisfy this definition.

B. Constant Delay Contour

A definition of a common crossover point is a specific per cent degradation in the CLK-to-Q delay. Once the CLK-to-Q delay surface in three dimensions is obtained, all of the final pairs can be extracted from the constant delay contour as a per cent of the crossover point.

The contour obtained at 10% degraded CLK-to-Q delay is depicted in Fig. 4(b). Each (setup time, hold time) pair on this contour is interdependent and valid. Further, any pair in region 1 is also valid with additional pessimism whereas any pair in region 2 is invalid, as the pairs in this region are optimistic.

Two important conclusions can be drawn from this contour:

1) Rather than single and independent setup and hold times, there are multiple and interdependent (setup time, hold time) pairs. Any pair can be chosen depending upon the potential to remove timing violations.

2) As indicated in Fig. 4(b), the setup and hold times are inversely proportional. Hence, a small setup time can be obtained at the expense of a large hold time (or vice versa).

C. Critical Pairs on Contour

The following pairs on the contour are distinguished because these pairs are appropriate candidates to include in a cell library. Note in Fig. 4(b), the setup times and hold times are on the abscissa and ordinate, respectively.

Definition 1: P is defined as the set of all (s,h) pairs on the contour where s is the setup time and h is the hold time.

Definition 2: S and H are defined as the set of all setup times s and hold times h on the contour, respectively.

Definition 3: The *minimum setup pair MSP* is defined as the pair (s,h) in P such that s is minimum in S. More formally,

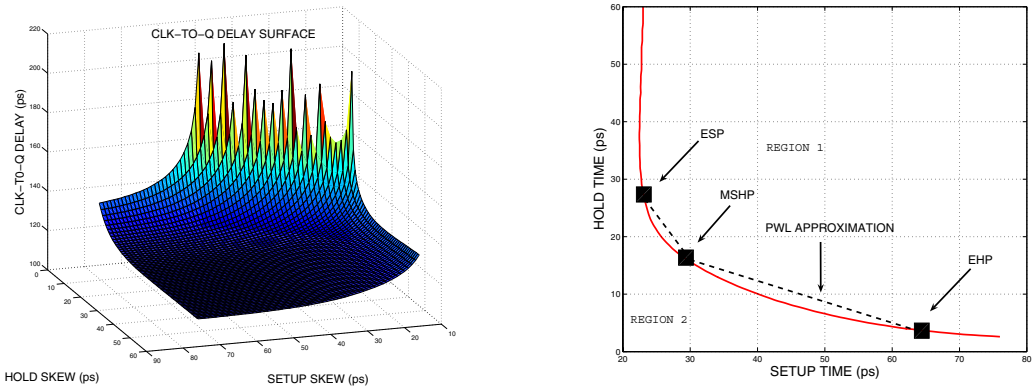
$$MSP = (s,h) \in P \text{ such that } s = \min_{\forall s \in S}(s). \quad (7)$$

Definition 4: The *minimum hold pair MHP* is defined as the pair (s,h) in P such that h is minimum in H. More formally,

$$MHP = (s,h) \in P \text{ such that } h = \min_{\forall h \in H}(h). \quad (8)$$

Definition 5: The *effective setup pair ESP* is defined as

$$ESP = (s,h) \in P \text{ such that } s = s[MSP] + \varepsilon_s * |s[MSP]|, \quad (9)$$



(a) (b)

Fig. 4. Interdependent constraint characterization: (a) CLK-to-Q delay surface as a function of independently varying setup skew and hold skew, (b) The contour at 10% degraded CLK-to-Q delay. The contour includes the critical pairs as well as a piecewise linear approximation. Regions 1 and 2 are the pessimistic and optimistic regions, respectively.

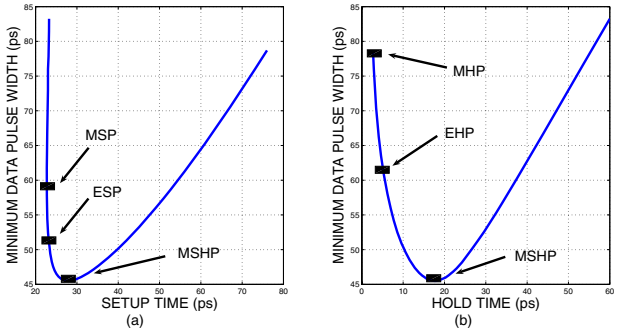


Fig. 5. The relationship between constraints and the minimum pulse width: (a) setup skew vs. minimum pulse width, (b) hold skew vs. minimum pulse width.

where $\varepsilon_s \geq 0$ is a small constant and s[MSP] is the setup time of MSP.

Definition 6: The *effective hold pair EHP* is defined as

$$EHP = (s,h) \in P \text{ such that } h = h[MHP] + \varepsilon_h * |h[MHP]|, \quad (10)$$

where $\varepsilon_h \geq 0$ is a small constant and h[MHP] is the hold time of MHP.

Definition 7: The *minimum setup-hold pair MSHP* is defined as

$$MSHP = (s,h) \in P \text{ such that } s+h = \min\{\sum_{\forall (s,h) \in P} (s+h)\}. \quad (11)$$

A distinction is made between the *MSP (minimum setup pair)* and the *ESP (effective setup pair)* because *MSP* requires an impractically large hold time. That is, the setup time must be increased by $100\varepsilon_s\%$ in order to reduce the hold time to an acceptable level.

The distinction between the minimum and effective pairs can be illustrated by considering the minimum pulse width of the data signal. The minimum pulse width of the data signal is determined by summing the setup and hold times.

The variation of the minimum pulse width with respect to the setup and hold times is shown in Fig. 5. Note that if minimum constraints are used rather than effective constraints, the minimum pulse width increases significantly. At zero ε_s and ε_h, the effective constraints are equal to the minimum constraints.

D. Piecewise Linear (PWL) Approximation of Contour

In order to fully exploit this interdependency, the STA tool should use more than one (setup time, hold time) pair by switching between multiple pairs such that the violations can be removed or improved. Since cell libraries require time and memory to generate and store, these libraries cannot be generated at every point on the contour. An appropriate strategy is to generate one cell library per critical pair. The resulting libraries, however, can be insufficient to remove all violations. An improvement is to approximate the contour using a PWL curve by means of critical pairs. The section of the contour between *ESP* and *EHP* is always convex [8]. As such, the PWL curve remains in region 1, and the setup and hold time pairs cannot be optimistic. If, however, the contour section between *ESP* and *EHP* is not convex, a smaller but convex section needs to be determined to enable a PWL approximation.

The linear representation of the contour at three different data and clock slew pairs is shown in Fig. 6. Each linear curve is obtained using *ESP* and *EHP* on the contour. Note that the number of critical pairs used in the PWL curve represents a tradeoff between accuracy and complexity.

E. Integration of Methodology into an STA Tool

If characterization is achieved in an interdependent way, and at least two pairs are provided to the STA tool, an efficient

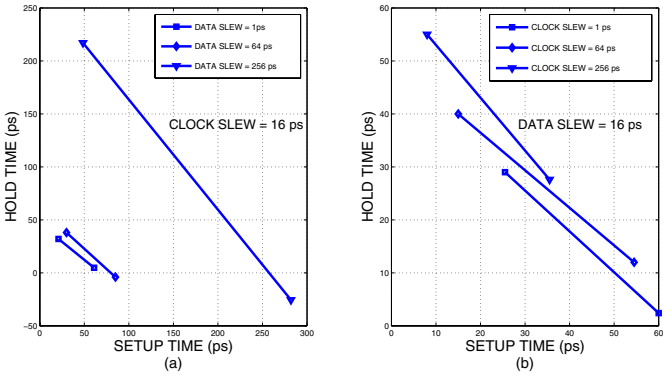


Fig. 6. Linear representations using two pairs, ESP and EHP: (a) at different data slews, (b) at different clock slews.

FIND-BEST-PAIR(P)
1. Select a valid pair (s_0, h_0) from P
2. Calculate hold slack = HS (as in § II-B)
3. Calculate setup slack = SS (as in § II-B)
4. **if** $(HS \geq 0$ and $SS \geq 0)$ **then**
5. **return** $< (s_0, h_0)$, found $>$
6. **else**
7. Calculate max. required setup time = $RST = s_0 + SS$
8. Calculate max. required hold time = $RHT = h_0 + HS$
9. **for** each $(s,h) \in P$ **do**
10. **if** $(s \leq RST$ and $h \leq RHT)$ **then**
11. **return** $< (s,h)$, found $>$
12. **return** $< (RST, RHT)$, not found $>$

Fig. 7. Pseudo-code to determine the (setup,hold) pair that removes the violation over the PWL approximation of the contour curve.

algorithm can be used to fully exploit this interdependency. The pseudo-code of a proposed algorithm FIND-BEST-PAIR is provided in Fig. 7.

FIND-BEST-PAIR reads in the PWL representation P of the contour as an input. At line 1, a (setup time, hold time) pair is selected from the input. This pair can be any of the critical pairs on P, but it is suggested here to use *EHP*, as hold times are typically more critical. The setup and hold slacks are determined as described in Section II-B. Both slacks are checked for violations. If both are nonnegative, the algorithm terminates, returning the pair as the "best" pair. If one or both of the slacks are negative, these slacks are used to compute the maximum setup and hold times required to remove the violations. The loop at line 9 determines if such a pair actually exists in P. If so, the pair is returned as the best pair. If no such pair exists, the required setup and hold times are returned with a warning that no solution is possible. The required setup and hold times can be used to search for a pair that minimizes the violations. Note that the search at line 9 can be optimized using techniques from computational geometry to determine the relative location of a point with respect to a line [9].

F. Limitations

The primary limitations of the proposed methodology are twofold: (1) the constraint characterization time increases for sequential circuits, and (2) the STA runtime increases. The first limitation is due to the generation of the delay surfaces, and the second limitation is due to the use of multiple constraints during STA.

These limitations can be mitigated as follows: (1) a single characterization run can generate all of the constraints at each critical pair; (2) the number of independent skews for the delay surfaces can be reduced, *i.e.*, those skews pairs that do not change the delay surface can be eliminated; and (3) the number of critical pairs can be reduced to two (at the expense of some pessimism).

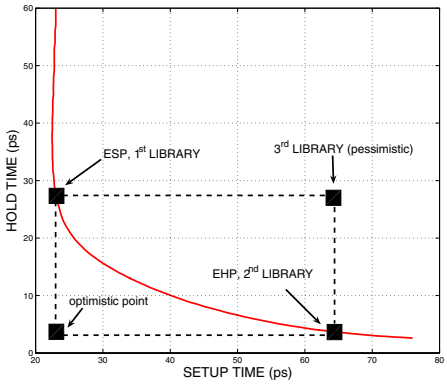


Fig. 8. Constant delay contour curve illustrating the characterization points of the three prototype libraries.

V. STA RESULTS

A 90 nm library is used as a template to generate three new cell libraries: library 1, library 2, and library 3. The sequential circuits of each library are characterized using H-SPICE with BSIM4/BSIM3 models.

The library characterization points for these three libraries are illustrated in Fig. 8. Both library 1 and 2 are on the contour: library 1 is at the *ESP (effective setup pair)* and library 2 is at the *EHP (effective hold pair)*. Library 3 is not on the contour; this last library uses setup times from *EHP* and hold times from *ESP*, and as such, is an example of independent and pessimistic characterization. The optimistic point that results from using relatively large counterpart skews is also shown in the figure.

An industrial sign-off STA tool is used to evaluate each prototype library on two circuits: circuit A and circuit B. Both circuits are networking cores with nearly 20K cells. The clock frequencies of circuit A and circuit B are set to 666 MHz and 400 MHz, respectively.

From STA, the smallest negative slack value, referred to as the worst negative slack (WNS), and the number of violations are obtained for each of the endpoints. The STA results are listed in Table I. Each row corresponds to one simulation with one circuit and one library.

WNS and the number of violations from library 3 are taken as a baseline, and the absolute and relative improvements are

TABLE I

ABSOLUTE (ABS) AND RELATIVE (REL) IMPROVEMENTS OF TWO CIRCUITS WITH RESPECT TO LIBRARY 3. WNS IS THE WORST NEGATIVE SLACK. ΔWNS IS THE INCREASE IN WNS, AND ΔN IS THE DECREASE IN THE NUMBER OF VIOLATIONS.

Circuit	Period (ps)	Library	WNS (ps)		Number of violations		ΔWNS (ps): abs (rel)		ΔN: abs (rel)	
			setup	hold	setup	hold	setup	hold	setup	hold
Circuit A	1500	3	-1003	-488	361	1868	-	-	-	-
		1	-790	-488	285	1868	213 (21.2%)	-	76 (21.0%)	-
		2	-1003	-307	361	1684	-	181 (37.1%)	-	184 (9.9%)
Circuit B	2500	3	-766	-26	1977	1	-	-	-	-
		1	-397	-26	924	1	369 (48.2%)	-	1053 (53.3%)	-
		2	-766	0	1977	0	-	26 (100.0%)	-	1 (100.0%)

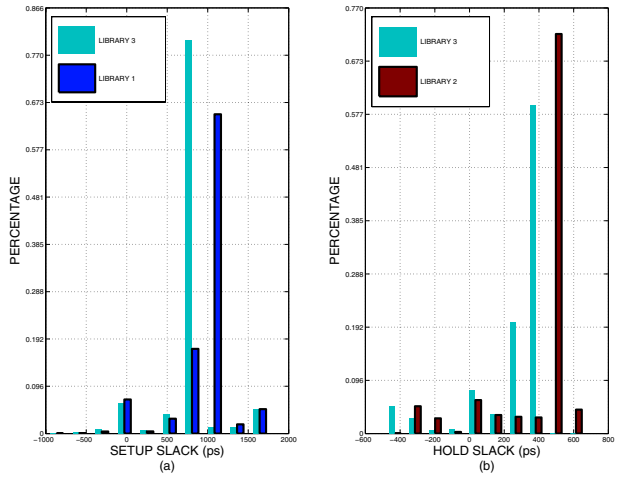


Fig. 9. Slack histograms for circuit A: (a) setup slack histograms of library 3 and library 1, (b) hold slack histograms of library 3 and library 2.

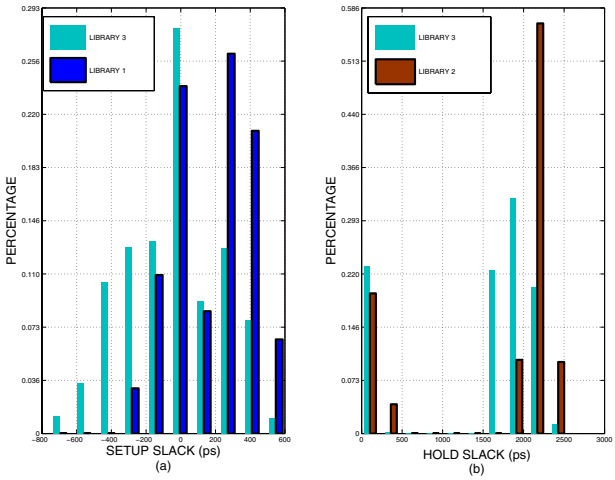


Fig. 10. Slack histograms for circuit B: (a) setup slack histograms of library 3 and library 1, (b) hold slack histograms of library 3 and library 2.

computed in WNS and the number of violations with respect to library 3. Improvements in WNS and the number of violations correspond, respectively, to an increase in WNS and a decrease in the number of violations.

As listed in Table I, the improvement in setup WNS is 369 ps (or 48.2%). This improvement corresponds to nearly 14% of the clock period. The improvement in hold WNS is 181 ps (or 37.1%). In terms of the number of violations, the improvement in the setup case is 53.3% and in the hold case is 9.9%. Note that for hold time improvements, the case where the only hold time violation is removed is ignored.

These improvements can also be illustrated by means of slack histograms over all the endpoints rather than a single number like WNS. Histograms for the two circuits are shown in Figs. 9 and 10. For both histograms, there is a shift towards the positive side, indicating improvements in almost all of the slack values. The baseline is the slacks from library 3.

VI. CONCLUSIONS

An interdependent characterization methodology is presented for setup and hold times of sequential circuits. The interdependency removes optimism. The existence of multiple (setup time, hold time) pairs can be exploited to reduce unnecessary pessimism in STA. The methodology is validated using industrial circuits and tools, exhibiting significant improvement in the worst negative slack as well as the number of slack violations.

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