Dominant Substrate Noise Coupling Mechanism for Multiple Switching Gates

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***Abstract*— The dominant substrate noise coupling mechanism is determined for multiple switching gates based on a physically intuitive model. The model exhibits reasonable accuracy as compared to SPICE. The regions where ground coupling and source/drain coupling dominate are described based on this model. The impact of multiple parameters such as the rise time, number of switching gates, decoupling capacitance, and parasitic inductance on the dominant noise coupling mechanism is investigated. The dominance of ground coupling in large scale circuits, as generally assumed, is shown to be invalid if sufficient decoupling capacitance is used or the circuit exhibits a low parasitic inductance such as a flip-chip package. The efficacy of several noise reduction techniques is discussed based on the application of the dominant noise analysis model.**

I. INTRODUCTION

Substrate noise coupling is a primary concern in mixed-signal systems where noise sensitive circuits coexist with noise generating aggressor circuits on the same monolithic substrate. The noise injected by the baseband digital circuit propagates through the substrate, either degrading the performance of a sensitive circuit [1], [2], or causing a circuit to fail [3]. The reduced physical distance between the noise generating and victim blocks exacerbates this issue. Better understanding of the dominant noise coupling mechanism is therefore necessary to apply efficient noise reduction techniques.

Noise is injected into the substrate through three primary mechanisms [4]: (1) coupling from the noisy power and ground networks of the digital circuits, (2) coupling from the source/drain junction capacitances during switching, and (3) impact ionization, which is negligible as compared to the first two mechanisms [4]. It is usually assumed in large scale circuits that power/ground coupling dominates source/drain coupling [5], [6], [7]. The validity of this assumption, however, depends upon several circuit parameters, such as the number of simultaneously switching gates, rise time, decoupling capacitance, and parasitic inductance of the power/ground rails.

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The existing work on dominant noise analysis fails to collectively model all of these parameters in a sufficiently accurate manner. Different noise injection mechanisms are investigated and quantified in [4], but the primary emphasis is on the generation rather than the propagation of the noise. In [6], the impact of technology scaling on several noise generation mechanisms is analytically examined to determine the dominant noise mechanism. For multiple switching gates, the substrate resistance between the source and victim is linearly scaled to quantify the ground coupling. This procedure, however, produces highly pessimistic results for ground coupling since an additional contact to the substrate does not linearly decrease the substrate resistance due to the mesh structure of the substrate.

A simple, yet intuitive subtrate coupling model is described in this paper for multiple switching gates to determine the dominant noise coupling mechanism. The model considers each of the parameters and is shown to be sufficiently accurate. The impact of various parameters are evaluated, determining the boundary conditions for the dominance of ground coupling and source/drain junction coupling.

The rest of the paper is organized as follows. The substrate coupling model and the validation of this model are described in Section II. The dominant noise coupling mechanism is investigated in Section III. Noise reduction techniques based on this dominant noise analysis are discussed in Section IV, and the paper is concluded in Section V.

II. SUBSTRATE COUPLING MODEL

The primary substrate noise generation mechanisms are coupling from the noisy power/ground network of the digital circuit and source/drain coupling from the junctions of the devices during switching. Resistive ground coupling is assumed to be dominant over capacitive power coupling due to the n-well isolation. Ground and source/drain coupling are therefore considered to be the two primary noise generation mechanisms. The dominant noise generation mechanism is evaluated as a function of multiple parameters. Substrate coupling models for a single switching gate and multiple switching gates, and validation of the model are described, respectively, in Sections II-A, II-B, and II-C.

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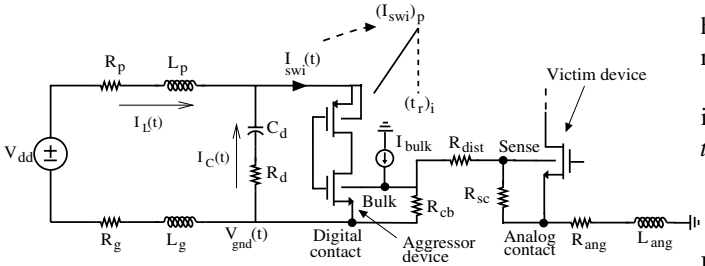

Fig. 1. Equivalent model to estimate ground coupling and source/drain junction coupling for a single switching gate. Ground noise $V_{gnd}(t)$ couples into the substrate through the digital contact. Source/drain junction coupling is represented as a current source I_{bulk} at the bulk of the aggressor device. Noise is observed at the sense node of the victim device.

A. Substrate Coupling for a Single Switching Gate

Noise on the ground distribution network resistively couples into the substrate through the substrate contacts. The ground noise is quantified, assuming that the substrate network does not affect the ground noise due to the high impedance of the substrate as compared to the ground network. In Fig. 1, L_p, R_p, and L_g, R_g represent, respectively, the power and ground network parasitic impedances. C_d is the decoupling capacitor and R_d is the effective series resistance of the capacitor. The load circuit is represented by a current source with a rise time $(t_r)_i$ and a peak current $(I_{swi})_p$. The substrate resistance between the contact and bulk of the device is represented by R_{cb}. R_{dist} represents the equivalent substrate resistance between the bulk and the sense node of the sensitive analog circuit. R_{sc} represents the equivalent substrate resistance between the sense node and the analog contact. R_{ang} and L_{ang} are the parasitic impedance of the analog ground network.

Assuming $R_p = R_g$, $L_p = L_g$, and a ramp function for the noise $V_{gnd}(t) = [(V_{gnd})_p/(t_r)_v]t$, where $(t_r)_v$ is the rise time and $(V_{gnd})_p$ is the peak ground noise voltage, the current provided by the decoupling capacitance $I_C(t)$ and the current flowing through the parasitic inductance $I_L(t)$ from the power supply can be expressed, respectively, as

$$I_C(t) = G_C(t)(V_{gnd})_p, \tag{1}$$

$$I_L(t) = G_L(t)(V_{gnd})_p. \tag{2}$$

$G_C(t)$, the conductance of the capacitance path, and $G_L(t)$, the conductance of the inductance path, are given, respectively, by

$$G_C(t) = \frac{2C_d}{(t_r)_v}(1 - e^{-t/(R_d C_d)}), \tag{3}$$

$$G_L(t) = \frac{t}{(t_r)_v R_g} - \frac{L_g}{(t_r)_v R_g^2}(1 - e^{-t/\frac{L_g}{R_g}}). \tag{4}$$

Note that these conductances are both a function of the rise time $(t_r)_v$. Specifically, as the rise time becomes smaller, $G_C(t)$ increases and $G_L(t)$ decreases. The capacitive current, therefore, increases with decreasing rise time. Alternatively, the inductive current increases with longer rise times. Intuitively, a smaller rise time corresponds to a higher frequency where the impedance of the capacitance is smaller and the inductance is higher. The capacitance is, therefore, more effective at smaller rise times and becomes less effective as the rise time increases.

Assuming the peak noise occurs when the switching current is maximum, *e.g.*, $(t_r)_v = (t_r)_i = t_r$, the peak ground noise at $t = t_r$ can be expressed as

$$\frac{1}{(V_{gnd})_p} = \frac{G_C(t_r)}{(I_{swi})_p} + \frac{G_L(t_r)}{(I_{swi})_p}. \tag{5}$$

Replacing (3) and (4) in (5) produces

$$(V_{gnd})_p = \frac{(I_{swi})_p R_g^2 t_r}{2C_d R_g^2(1 - e^{-t_r/(R_d C_d)}) - L_g(1 - e^{-t_r/\frac{L_g}{R_g}}) + R_g t_r}. \tag{6}$$

If the circuit is underdamped, *e.g.*, the damping factor is smaller than one, oscillations occur due to a parallel combination of the parasitic inductance and the decoupling capacitor. In this case, the peak-to-peak ground noise voltage is

$$(V_{gnd})_{pp} = (V_{gnd})_p[1 + e^{-\pi\zeta/\sqrt{1-\zeta^2}}], \tag{7}$$

where $\zeta = [(2R_g + R_d)/2]\sqrt{C_d/2L_g}$ is the damping factor. The substrate noise at the sense node due to ground coupling can be approximated as

$$(V_{s-gnd})_{pp} \approx \frac{(V_{gnd})_{pp}}{R_{cb} + R_{dist} + R_{sc}}(R_{ang} + R_{sc} + \frac{L_{ang}}{t_r}). \tag{8}$$

Noise couples into the substrate through the source/drain junction capacitance of the devices during switching. This noise source is modeled as a current source at the bulk of a device with a peak current of $(I_{bulk})_p$ and a rise time of t_r (which is assumed to be equal to the rise time of the switching current). The substrate noise at the sense node due to source/drain junction coupling can be approximated as

$$(V_{s-bulk})_p \approx (I_{bulk})_p \frac{R_{cb}}{R_{cb} + R_{dist} + R_{sc}} . (R_{ang} + R_{sc} + \frac{L_{ang}}{t_r}). \tag{9}$$

The total noise at the sense node is determined by the summation of (8) and (9),

$$(V_{s-total})_{pp} \approx (V_{s-gnd})_{pp} + (V_{s-bulk})_p. \tag{10}$$

B. Substrate Coupling for Multiple Switching Gates

The model introduced in the previous section for a single switching gate is extended to analyze the effect of simultaneously switching gates on the substrate noise characteristics. Each macromodel for a switching gate consists of two current sources, I_{swi-g} and I_{bulk-g}, to represent the switching and bulk currents, respectively, and a substrate resistance R_{cb} between the contact and bulk if the gate has a substrate contact. The channel capacitance and resistance of the switching gates are neglected in the noise analysis, as described in [8].

These gates are connected as shown in Fig. 2 to obtain a substrate coupling model for multiple gates. For a given number of switching gates n, the L and M gates are placed in the horizontal and vertical directions, respectively, such that $L \times M = n$. The resulting rectangle is as close as possible to a square in terms of the physical layout of the aggressor

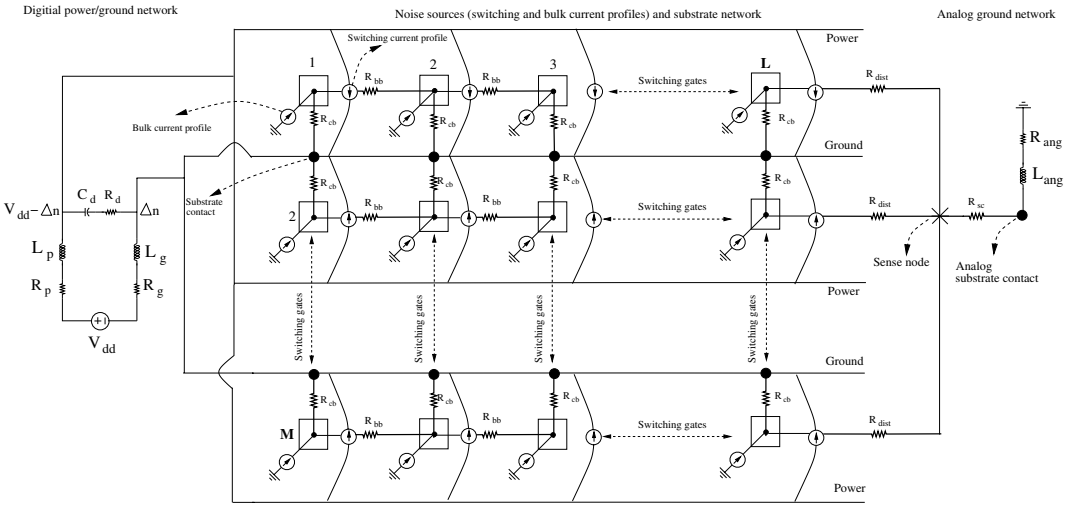

Fig. 2. Equivalent circuit model to estimate substrate noise for multiple switching gates. Each switching gate consists of two current sources, I_{swi-g} and I_{bulk-g}, and a substrate resistance R_{cb} between the substrate contact and bulk. The bulk node of each gate located along the horizontal direction are connected through a substrate resistance R_{bb}. The bulk of the gates located along the vertical direction which share the same local ground line are vertically connected through the resistance 2 x R_{cb}. The physical distance between the aggressor digital circuits and sensitive circuit is represented by R_{dist}. R_{sc} is the equivalent substrate resistance between the sense node and the analog contact.

circuit. The bulk node of each gate located along the horizontal direction is connected through a substrate resistance R_{bb}. The bulk of the gates located along the vertical direction which share the same local ground line is vertically connected through the resistance, 2 *x* R_{cb}. The parasitic power/ground network impedance between the gates is neglected, assuming that all of the gates have the same power/ground network impedance and decoupling capacitance. R_{dist} represents the substrate resistance between the aggressive digital and sensitive analog circuits. R_{sc} is the equivalent substrate resistance between the sense node and the analog contact. L_{ang} and R_{ang} represent the ground network *LR* impedance of the analog circuit.

The ground noise $(V_{gnd})_{pp}$ at each substrate contact location is determined from (8) where the total peak current scales to $n(I_{swi-g})_p$. Note that the switching gates are assumed in this analysis to be identical. The peak-to-peak substrate noise at the sense node $(V_{sense})_{pp}$ is the summation of the noise due to each contact and bulk current source,

$$(V_{sense})_{pp} = [(V_{gnd})_{pp}TF_{c1} + ... + (V_{gnd})_{pp}TF_{cn}] + [(I_{bulk1})_{pp}TF_{ib1} + ... + (I_{bulkn})_{pp}TF_{ibn}], \quad (11)$$

where $TF_{c1}, ..., TF_{cn}$ represent the voltage noise transfer function from the corresponding contact location to the sense node, and $TF_{ib1}, ..., TF_{ibn}$ represent the current noise transfer function from the corresponding bulk current source to the sense node. These transfer functions are determined from the resistive substrate network, as illustrated in Fig. 2. Matlab code is generated based on this model to quantify various noise sources and evaluate the dominant coupling mechanism.

C. Extraction of Parameters and Model Validation

An industrial 90 nm CMOS technology with a bulk-type substrate is used to extract the parameters required for the

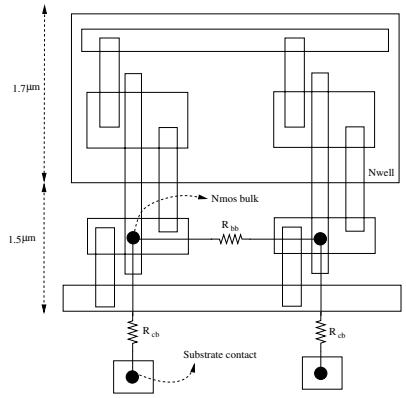

Fig. 3. Layout of two inverters to extract the substrate resistance between the bulk of the NMOS devices (R_{bb}) and the substrate resistance between the bulk of an NMOS device and the substrate contact (R_{cb}) in a 90 nm CMOS technology with a bulk type substrate.

models. An inverter with NMOS size, $W/L = 0.31$ μm / 0.1 μm, and PMOS size, $W/L = 0.44$ μm / 0.1 μm, is used as the standard cell for all of the analyses presented in this paper. The layout of the two cells, as shown in Fig. 3, is extracted using Assura and SubstrateStorm [9]. The related parameters are listed in Table I. The peak switching and bulk currents are obtained when the cell is driven by a ramp input with a 100 ps rise and fall time and drives an identical gate. The substrate resistances R_{dist} and R_{sc} are similarly extracted assuming the sense node is located 100 μm from the aggressor circuit, and the sense node is placed within a $p+$ guard ring with 15 analog substrate contacts.

At a certain number of switching gates, the estimated peak-to-peak ground and substrate noise is characterized, respectively, by (7) and (11). These expressions are compared with SPICE simulations in Figs. 4 and 5, where $n = 200$, $L_g = 1$ nH, $C_d = 10$ pF, $R_g = 2.2$ Ω, and $R_d = 0.1$ Ω, and the substrate

TABLE I

THE EXTRACTED PARAMETERS OF AN INVERTER IN A 90 NM CMOS TECHNOLOGY.

Parameter	Value
$(W/L)_{nmos}$	0.31 μm / 0.1 μm
$(W/L)_{pmos}$	0.44 μm / 0.1 μm
$(I_{swi-g})_p$	57.5 μA
$(I_{bulk-g})_p$	6.7 μA
R_{bb}	16.8 kΩ
R_{cb}	10.7 kΩ
R_{dist}	40 kΩ
R_{sc}	660 Ω

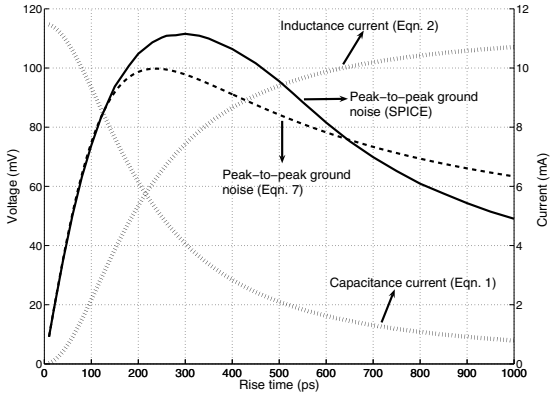

Fig. 4. Comparison of peak-to-peak ground noise as a function of the rise time obtained from SPICE simulations and (7) for $n = 200$. The ground network impedances are $L_g = 1$ nH, $C_d = 10$ pF, $R_g = 2.2$ Ω, and $R_d = 0.1$ Ω. The dotted lines depict the estimated capacitive and inductive currents as a function of the rise time.

resistances are $R_{bb} = 16.8$ kΩ, $R_{cb} = 10.7$ kΩ, $R_{dist} = 40$ kΩ, and $R_{sc} = 660$ Ω. The parasitic impedance of the analog ground network is assumed to be the same as the digital ground network, specifically, $R_{ang} = 2.2$ Ω and $L_{ang} = 1$ nH. The model accurately captures the nonmonotonic dependence of noise on rise time, exhibiting a maximum error of 12.5% for the peak-to-peak ground noise and 18.4% for the substrate noise. Note that this error is due to approximating the noise as a ramp function which is a better assumption for smaller rise times, producing a smaller error, as shown in Fig. 5.

III. DOMINANT SUBSTRATE NOISE COUPLING

The models and expressions for ground and source/drain coupling are used in this section to evaluate the dominant substrate noise generation mechanism. The boundary conditions are determined where the ground coupling exceeds the source/drain coupling. These conditions are presented as a function of the parasitic inductance L_g, decoupling capacitor C_d, rise time t_r, and number of switching gates n.

The extraction and simulation of large scale circuits to determine the dominant noise generation mechanism is not feasible due to the high computational requirements since the logic gates, power/ground network, and substrate must all be considered together [10], [11], [12]. A sufficiently accurate model which considers the effects of multiple parameters on the dominant noise is therefore required. The models and expressions presented in this paper are used to compare

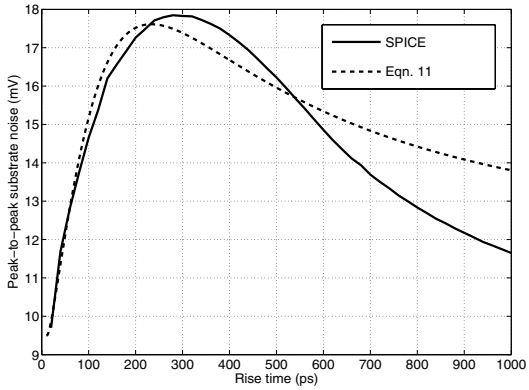

Fig. 5. Comparison of peak-to-peak substrate noise as a function of the rise time obtained from SPICE simulations and (11) for $n = 200$. The ground network impedances are $L_g = 1$ nH, $C_d = 10$ pF, $R_g = 2.2$ Ω, and $R_d = 0.1$ Ω. The substrate resistances are $R_{bb} = 16.8$ kΩ, $R_{cb} = 10.7$ kΩ, $R_{dist} = 40$ kΩ, and $R_{sc} = 660$ Ω. The analog ground network impedances are $R_{ang} = 2.2$ Ω and $L_{ang} = 1$ nH.

source/drain coupling with ground coupling, thereby providing improved understanding of the behavior of these two noise generation mechanisms as a function of multiple parameters.

Based on the model shown in Fig. 2, a specific number of switching gates exists beyond which ground coupling exceeds source/drain coupling. This number depends primarily upon the rise time, parasitic inductance, and decoupling capacitance. The effect of the number of switching gates, decoupling capacitance, and parasitic inductance on the dominant noise generation mechanism is explained, respectively, in Sections III-A and III-B.

A. Effect of Number of Switching Gates on the Dominant Noise Coupling Mechanism

As a greater number of gates simultaneously switch, the ground noise on each substrate contact increases due to the additional supply current. The ground coupling component of the substrate noise therefore increases with a larger number of switching gates. Furthermore, each switching gate injects noise from the junction capacitances, increasing the source/drain junction coupling mechanism. Alternatively, a contact filters the noise injected by the source/drain junction coupling and ground coupling of the other contacts, reducing the overall substrate noise.

An example of source/drain coupling, ground coupling, and the total noise vs. number of switching gates is shown in Fig. 6, as predicted based on the model illustrated in Fig. 2. For a small number of switching gates, source/drain coupling dominates the ground coupling. For a larger number of switching gates, the ground coupling increases at a faster rate as compared to the source/drain coupling due to an increase in the overall supply current and number of contacts. The injected noise from the source/drain coupling is primarily filtered by these contacts rather than propagated towards the sense node. The source/drain coupling component of the substrate noise is, therefore, primarily produced by those gates closest to the

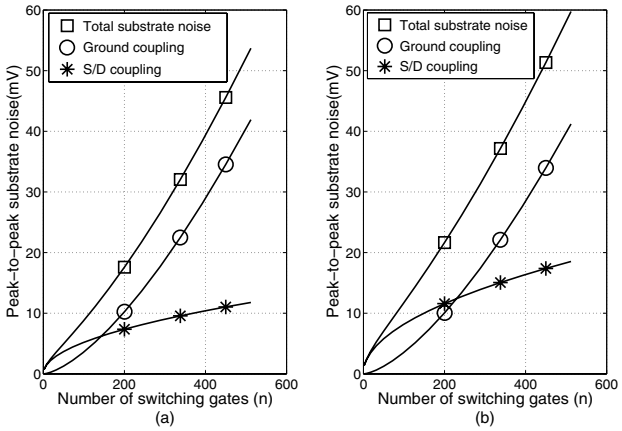

Fig. 6. Number of simultaneously switching gates vs. substrate noise as predicted by (11) when $(t_r)_i = 250$ ps, $L_g = 1$ nH, $C_d = 10$ pF, $R_g = 2.2\ \Omega$, $R_d = 0.1\ \Omega$, $R_{bb} = 16.8$ kΩ, $R_{cb} = 10.7$ kΩ, $R_{dist} = 40$ kΩ, $R_{sc} = 660\ \Omega$, $R_{ang} = 2.2\ \Omega$, and $L_{ang} = 1$ nH. (a) Each gate has a substrate contact, (b) two gates share one substrate contact.

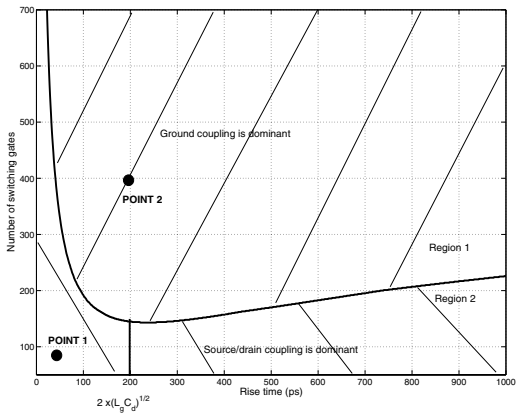

Fig. 7. For each rise time, the number of switching gates for which source/drain coupling is equal to ground coupling is determined from (11). Regions 1 and 2 represent, respectively, the area where ground and source/drain coupling are dominant. The operating parameters are $L_g = 1$ nH, $C_d = 10$ pF, $R_g = 2.2\ \Omega$, $R_d = 0.1\ \Omega$, $R_{bb} = 16.8$ kΩ, $R_{cb} = 10.7$ kΩ, $R_{dist} = 40$ kΩ, $R_{sc} = 660\ \Omega$, $R_{ang} = 2.2\ \Omega$, and $L_{ang} = 1$ nH.

sense node. At a certain number of switching gates, the ground coupling becomes larger than the source/drain coupling. Note that this crossover number is higher in Fig. 6(b) where the two gates share one contact as opposed to Fig. 6(a) where a contact exists for each gate.

Ground coupling starts to dominate source/drain coupling beyond this crossover point. For large scale circuits with a significant number of switching gates, ground coupling is expected to be the dominant substrate noise generation mechanism. Source/drain coupling is effective only for a small number of gates which are sufficiently close to the sense node. For localized noise analysis, however, the effect of source/drain coupling cannot be neglected. Note that the specific number of switching gates where the crossover occurs is highly dependent on the rise time, parasitic inductance, and decoupling capacitance, as explained in the following section.

B. Effect of Rise Time, Inductance, and Capacitance on Dominant Noise Coupling Mechanism

The peak-to-peak ground noise is a function of the rise time of the current load, parasitic inductance of the ground network, and the decoupling capacitance in the circuit, as specified by (7). Correspondingly, these parameters determine the dominant substrate noise generation mechanism by affecting the number of switching gates at which ground coupling surpasses source/drain coupling. These crossover points are numerically determined at each rise time using (11) to quantify and compare those regions where ground and source/drain coupling are dominant. The results are illustrated in Fig. 7. At each rise time, the number of switching gates at which ground coupling is equal to source/drain coupling is illustrated. Hence, the area above the curve represents the region where ground coupling is dominant (region 1) and, correspondingly, source/drain coupling is dominant under the curve (region 2). Note that this graph is obtained for a specific value of decoupling capacitance and parasitic inductance.

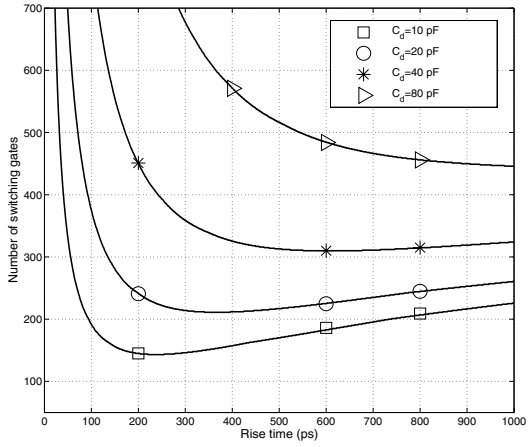

Fig. 8. The effect of decoupling capacitance on the dominant noise coupling mechanism. The data shown in Fig. 7 is obtained for different decoupling capacitances while the other circuit parameters are maintained the same.

For sufficiently small rise times, the ground noise is relatively low since the decoupling capacitance is effective. The number of switching gates where the crossover occurs is therefore the greatest for small rise times. This crossover point decreases as the rise time increases and is smallest at $t_r \approx 2\sqrt{(L_g C_d)}$ where the ground noise is greatest, maximizing the area of region 1. As the rise time further increases, the ground noise decreases due to lower $L\,\partial i/\partial t$ noise, increasing the area of region 2. Note that for small rise times or, equivalently, at higher operating frequencies, source/drain coupling becomes the significant noise injection mechanism.

The same graph is obtained for different decoupling capacitances and parasitic inductances in order to evaluate the effect of these parameters on the dominant noise generation mechanism, as shown in Figs. 8 and 9, respectively. As

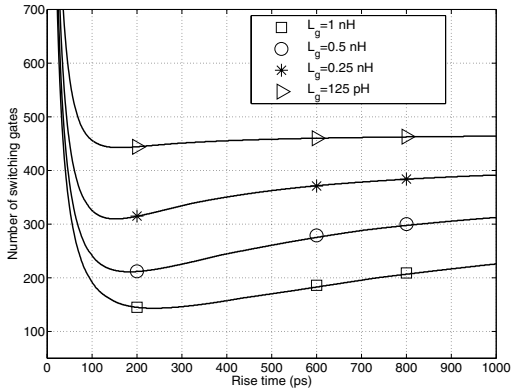

Fig. 9. The effect of parasitic inductance on the dominant noise coupling mechanism. The data shown in Fig. 7 is obtained for different parasitic inductances while the other circuit parameters are maintained the same.

the parasitic inductance decreases or the decoupling capacitor increases, the area of region 1 decreases while the area of region 2 increases. For example, at $t_r = 300$ ps, the number of switching gates n where the ground coupling is equal to the source/drain coupling is 146 for $C_d = 10$ pF. Alternatively, if $C_d = 40$ pF and 80 pF, n increases, respectively, to 359 and 677, as shown in Fig 8. Similarly, at the same rise time, the ground coupling and source drain coupling are equal at $n = 146$ for $L_g = 1$ nH and at $n = 334$ and 451 for $L_g = 0.25$ nH and 125 pH, respectively, as shown in Fig 9. Thus, for circuits with flip-chip packages and sufficiently high decoupling capacitance, source/drain coupling cannot be neglected and may be the dominant substrate noise generation mechanism.

IV. Discussion

Identification of the dominant substrate noise coupling mechanism helps determine the preferable noise reduction technique for a given set of parameters. For example, for cases where source/drain coupling dominates, increasing the number of substrate contacts or a p+ guard ring around the aggressor circuit achieves enhanced noise reduction as compared to reducing the parasitic inductance on the ground lines or increasing the decoupling capacitance. Alternatively, if ground coupling is the dominant coupling mechanism, placing additional decoupling capacitance and reducing the parasitic inductance are more efficient techniques.

In Fig. 7, points 1 and 2 represent, respectively, the dominance of source/drain coupling and ground coupling. For point 1, the peak-to-peak substrate noise is reduced by 31% by doubling the substrate contacts. Lowering the parasitic inductance by a factor of four reduces the noise by only 3.5%. Similarly, increasing the decoupling capacitance by a factor of four reduces the noise by 10.5%. Alternatively, for point 2, where ground coupling is dominant, doubling the substrate contacts achieves a 12.1% reduction in noise while reducing the parasitic inductance and increasing the decoupling capacitance, each by a factor of four, reduces the noise by, respectively, 34.1% and 42.8%. These results are listed in Table II.

TABLE II

Comparison of three noise reduction techniques for two different points, as shown in Fig. 7.

	Point 1	Point 2
Reduce L_g by four	3.5%	34.1%
Increase C_d by four	10.5%	42.8%
Double substrate contact density	31.4%	12.1%

V. Conclusions

A model is presented that determines the dominant substrate noise coupling mechanism for multiple switching gates. The model accurately captures the effects of multiple parameters, as validated by SPICE. The regions where ground coupling and source/drain coupling dominate are determined based on this model. Given a set of parameters, the dominant noise source is identified. The effect of the number of switching gates, rise time, decoupling capacitance, and parasitic inductance on the dominant noise coupling mechanism is investigated. Ground coupling tends to dominate if a larger number of gates are switching. For a sufficiently high decoupling capacitance and low parasitic inductance, such as a flip-chip package, source/drain coupling is shown to be the dominant noise coupling mechanism.

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