On-Chip DC-DC Converters for Three-Dimensional ICs

Jonathan Rosenfeld and Eby G. Friedman

Department of Electrical and Computer Engineering
University of Rochester

Abstract—**Guidelines for distributing a buck converter rectifier for application to three-dimensional (3-D) circuits is described. The 3-D rectifier exploits the properties of transmission lines to generate and distribute power supplies to different planes. As compared to a conventional rectifier, the proposed rectifier circuit only requires moderately size capacitors without the use of on-chip inductors. A case study in a 0.18 μm CMOS 3-D technology demonstrates the generation of a 1.2 volt power supply delivering 700 mA peak current.**

I. INTRODUCTION

With the significant performance improvement offered by 3-D circuits [1], new design challenges arise. One primary requirement of 3-D integrated systems is diverse, high quality, and reliable power. This fundamental issue of power generation and distribution in 3-D circuits is explored in this paper.

Three-dimensional integrated circuits are comprised of multiple planes with many circuit domains. The different planes are typically dedicated to a specific function, forming a highly heterogeneous system [1], [2], [3]. As an example, RF, analog, communications, and digital circuits are typically located on different planes, requiring a variety of power supply voltages, as illustrated in Fig. 1. In this example, V_{dd1}, V_{dd2}, V_{dd3}, and V_{dd4} are generated from the primary power supply V_{dd}.

Multiple circuit domains require several power supplies to reliably operate and provide sufficient and stable current. To provide circuit domains with the appropriate power supplies, DC-DC converters are distributed across each plane [4] as it is often impractical to provide external power supplies due to the limited number of input pins. Moreover, planes located far from the faces of the 3-D cube require a large number of expensive 3-D vias to distribute the power supply across the plane.

To alleviate these difficulties, DC-DC converters are distributed on-chip, generating a specific voltage required by the different circuit blocks within each plane of a 3-D system. A suitable DC-DC converter for low power applications is a buck converter [4], [5]. A buck converter generates an output supply voltage with a magnitude smaller than the input supply voltage [4]. This property is useful for on-chip power supply generation.
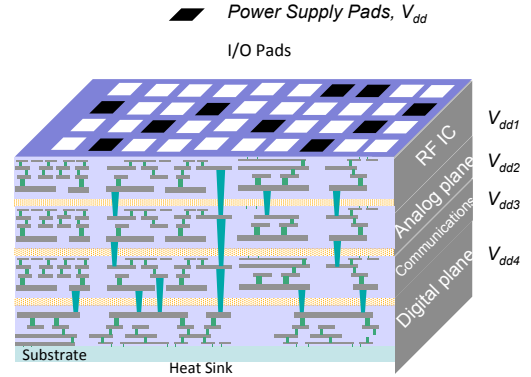
Fig. 1.   Three-dimensional circuit with multiple power supplies

Exploiting the rectifier portion of a buck converter to generate and distribute power supplies in 3-D integrated circuits is the primary focus of this paper. The proposed rectifier is comprised of on-chip interconnects and capacitors, eliminating the need for on-chip inductors. For a target DC voltage ripple, the distributed rectifier produces the required transfer function, passing the DC component of the input signal while attenuating the high frequency harmonics.

The paper is organized into six sections. Background on the operation of a conventional buck converter is reviewed in section II. In section III, the operating principle behind a novel distributed rectifier within a buck converter is presented, followed by a methodology for designing these circuits in section IV. To exemplify the proposed approach, a case study is described in section V. Finally, some conclusions are offered in section VI.

II. BACKGROUND

A standard topology of a buck converter for high performance microprocessors is depicted in Fig. 2(a) [4]. The power MOSFETs produce an AC signal at node A by a signal controlled by a pulse width modulator (PWM), as shown in Fig. 2(b). The AC signal at node A is filtered by a rectifier composed of a second order low pass band LC filter. Assuming the resonance frequency $1/2\pi\sqrt{LC}$ is less than the switching frequency of the power MOSFETs, the filter only passes the DC component of the signal and a residue composed of the high frequency harmonics.

The DC component of the signal shown in Fig. 2(b) is

$$\frac{1}{T_s} \int_0^{T_s} V_A \, dt = \frac{V_{dd1}(2DT_s - t_{rp} + t_{fp})}{2T_s}, \qquad (1)$$
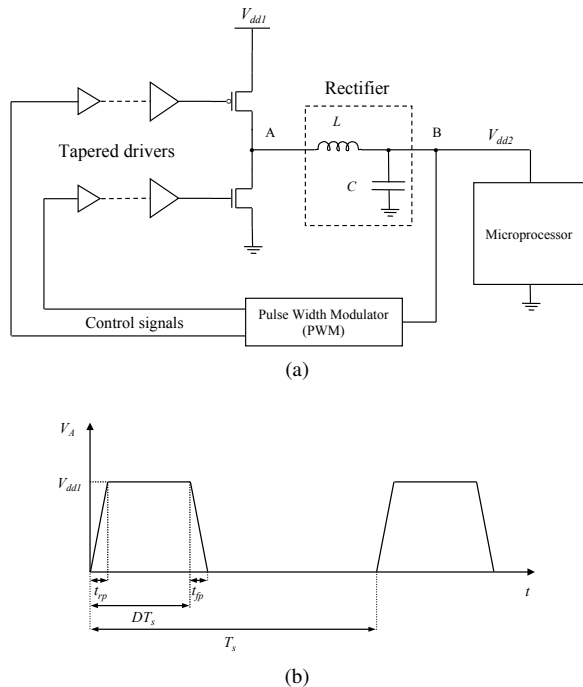
Fig. 2. Conventional DC-DC converter: (a) buck converter circuit [4], (b) signal at the output of the power MOSFETs (node A)

where D, T_s, and V_{dd1} are the duty cycle, time period, and input power supply, respectively, and t_{rp} and t_{fp} are the rise and fall times, respectively, of the switching signal produced by a pulse width modulator (PWM) circuit. In the case of $t_{rp} = t_{fp}$, (1) reduces to

$$V_{dd2} = V_{DC}|_{t_{rp}=t_{fp}} = DV_{dd1}. \qquad (2)$$

Hence, the buck converter produces an output voltage V_{dd2} at node B equal to DV_{dd1}.

The power transistors are typically large in physical size and are therefore driven by tapered buffers [6]. These buffers are controlled by the PWM circuit. The feedback PWM circuit senses the output voltage supply V_{dd2} at node B and modifies the control signal to ensure that the appropriate duty cycle D is produced at node A. In this manner, the output voltage is maintained at the desired value while compensating for variations in the load current and input voltage. The performance and functionality of the different circuit domains under load current and DC input voltage variations are dependent upon the maximum voltage fluctuations generated by the buck converter, which is therefore regulated to provide the target voltage [4].

The performance of a buck converter can be improved by integrating these converters on-chip. In this manner, the parasitic losses associated with the interconnects among the non-integrated components of the DC-DC converter are significantly decreased. Moreover, integrated converters benefit by advances in on-chip technologies and high operating frequencies. Monolithic fully integrated DC-DC converters

can therefore achieve higher efficiency as compared to non-integrated converters [7], [8].

Integrating DC-DC converters on-chip in both 2-D and 3-D technologies, however, imposes challenges as the on-chip integration of large inductive and capacitive elements is problematic. A significant issue is the poor parasitic impedance characteristics exhibited by the on-chip inductors, which degrades the performance of the on-chip converter. Although the size and magnitude of the on-chip inductors and capacitors required to implement a buck converter are reduced with increasing switching frequency, the on-chip passive devices comprising the rectifier are large and cannot be practically integrated in the megahertz frequency regime.

In [9] and [10], exotic inductor technologies have been developed to support the on-chip integration of a DC-DC converter in a stacked-chip environment. In [9], a coupled thin film with magnetic core inductors is integrated on-chip, achieving a high effective inductance while in [10], an air core spiral inductor is integrated in a 180 nm SiGe BiCMOS technology. In both circuits, a special inductor technology is utilized to achieve higher inductance and efficiency. In [11], a $2 \times 2 \, \mu m^2$ plane within a stacked-chip technology is used for the on-chip LC output filter. By exploiting higher switching frequencies and the proposed distributed rectifier, the on-chip integration and distribution of these types of power supplies in 2-D and, in particular, 3-D circuits become possible. All of these circuits, however, do not consider current distribution to the target planes. The multi-plane structure of a 3-D system accommodates the nature of the proposed distributed rectifier, achieving efficient generation and distribution of the power supplies.

A three-dimensional technology provides several advantages as compared to a two-dimensional technology. When the on-chip capacitors used by a distributed rectifier are implemented with active devices, less metallization resources are required to connect these capacitors to different sections of the rectifier as compared to a 2-D technology. Since in 3-D circuits each plane has a dedicated active device layer, routing congestion is reduced. Moreover, in a typical 2-D or 3-D system, the primary power supply is located on the top layers. In a 2-D technology, the input power supply to the power MOSFETs is routed to the lowest layer, where the active devices are located, therefore, additional routing resources are required. In a 3-D technology, however, the closest plane to the input power supply accommodates the power MOSFETs, saving metallization resources. The capacitance and inductance of the through silicon vias are also exploited, reducing the length of the interconnects and the size of the capacitors. An inherent benefit of utilizing the proposed rectifier in 3-D systems is that the generation and distribution of the power supply occur simultaneously, while in 2-D systems the rectifier can only be used to generate the power supply.

III. PRINCIPLE OF A DISTRIBUTED RECTIFIER

The proposed rectifier exploits the impedance characteristics of long transmission lines. By suppressing the inductive effects
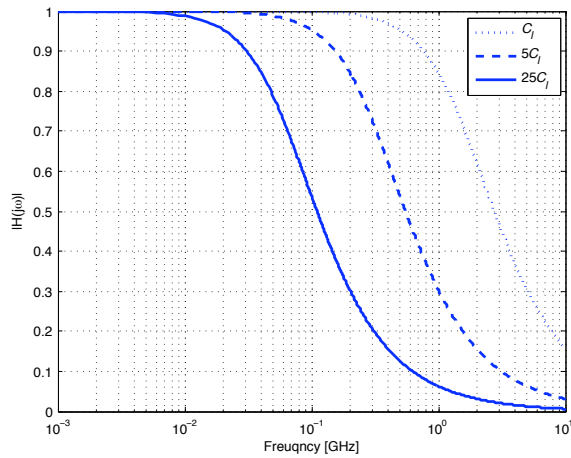
Fig. 3. Transfer function of the magnitude of an interconnect for different capacitive loads

Fig. 4. A distributed rectifier

A. Physical structure and current load properties of a 3-D rectifier

The proposed distributed rectifier is depicted in Fig. 4. The rectifier is driven by power MOSFETs (see Fig. 2(a)) which are modeled as a voltage source V_A followed by an effective resistance R_d. The power MOSFETs are connected in series with an on-chip resistor R_{rect}. The voltage source V_A is assumed to be periodic, as illustrated in Fig. 2(b).

Fig. 5. Profile of current load

of long interconnects, thereby attenuating the associated resonant peaks, the transfer function of the amplitude of these RC dominant interconnects exhibits no overshoots and decreases rapidly with increasing frequency. Consequently, this type of interconnect behaves as a low pass filter which can be utilized as a buck converter rectifier. In this manner, the high frequency harmonics of the AC signal at node A are filtered, producing a DC signal at node B. The distributed low pass filter spans multiple planes of a 3-D circuit, providing the required power supply to a specific circuit domain.

To illustrate this impedance behavior, consider a transmission line driven by a voltage source with an output resistance R_d and terminated with a capacitive load C_l. Transfer functions characterizing the effect of different capacitive loads are shown in Fig. 3. In this example, the driver resistance R_d, interconnect length l, and capacitive load C_l are $100\,\Omega$, $1\,\text{mm}$, and $1\,\text{pF}$, respectively, with transmission line parameters $r = 17\,\text{m}\Omega/\mu\text{m}$, $l = 1.66\,\text{pH}/\mu\text{m}$, and $c = 0.072\,\text{fF}/\mu\text{m}$.

Note that in the example depicted in Fig. 3, the resonant peaks associated with inductive effects do not appear. Additionally, as the load capacitance increases, the bandwidth of the low pass filter decreases. These observations suggest that an interconnect based rectifier can be used to generate and distribute power supplies within a 3-D system.

IV. DESIGN METHODOLOGY

A design methodology for a distributed buck converter is described in this section. A circuit and mathematical formulation of the power delivery process in 3-D circuits is presented. Based on the expressions developed here, design guidelines are provided. The physical structure of the distributed rectifier as well as the current load characteristics are described in section IV-A. In section IV-B, the transfer function of the rectifier is used to determine the condition that satisfies a target power supply ripple while the efficiency and area of the 3-D rectifier are determined in section IV-C.
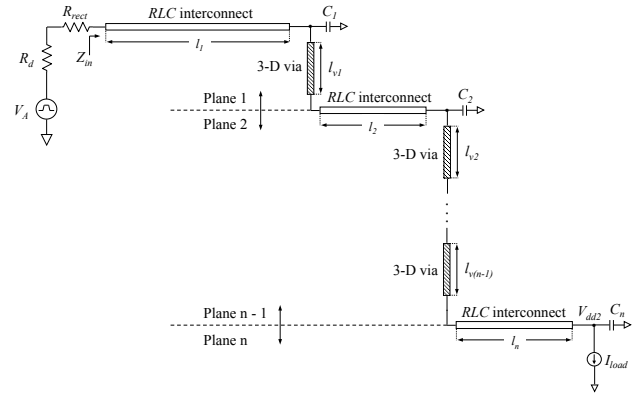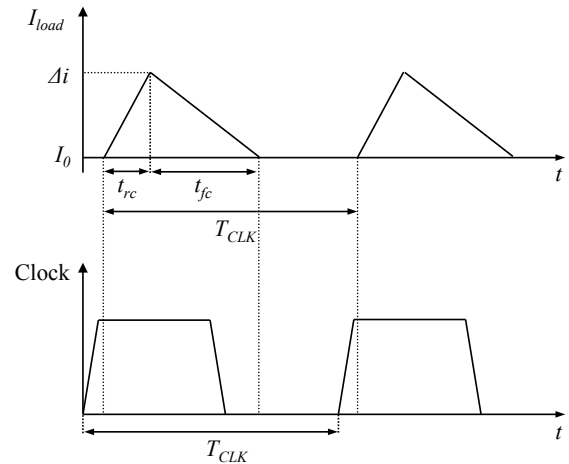
The rectifier is composed of transmission lines terminated with lumped capacitances. The inter-plane structure is connected by 3-D vias. At the target plane n, the load is represented by a periodic current load and a reference clock signal, as shown in Fig. 5. Note that the current load characterizes the approximate current profile of a specific circuit module within a plane.

In three-dimensional circuits, the ability to deliver current is primarily limited by the 3-D vias. The maximum current that can be delivered through a single 3-D via therefore determines the current magnitude,

$$I_0 + \Delta i = J_{via,max} \cdot A_{via} \cdot N, \qquad (3)$$

where $J_{via,max}$, A_{via}, and N are the maximum current density, cross-sectional area, and number of 3-D vias, respectively. Consequently, the maximum cross-sectional area of the interconnects (see Fig. 4) distributing the current within the different planes is

$$A_{int} = \frac{I_0 + \Delta i}{J_{int,max}} = \left(\frac{J_{via,max}}{J_{int,max}}\right) \cdot A_{via} \cdot N, \qquad (4)$$

where $J_{int,max}$ is the maximum current density of the interconnect.

In practical circuits, however, a significant amount of current is sunk by the load. To satisfy this requirement, multiple structures N, as depicted in Fig. 4, are connected in parallel, delivering $N(I_0 + \Delta i)$ amperes. In this case, the effective resistance and inductance per unit length of the interconnects and 3-D vias, as well as the output resistance of the driver and the on-chip rectifier R_{rect} (see Fig. 4), are N times smaller. The capacitance per unit length of the interconnects and 3-D vias, as well as the on-chip lumped capacitors, are N times larger.

B. Transfer function of a 3-D rectifier

To characterize the impedance of the rectifier (between R_d and I_{load}), the overall transfer function is determined based on the $ABCD$ matrices. Hence, the overall $ABCD$ matrix of a rectifier spanning n planes is

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & R_d + R_{rect} \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} A' & B' \\ C' & D' \end{bmatrix}. \qquad (5)$$

The right matrix in the right hand side of (5) is

$$\begin{bmatrix} A' & B' \\ C' & D' \end{bmatrix} = \prod_{i=1}^{n} \left(\begin{bmatrix} \cosh\gamma l_i & Z_0 \sinh\gamma l_i \\ \sinh\gamma l_i/Z_0 & \cosh\gamma l_i \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C_i & 1 \end{bmatrix} \right.$$
$$\left. \cdot \begin{bmatrix} \cosh\gamma_v l_{vi} & Z_{v0} \sinh\gamma_v l_{vi} \\ \sinh\gamma_v l_{vi}/Z_{v0} & \cosh\gamma_v l_{vi} \end{bmatrix} \right), \quad (6)$$

where Z_0 and γ are the characteristic impedance and propagation constant of the RLC interconnects, respectively, l_i and C_i are the interconnect length and capacitance on the ith plane, respectively, Z_{v0} and γ_v are the characteristic impedance and propagation constant of the 3-D vias, respectively, and l_{vi} is the length of the 3-D via on the ith plane. The transfer function of the rectifier is

$$H_{rect}(j\omega_s) = \frac{1}{A}, \qquad (7)$$

where A is obtained from (5), and ω_s is the radian frequency of the switching signal.

Since a practical rectifier within a buck converter does not provide ideal low pass characteristics, the signal at node B, shown in Fig. 2(a), carries a small amount of high frequency harmonics generated by switching the power MOSFETs. Hence, the voltage at node B is

$$V_{dd2}(t) = V_{DC} + V_r \sin(\omega_s t), \qquad (8)$$

where V_{DC} is the DC component of the output voltage described by (1) and V_r is the target voltage ripple (peak-to-peak) transferred by the non-ideal characteristics of the rectifier. When only the fundamental harmonic is passed, the ripple voltage exhibits a sinusoidal behavior. To satisfy a target ripple voltage V_r, the rectifier transfer function at the switching frequency f_s has to achieve a specific magnitude. To satisfy this objective, consider the output signal in the frequency domain,

$$|V_{dd2}(s)| = |H_{rect}(s)| \cdot |V_A(s)|. \qquad (9)$$

The periodic input signal V_A can be represented by a Fourier series,

$$v_A(t) = \sum_{k=-\infty}^{\infty} a_k e^{jk\omega_s t}, \qquad (10)$$

where a_k is the kth harmonic of the signal. In the case of the signal illustrated in Fig. 2(b) and assuming $t_{rp} = t_{fp} = t_r$, the fundamental harmonic (positive and negative) is

$$a_{\pm 1} = \left(\frac{V_{dd1}T_s}{4t_r\pi^2}\right) \cdot \left(e^{\mp j\omega_s t_r}\left(1 - e^{\mp j2\pi D}\right) + e^{\mp j2\pi D} - 1\right). \qquad (11)$$

Equation (9) implies that the required amplitude of the transfer function for a specific ripple voltage V_r is

$$|H_{rect}(j\omega_s)| \leq \frac{V_r/2}{2|a_1|} = \frac{V_r}{4|a_1|}. \qquad (12)$$

Once the current profile of a circuit is determined, the interconnect length l_1 to l_n, shown in Fig. 4, and the required ripple voltage V_r are chosen. Based on (7), the magnitude of the transfer function at ω_s is plotted as a function of the capacitances, C_1 to C_n. The interconnect length and capacitance are chosen to satisfy (12).

To achieve a specific DC voltage at the output of the rectifier, the duty cycle in (2) is modified to

$$D_{PWM} = D \cdot \left|1 + \frac{R_d + R_{rect}}{Z_{in}(0)}\right|. \qquad (13)$$

Observe from (13) that D_{PWM} is always larger then the original duty cycle D obtained from (2), limiting the magnitude of the generated power supply.

C. Efficiency and area of a 3-D rectifier

An important property of a buck converter is the power efficiency. The efficiency of a distributed rectifier is

$$\eta_{rect} = \frac{P_{load}}{P_{load} + P_{rect}} \times 100, \qquad (14)$$

where P_{load} is the average power delivered to the load and P_{rect} is the average power consumed by the rectifier. The power expressions P_{load} and P_{rect} are, respectively,

$$P_{load} = V_{dd2}I_{DC}, \quad (15)$$

$$P_{rect} = \frac{1}{2} \cdot V_{A,rms}^2 \left| \frac{Z_{in}(j\omega_s)}{Z_{in}(j\omega_s) + R_d + R_{rect}} \right|^2$$
$$\cdot \Re\left\{ \frac{1}{Z_{in}(j\omega_s)} \right\}, \quad (16)$$

where $V_{A,rms}$ is the root-mean-square value of the driving signal with a duty cycle D_{PWM}, and $Z_{in}(j\omega_s)$ is

$$Z_{in}(j\omega_s) = \frac{V_{DC}A'(j\omega_s) + I_{DC}B'(j\omega_s)}{V_{DC}C'(j\omega_s) + I_{DC}D'(j\omega_s)}. \quad (17)$$

The area occupied by a 3-D rectifier is

$$A_{3-D,rect} = \left(A_{R_{rect}} + \sum_{i=1}^{n}(W_{metal,i} \cdot l_i + A_{C_i}) \right.$$
$$\left. + \sum_{i=1}^{n-1} A_{via,i} \right) \cdot N + S_i \cdot l_i \cdot n \cdot (N-1), \quad (18)$$

where $A_{R_{rect}}$ is the area occupied by the on-chip resistor while A_{C_i} and $A_{via,i}$ are the area occupied by the on-chip capacitors and 3-D vias on the ith plane, respectively. $W_{metal,i}$ and S_i are the width and spacing of the interconnects on the ith plane, respectively. As mentioned in section IV-A, n and N are the number of planes spanned by the rectifier and the number of parallel connected rectifier structures, respectively.

V. CASE STUDY

To demonstrate the design methodology described in section IV, an example DC-DC converter based on the MIT Lincoln Lab (MITLL) 180 nm 3-D integration process [12] is described in this section. Characterization of the maximum current that can flow through a single via is described in section V-A while a distributed rectifier based on a 3-D technology is described and compared in section V-B.

A. Current load characterization

The MITLL technology is a $0.18\,\mu\text{m}$ low power, fully depleted silicon-on-insulator (FDSOI) CMOS process where three independent wafers are physically bonded to form a 3-D integrated structure. Each plane has three aluminum metallization layers. In this technology, the maximum current density is [12]

$$J_{Al,3-D} = 3\,\text{mA}/\mu\text{m}^2. \quad (19)$$

Since the cross-sectional area of a 3-D via in this technology is $1.5 \times 1.5\,\mu\text{m}^2$, the maximum current that can flow through a single 3-D via, based on (3), is

$$I_0 + \Delta i \approx 7\,\text{mA}. \quad (20)$$

In this case study, the current load waveform, depicted in Fig. 5, has the following characteristics: $1/T_{CLK} = 3\,\text{GHz}$, and t_{rc} and t_{fc} are $0.3T_{CLK}/2$ and $0.7T_{CLK}/2$, respectively.

B. Distributed 3-D rectifier

A distributed rectifier circuit has been developed that generates and distributes the power supply to a target plane within a 3-D structure. This rectifier is described in this section. The resistance, inductance, and capacitance per unit length of the interconnects (Metal 3) and 3-D vias are extracted based on the predictive technology model (PTM) [13], [14], as listed in Table I. The width of the interconnects is determined by the maximum current density of the MITLL 3-D technology. Assuming that both the interconnect and 3-D vias support the same current density of $3\,\text{mA}/\mu\text{m}^2$, the maximum cross-sectional area of the interconnect determined from (4) is $1.5 \times 1.5\,\mu\text{m}^2$. The thickness of the interconnect for this technology is 630 nm, resulting in an approximately $4\,\mu\text{m}$ wide line. Note that each 3-D via is $7.34\,\mu\text{m}$ long, connecting three planes, as illustrated in Fig. 4.

TABLE I
RLC INTERCONNECT AND 3-D VIA IMPEDANCES

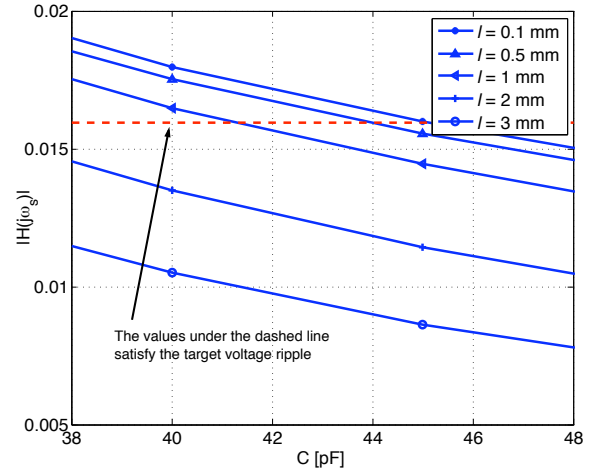|	$R\ [m\Omega/\mu\text{m}]$	$L\ [\text{pH}/\mu\text{m}]$	$C\ [\text{fF}/\mu\text{m}]$
Interconnects	14.5	1.3	0.5
3-D via [14]	20.40	0.55	0.37

Fig. 6. Magnitude of the transfer function at ω_s for different line lengths and capacitances

The magnitude of the transfer function at ω_s for different capacitances and interconnect lengths, assuming $l = l_1 = l_2 = l_3$ and $C = C_1 = C_2 = C_3$, is depicted in Fig. 6. On-chip resistance $R_{rect} = 500\,\Omega$, is assumed in this case study.

As the interconnect line length increases, less capacitance is required, as evident in Fig. 6. To satisfy the required
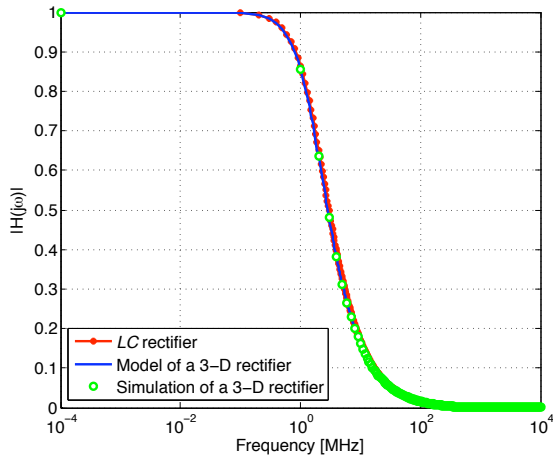
Fig. 7. Simulation and model of the magnitude of the transfer function of a 3-D rectifier and a conventional **LC** rectifier circuit
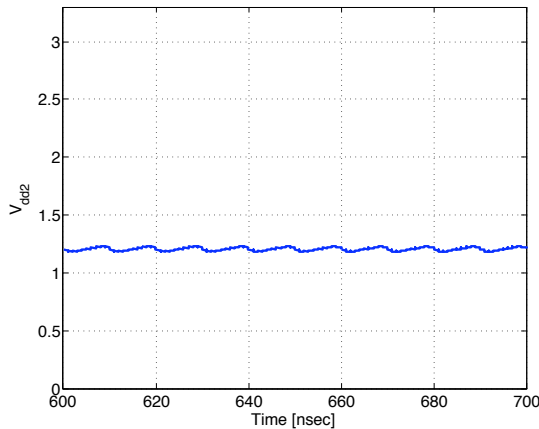

Fig. 8. DC voltage at the output of a distributed rectifier

voltage ripple, the target interconnect length in this example is $l = 1$ mm with a capacitance $C = 42$ pF. The magnitude of the transfer function of the distributed rectifier is shown in Fig. 7. Note that the simulated rectifier accurately verifies the physical model described in section IV. The DC voltage at the output of the rectifier is shown in Fig. 8. In this example, the required duty cycle of the signal driving the power MOSFETs is $D_{PWM} = 0.73$, and the efficiency of the rectifier is about 88%.

If additional current is required, the distributed rectifier can be extended by connecting multiple structures in parallel. For example, to enlarge this structure to provide 700 mA, 100 parallel structures are required. In this case, the effective resistance and inductance per unit length, listed in Table I, R_d, and R_{rect} are N times smaller, while the capacitance per unit length is N times larger. The multiple parallel rectifiers produce the same transfer function magnitude, as shown in Fig. 6. The same interconnect lengths and capacitances can therefore be chosen, producing a 1.2 volt power supply with

700 mA maximum current.

VI. CONCLUSIONS

Integrating DC-DC converters on-chip can significantly enhance the performance and reliability of integrated circuits. Conventional rectifiers, however, are difficult to integrate due to the large magnitude of the on-chip inductors and capacitors. A distributed buck converter rectifier for application to three-dimensional circuits is proposed in this paper. By exploiting the low pass bandwidth properties of transmission lines, the efficient generation and distribution of power supplies to different planes are possible. An example converter based on the MITLL 3-D CMOS technology is described, demonstrating a DC-DC converter that can generate a 1.2 volt power supply while delivering 700 mA.

REFERENCES

[1] V. F. Pavlidis and E. G. Friedman, *Three-Dimensional Integrated Circuit Design*, Morgan Kaufmann, 2009.
[2] R. G. Gutmann *et al.*, "Three-Dimensional ICs: A Technology Platform for Integrated Systems and Opportunities for New Polymeric Adhesives," *Proceedings of the IEEE International Conference on Polymers and Adhesives in Microelectronics and Photonics*, pp. 173–180, October 2001.
[3] C. S. Tan, R. J. Gutmann, and L. R. Reif, *Wafer Level 3-D ICs Process Technology*, Springer, 2008.
[4] V. Kursun and E. G. Friedman, *Multi-Voltage CMOS Circuit Design*, John Wiley & Sons, 2006.
[5] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, Kluwer, 2001.
[6] B. S. Cherkauer and E. G. Friedman, "A Unified Design Methodology for CMOS Tapered Buffers," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 3, No. 1, pp. 99–111, March 1995.
[7] R. S. Kagan and M. Chi, "Improving Power Supply Efficiency with MOSFET Synchronous Rectifiers," *Proceedings of the IEEE International Conference on Polymers and Adhesives in Microelectronics and Photonics*, pp. D4.1–D4.9, July 1982.
[8] V. Kursun, S. G. Narendra, V. K. De, and E. G. Friedman, "Low-Voltage-Swing Monolithic DC-DC Conversion," *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 51, No. 5, pp. 241–248, May 2004.
[9] G. Schrom, P. Hazucha, J.-H. Hahn, V. Kursun, D. Gardner, S. Narendra, T. Karnik, and V. De , "Feasibility of Monolithic and 3D-Stacked DC-DC Converters for Microprocessors in 90nm Technology Generation," *Proceedings of the IEEE International Symposium on Low Power Electronics and Design*, pp. 263–268, August 2004.
[10] J. Sun, J.-Q. Lu, D. Giuliano, T. P. Chow, and R. J. Gutmann, "3D Power Delivery for Microprocessors and High-Performance ASICs," *Proceedings of the IEEE Applied Power Electronics Conference*, pp. 127–133, February 2007.
[11] K. Onizuka, K. Inagaki, H. Kawaguchi, M. Takamiya, and T. Sakurai, "Stacked-Chip Implementation of On-Chip Buck Converter for Distributed Power Supply System in SiPs," *IEEE Journal of Solid-State Circuits*, Vol. 43, No. 11, pp. 2404–2410, November 2007.
[12] MIT Lincoln Laboratories, *MITLL Low-Power FDSOI CMOS Process Design Guide*, 2006.
[13] Predictive Technology Model: http://www.eas.asu.edu/~ptm.
[14] I. Savidis and E. G. Friedman, "Electrical Characterization and Modeling of 3-D Vias," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 784–787, May 2008.