An Area Effcient On-Chip Hybrid Voltage Regulator

Selçuk Köse and Eby G. Friedman
Department of Electrical and Computer Engineering
University of Rochester
Rochester, New York 14627
{kose, friedman}@ece.rochester.edu

Simon Tam
Intel Corporation
Santa Clara, California 95054
simon.tamee1688@hotmail.com

Sally Pinzon and Bruce McDermott
Eastman Kodak
Rochester, New York 14652
sally.pinzon@kodak.com
lwjq00@rochester.rr.com

***Abstract*— Experimental results of an active filter based on-chip hybrid voltage converter are described in this paper. The area of the voltage converter is significantly less than the area of a conventional passive filter based DC-DC voltage converter or a low-dropout (LDO) regulator. Hence, the proposed circuit is appropriate for point-of-load voltage regulation for the noise sensitive portions of an integrated circuit. The performance of the circuit has been verified with Cadence Spectre simulations and fabricated with a commercial 110 nm CMOS technology. The area of the voltage regulator is 0.015 mm^2 and delivers up to 80 mA of output current. The transient response with no output capacitor ranges from 72 ns to 192 ns. The advantages and disadvantages of an active filter based, conventional switching, linear, and switched capacitor voltage converters are compared. The proposed circuit provides a means for distributing multiple local power supplies across an integrated circuit while maintaining high current efficiency and fast response time within a small area.**

I. Introduction

The power supply voltage aggressively scales with each technology generation, making the delivery of a high quality supply voltage to noise sensitive circuit blocks highly challenging [1]–[3]. The number of voltage domains within an integrated circuit is increasing to satisfy stringent power budgets [4]. This increase in the number of voltage domains requires innovative techniques to generate these voltages close to the load circuitry while occupying a small area (point-of-load voltage delivery). Physical size is therefore a primary issue for point-of-load voltage regulation.

Several topologies are commonly used to generate DC voltages on-chip. DC-DC voltage converters are generally used as on-chip power supplies in high performance integrated circuits. Conventional DC-DC converters can be grouped into three primary categories; switching, switched capacitor (SC), and linear DC-DC converters [2]. These classical power supply topologies occupy large on-chip area and are therefore inappropriate for point-of-load power delivery.

An area efficient voltage converter is required for the next generation of multi-voltage systems because these systems are highly sensitive to local power/ground (P/G) noise. To produce a voltage regulator appropriate for distributed point-of-load voltage generation, the passive LC filter within a buck converter is replaced with a more area efficient active filter [5]–[7]. A switching voltage is generated at the input of the active filter and the converter with this filter structure produces the desired output voltage. The current supplied to the output node, however, does not originate from the input switching signal; rather, from the operational amplifier (Op Amp) output stage, similar to a linear voltage converter. This voltage converter is therefore a hybrid combination of a switching and linear DC-DC converter. In this paper, experimental results characterizing this promising hybrid voltage regulator topology [5], [6] is experimentally verified. Design tradeoffs among area, maximum load current, and load regulation are evaluated with experimental results. The on-chip area of this hybrid regulator is 0.015 mm^2 with a mature 110 nm CMOS technology, significantly smaller than state-of-the-art output capacitorless LDOs. The power efficiency, however, is limited to V_{out}/V_{in}, similar to LDOs.

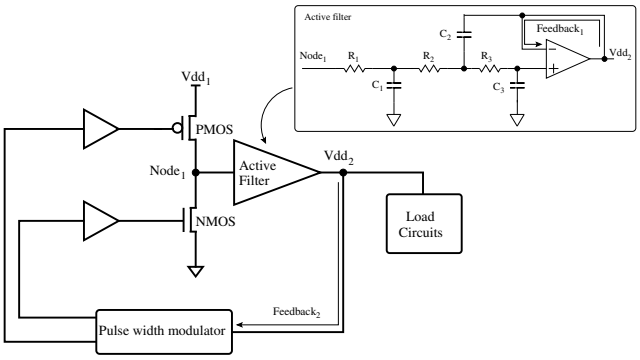

Fig. 1. Proposed DC-DC converter. Note that the passive LC filter is replaced with an active filter and the large tapered buffers are no longer necessary.

The rest of the paper is organized as follows. In Section II, background information is provided for the active filter-based hybrid voltage regulator. The design requirements of the Op Amp and related tradeoffs are also discussed in this section. The advantages and disadvantages of the proposed voltage regulator as compared to conventional switching and LDO regulators are discussed in Section III. Experimental results are provided in Section IV. The paper is concluded in Section V.

II. Active Filter Based Switching DC-DC Converter Design

In the proposed circuit, the bulky LC filter in a conventional buck converter is replaced with an active filter structure and the tapered buffers are replaced with smaller buffers, as shown in Fig. 1. The switching input signal generated at $Node_1$ is filtered by the active filter structure, similar to a buck converter, and a DC voltage is generated at the output. Increasing the duty

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TABLE I

SENSITIVITY ANALYSIS FOR A THIRD ORDER SALLEN-KEY FILTER.

	R1	R2	R3	C1	C2	C3
Q	0	-0.4	0.4	0	-0.5	0.5
Cut-off frequency	-1	-0.5	-0.5	-1	-0.5	-0.5

cycle D of the input switching signal at $Node_1$ increases the generated DC voltage.

Large tapered buffers are required in a conventional buck converter to drive the large output power transistors, which deliver current to the load circuitry. In the proposed circuit, however, the current delivered to the load circuitry is supplied by an operational amplifier. Small buffers are therefore sufficient for driving the active filter. Replacing the tapered buffers with smaller buffers significantly decreases the power dissipated by the input stage. Alternatively, the output buffers within the Op Amp dissipate power within the regulator. Another characteristic of the regulator is that the feedback required for line and load regulation is satisfied with separate feedback paths, as shown in Fig. 1. Feedback$_1$ is generated by the active filter structure and provides load regulation whereas feedback$_2$ is optional and controls the duty cycle of the switching signal for line regulation. In most cases, feedback$_1$ is sufficient to guarantee fast and accurate load regulation. When only one feedback path is used, the switching signal is generated by simpler circuitry (*e.g.*, a ring oscillator) and the duty cycle of the switching signal is compensated by a local feedback circuit (a duty cycle adjustor). The primary advantage of a single feedback path is smaller area since feedback$_1$ is produced by the active filter and no additional circuitry is required for the compensation structure.

Utilizing active filters within a switching voltage regulator to replace the passive LC filter was first proposed in [5], however, several important design issues such as the power efficiency, the sensitivity of the active filter, the output buffer stage of the Op Amp, and the type and topology of the active filter structure were overlooked. Additionally, the active filter-based regulator in [5] requires a 10 μF capacitor, which occupies significant on-chip area and is therefore inappropriate for point-of-load voltage regulation. Less than 8 pF capacitance is used within the active filter portion of the proposed voltage regulator for a cutoff frequency of 50 MHz.

A Sallen-Key active filter topology is used in the proposed circuit since the static power dissipation of this topology is lower than other low complexity active filters. A third order Chebyshev type I filter is chosen for the active filter due to the steep roll-off factor as compared to those filter structures which do not require resistive components connected to ground to produce finite zeros. The active filter passes the switching signal at a constant frequency and generates a DC output voltage. The per cent change in the cutoff frequency and the Q factor of the third order Sallen-Key filter are listed in Table I to analyze the sensitivity for an increase of 1% in the value of the individual parameters.

A three stage classical differential-input single-ended CMOS Op Amp structure is utilized in the proposed regulator, as shown in Fig. 2 [8]. The size of the transistors in the output stage is considerably larger than the first two stages to supply sufficient current to the load circuits. The first and second stages are gain stages which provide a cascaded gain of greater than 50 dB. The third stage exhibits a gain close to unity. The overall three stage gain is close to 50 dB with a phase margin of 51°.

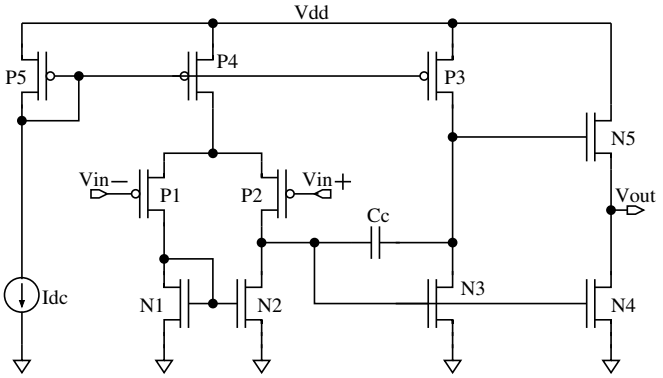


Fig. 2. Three stage Op Amp with PMOS input transistors. The PMOS input transistors are used in the first differential input stage. The second stage is a common-source gain stage and the third stage forms the output buffer that supplies the current to the load.

III. PROS AND CONS OF ACTIVE FILTER-BASED VOLTAGE REGULATOR

The proposed voltage regulator is a hybrid combination of a switching and linear voltage regulator and exhibits certain advantages and disadvantages from using a combination of a switching and LDO regulator topology.

Voltage regulation: The line and load regulation of the proposed voltage converter is separated into two different feedback paths, as shown in Fig. 1. The response time for abrupt changes in the load current is faster than a switching regulator and similar to an LDO regulator. The line regulation characteristics are, however, similar to a switching voltage regulator where the duty cycle of the input switching signal is altered by the pulse width modulator (PWM).

Stability: The stability of a buck converter is typically determined by the effective series resistance (ESR) of the output capacitor. A buck converter can be unstable when the ESR is too small due to a double pole formed by a second order LC filter. The proposed regulator uses an NMOS transistor at the output stage of the Op Amp with a low output impedance shifting the dominant pole at the output node to a higher frequency. During full load condition, *i.e.*, the effective load resistance is small, the stability is not significantly degraded due to the small effective output impedance. With an NMOS output stage, the proposed regulator is inherently stable since one of the poles is at a higher frequency. When the Op Amp within the proposed regulator is altered to provide a PMOS output stage to reduce the dropout voltage, the capacitors in the active filter structure (particularly C_2) maintain stability while reducing the size of any additional output capacitor. In

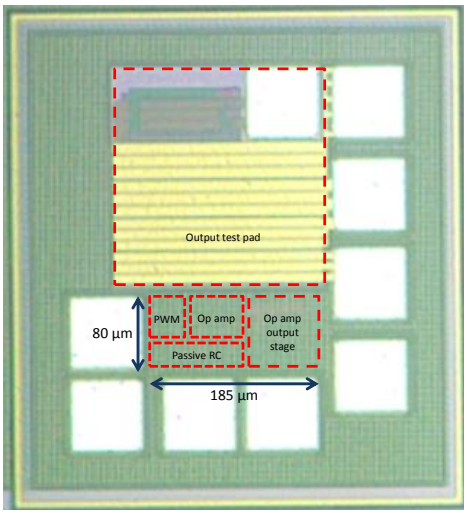


Fig. 3. Die microphotograph of the hybrid voltage regulator.

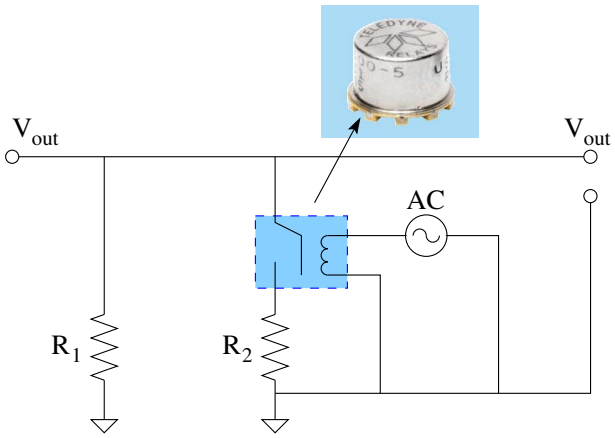


Fig. 4. Set-up for load transient testing of the voltage regulator. A Teledyne relay (GRF303 series) is used to switch the output current.

this manner, the stability of the proposed regulator is similar to an LDO but does not require a large output capacitor.

On-chip area: The physical area of the proposed regulator is smaller than both a switching and LDO voltage regulator since there is no large output capacitor. The frequency of the input switching signal can be increased without significantly degrading the power efficiency because the buffers delivering this switching signal can be small. With higher switching frequencies, the size of the proposed regulator can be further decreased. The primary advantage of the proposed regulator as compared to other regulator topologies is the small area requirement which is further reduced in highly scaled technologies without significantly degrading the power efficiency.

Power efficiency: The power efficiency of a buck converter can theoretically approach 100% when the parasitic impedances are ignored. For an LDO or the proposed regulator, the maximum attainable power efficiency is limited to V_{out}/V_{in}, as previously mentioned.

Maximum load current: The maximum current that can be delivered to the load depends upon the size of the power transistors driving the LC filter. A higher current can be delivered with larger power transistors. The maximum load current of an LDO regulator depends upon the size of the pass transistor. Similarly, the maximum load current of the proposed voltage regulator is determined by the size of the output stage of the Op Amp.

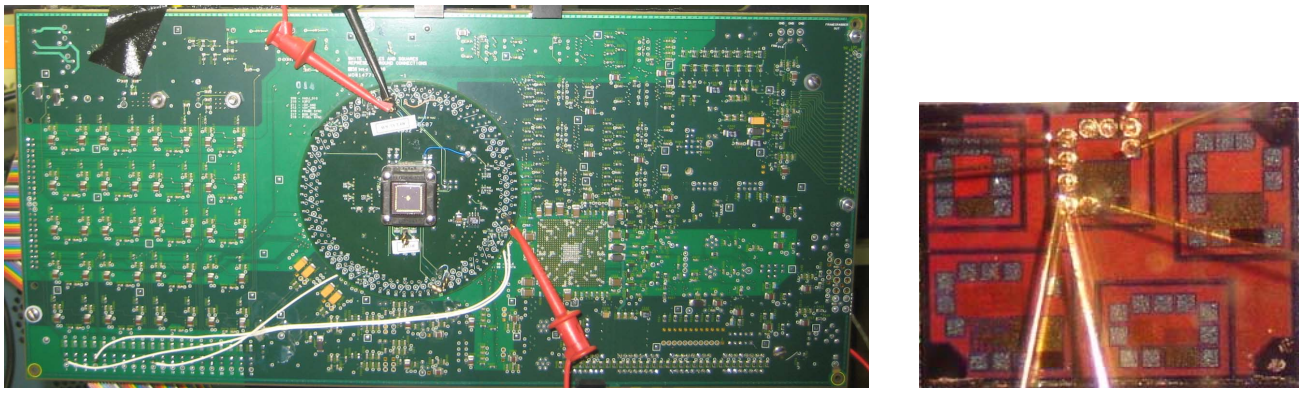
IV. Experimental Results

The proposed active filter based DC-DC voltage converter has been designed and fabricated in a 110 nm CMOS technology. The ultra-small voltage regulator is 0.015 mm^2. A significant portion of this area is allocated to the Op Amp, as shown in Fig. 3. The active filter is designed with a cutoff frequency of approximately 50 MHz. The 80 MHz input switching signal is sufficiently fast to filter out the high frequency harmonics within the input switching signal. An input switching frequency greater than 80 MHz increases the dynamic power dissipation. A ring oscillator supplies a 50% duty cycle switching signal to the input. Since there is no need for large tapered buffers, the power dissipated by the ring oscillator and output buffers is relatively small. The size of the transistors at the output stage of the Op Amp can be changed for different output voltage or load current demands. The on-chip area of the proposed regulator is therefore chosen depending on the specific output voltage and load current characteristics.

The on-chip area provides up to 80 mA and is 185 μm $\times$ 80 μm, as shown in Fig. 3. This on-chip area is significantly less than some recently proposed LDO regulators [9]–[12] and SC voltage regulators [13], [14], as listed in Table II. No capacitor is required at the output node to maintain stability and load regulation, making the proposed circuit convenient for point-of-load voltage regulation.

A Teledyne GRF303 relay, as shown in Fig. 4, switches the output current of the regulator. The test board and test circuit for load transient testing is illustrated, respectively, in Figs. 5a and 5b. The output current is varied between 5 mA to 70 mA while generating 0.9 volts. The transition time of the current transients is approximately 70 ns. When the output current demand transitions from 5 mA to 70 mA and 70 mA to 5 mA, the output voltage settles, respectively, in 72 ns and 192 ns. The experimental results are shown in Fig. 6a. A zoomed view of the rise and fall transitions of the output voltage is illustrated, respectively, in Figs. 6a and 6b. Note that no ringing or overshoot in the output voltage occurs during transient operation, exhibiting highly stable operation of the voltage regulator with abrupt changes in the output current demand.

The hybrid voltage regulator dissipates 0.38 mA quiescent current and delivers up to 80 mA current while generating 0.9 volts from a 1.8 volt input voltage. The current efficiency is over 99% when the output current demand is greater than 40 mA. When the output current demand changes, a DC voltage shift occurs in the generated voltage. This DC voltage shift at the output of the regulator is 44 mV, as shown in Fig. 7. When the output current varies between 5 mA and 70



(a) (b)

Fig. 5. Setup for the test circuit; a) test board, and b) test circuit with wirebonds.

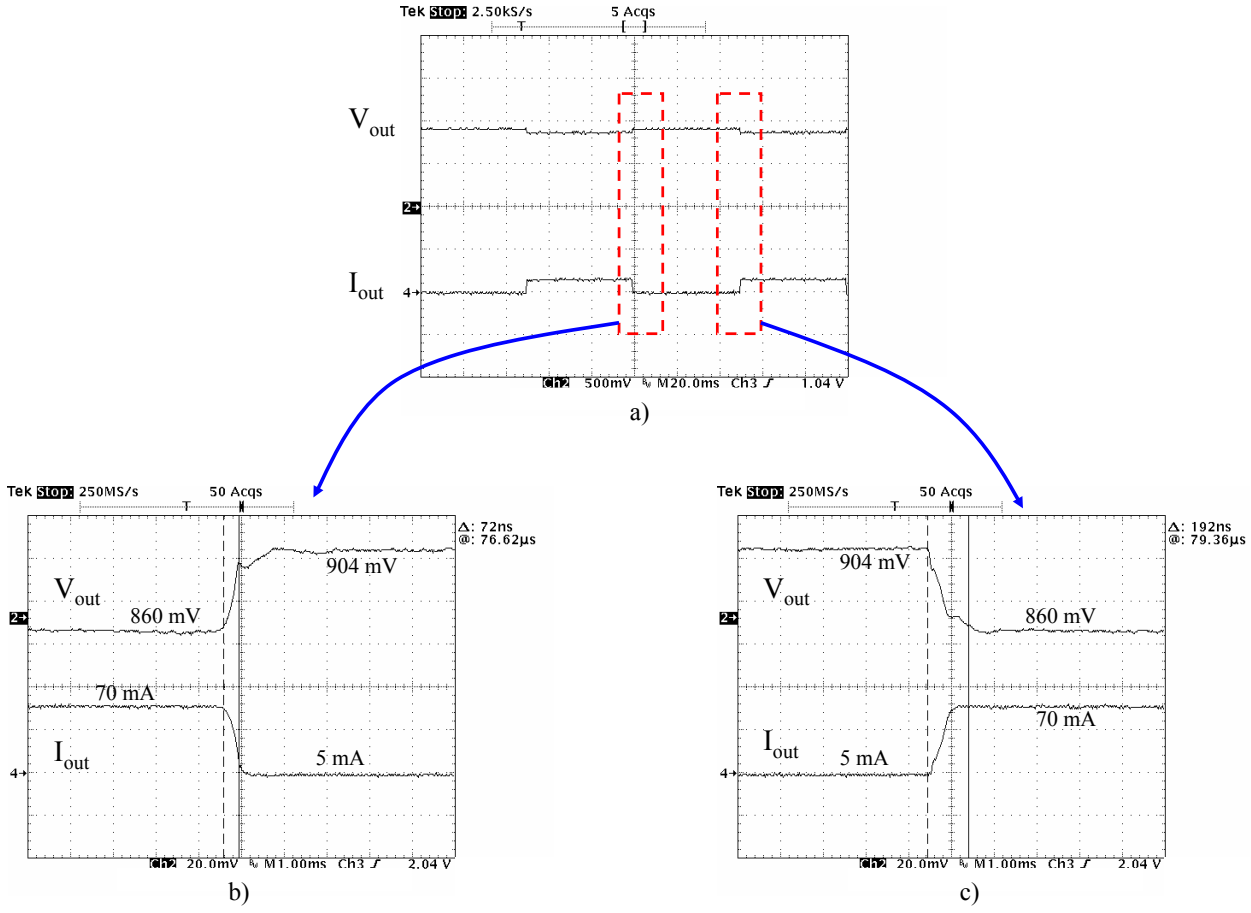


Fig. 6. Measured transient response of the active filter based voltage regulator a) the output current changes from 5 mA to 70 mA, and a zoomed view of the transient response for the output current changing from b) 70 mA to 5 mA, and c) 5 mA to 70 mA. The transition time for the output current is 70 ns.

mA, a load regulation of 0.67 mV/mA is exhibited. With a 52% increase in voltage regulator area (*i.e.*, utilizing a larger output buffer), the load regulation is reduced to ~ 0.17 mV/mA, a four fold decrease in the DC voltage shift at the output voltage. Measurement of the load regulation characteristics of the regulator is illustrated in Fig. 8.

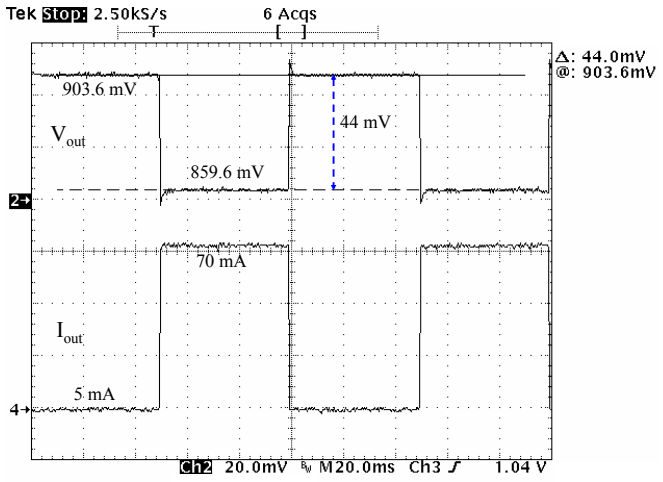


Fig. 7. Measured load regulation when the transient output current changes between 5 mA and 70 mA. The output DC voltage shift is 44 mV. The transition time of the output current is approximately 70 ns.

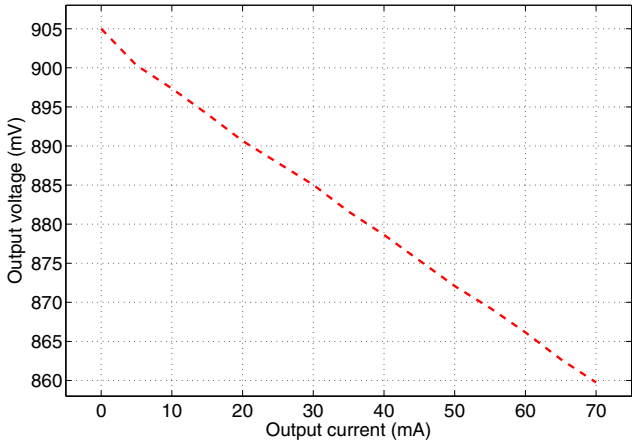


Fig. 8. Measured load regulation of the proposed circuit is approximately 0.67 mV/mA.

A performance comparison of the proposed circuit with other switching and linear DC-DC converters is listed in Table II. The on-chip area required by the proposed circuit is significantly less than previously proposed state-of-the-art buck converters [15], [16], LDO [9]–[12], [17]–[19], and SC voltage regulators [13], [14].

A figure of merit (FOM) is proposed by Guo *et al.* in [12] as

$$\text{FOM}_{guo} = K\left(\frac{\Delta V_{out}\cdot I_Q}{\Delta I_{out}}\right) \qquad (V), \tag{1}$$

where K is

$$K = \frac{\Delta t \text{ used in the measurement}}{\text{Smallest } \Delta t \text{ among the compared circuits}}, \tag{2}$$

and Δt is the transition time of the load current during test. FOM_{guo} however does not consider the speed of the load regulation which is a primary issue in point-of-load voltage regulation.

A second FOM is therefore proposed that considers the response time and on-chip area of a voltage regulator,

$$\text{FOM}_1 = K\left(\frac{\Delta V_{out}\cdot I_Q}{\Delta I_{out}}\right)\cdot R_t\cdot A \qquad (V\ \mu sec\, mm^2), \tag{3}$$

where R_t and A are, respectively, the response time and area of a voltage regulator. Since the required area is technology dependent, the fabrication technology can also be included in the FOM_1, assuming a linear reduction in area with technology.

$$\text{FOM}_2 = K\left(\frac{\Delta V_{out}\cdot I_Q}{\Delta I_{out}}\right)\cdot\frac{R_t\cdot A}{T} \qquad (V\ \mu sec), \tag{4}$$

where T is the technology node.

A smaller FOM_1 and FOM_2 of a voltage regulator is a better choice for point-of-load voltage regulation. The regulator described in [11] exhibits the smallest FOMs; however, the response time of [11] is not a measurement result but originates from a mathematical analysis. The voltage regulator presented in this paper exhibits the smallest FOM among all of the remaining circuits despite the comparably high quiescent current (I_Q). By reducing I_Q, the FOM for the proposed regulator can be further reduced.

The primary disadvantage of the proposed circuit is that the power efficiency is limited to V_{out}/V_{in} as in a linear voltage regulator. This power loss, however, is somewhat compensated by replacing the large tapered buffers with smaller buffers which drive the active filter. Additionally, the filter inductor and capacitor related power losses are eliminated by the active filter structure. The primary advantage of the proposed regulator is smaller on-chip area. Considering the target application of distributed multi-voltage on-chip power supplies, where the local voltage differences are relatively small, this circuit provides an effective tradeoff between physical area and power efficiency.

V. Conclusions

An active filter based on-chip DC-DC power supply appropriate for point-of-load voltage regulation is proposed in this paper. The on-chip area of the proposed fully monolithic hybrid voltage regulator is 0.015 mm^2 and provides up to 80 mA output current. The load regulation is 0.67 mV/mA and the response time ranges from 72 ns to 192 ns. The area of the proposed regulator is significantly less than previously proposed state-of-the-art buck converters, LDOs, and SC voltage regulators despite a mature 110 nm CMOS technology. The area of the proposed regulator will therefore be significantly smaller with more advanced technologies. The need for an off-chip capacitor or advanced on-chip compensation techniques to satisfy stability and performance requirements is eliminated in the proposed circuit. This circuit therefore provides a means for distributing multiple power supplies close to the load to reduce power/ground noise while enhancing circuit performance by delivering a high quality supply voltage to the load circuitry. With the proposed voltage regulator, on-chip signal and power integrity is significantly enhanced while

TABLE II

PERFORMANCE COMPARISON AMONG DIFFERENT DC-DC CONVERTERS.

	[15]	[20]	[11]	[9]	[10]	[12]	[13]	[14]	This work
Year	2003	1998	2005	2007	2008	2010	2010	2010	2010
Type	Buck	LDO	LDO	LDO	LDO	LDO	SC	SC	Hybrid
Technology [nm]	80	500	90	350	350	90	45	32	110
Response time [ns]	87[a]	150,000	0.054[b]	270	300	3000-5000	120-1200	N/A	72-192
On-chip area [mm^2]	12.6	1	0.098	0.264	0.045[c]	0.019	0.16	0.374	0.015
Output voltage [V]	0.9	2-3.6	0.9	1.8-3.5	1	0.5-1	0.8-1	0.66-1.33	0.9
Input voltage [V]	1.2	5	1.2	2-5.5	1.2	0.75-1.2	N/A	N/A	1.8
Maximum current [mA]	9500	300	100	200	50	100	8	205	80
Maximum current efficiency	N/A	99.8	94	99.8	99.8	99.9	N/A	N/A	99.5
ΔV_{out} [mV]	100	300	90	54	180	114	N/A	N/A	44
Quiescent current [mA]	N/A	10-750	6	0.02-0.34	0.095	0.008	N/A	N/A	0.38
Load regulation [mV/mA]	0.014[a]	0.5	1.8	0.27	0.28	0.1	N/A	N/A	0.67
Transition time [ns]	N/A	N/A	0.1	100	~150	100	N/A	N/A	70
Transition time ratio (K)	N/A	N/A	1	1000	1500	1000	N/A	N/A	700
FOM$_1$=$K\left(\frac{\Delta V_{out}\cdot I_Q}{\Delta I_{out}}\right)\cdot R_t\cdot A$	N/A	N/A	0.029[b]	6.544	6.926[c]	0.893	N/A	N/A	0.518
FOM$_2$=$K\left(\frac{\Delta V_{out}\cdot I_Q}{\Delta I_{out}}\right)\cdot \frac{R_t\cdot A}{T}$	N/A	N/A	3.6[b]	53.4	56.5[c]	110.2	N/A	N/A	42.8

[a] Simulation results (not experimental data).

[b] Mathematical analysis (not experimental data).

[c] An off-chip capacitor of 1 nF to 10 μF is required.

providing the capability for distributing multiple point-of-load power supplies.

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