Optimizing Inductive Interconnect for Low Power

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Abstract: The width of an interconnect line affects the total power consumed by a circuit. A trade off exists between the dynamic power and the short-circuit power dissipated in inductive interconnect. The optimum line width that minimizes the total transient power dissipation is determined in this paper. A closed form solution for the optimum width with an error less than 5% is presented. For a specific set of line parameters and resistivities, a reduction in power approaching 78% is achieved as compared to the minimum wire width. Considering the driver size in the design process, the optimum wire and driver size that minimizes the total transient power is also determined.

Keywords: transient power dissipation,inductive interconnect, underdamped systems, short-circuit power, characteristic impedance, dynamic power

1. INTRODUCTION

As the feature size of CMOS circuits and wiring has decreased, interconnect design has become an important issue in high speed, high complexity integrated circuits (IC). With the increase in signal frequencies and the corresponding decrease in signal transition times, the interconnect impedance can behave inductively [1], increasing the on-chip noise. Furthermore, considering inductance within the design process increases the computational complexity of IC synthesis and analysis tools. However, inductive behaviour can also be useful. As shown in [3], a properly designed inductive line can reduce the total power dissipated by high-speed clock distribution networks. Clock networks can dissipate a large portion of the total power dissipated within a synchronous IC, ranging from 25% to 75 %[4,5]. The technique proposed here can be used to reduce the overall power being dissipated by long interconnect such as a high-speed clock distribution network or data buss.

Many algorithms have been proposed to determine the optimum wire size that minimizes a cost function such as delay [6] or power. Some of these algorithms address reliability issues by reducing clock skew. The work described in [7] considers simultaneous driver and wire sizing using the Elmore delay model with simple capacitance, resistance, and power models. As the inductance becomes important, certain algorithms have been enhanced to consider an RLC model [8].

In this paper, the tradeoff between short-circuit and dynamic power in inductive interconnect is introduced. The optimum line width that minimizes the total power dissipation is determined. As the line driver has an important effect on the signal and power dissipation characteristics, a closed form solution for the simultaneous driver and wire-sizing problem that minimizes the total transient power dissipation is presented. An analytical solution for the transition time at the far end of a long inductive interconnect is also provided. These results are used to determine a closed form solution for the width of an inductive interconnects line that minimizes the power dissipated by that line.

The paper is organized as follows. In section 2, the transient power characteristics of inductive interconnect line are discussed. The signal behaviour at the end of an inductive line is described in section 3. In section 4, a power optimization criterion is formulated. The effect of line material and length on the optimum interconnect width is demonstrated in section 5. Some conclusions are discussed in section 6.

2. POWER CHARACTERISTICS OF INDUCTIVE INTERCONNECT

The transient powers characteristics of inductive interconnect are presented in this section. The research described [3] uses wire sizing techniques to reduce the total transient power dissipated by a clock distribution network, but does not provide a closed form solution to determine the optimum interconnect width. Their model also ignores the change in the circuit behavior that occurs when the width of the line is increased. The matching response between the line and the driver plays an important role in the transient power dissipation as discussed in section 3. In [3], the driver size is also not considered as a design parameter.

Issues that affect wire sizing are discussed in this section. In subsection 2.1, the trade off between dynamic and short-circuit power dissipation in inductive interconnect is described. A lossy transmission line model used in the development of a closed form solution for the interconnect width that minimizes the total transient power is presented in subsection 2.2. Simultaneous wire and driver sizing criteria are described in subsection 2.3.

2.1 Transient Power in Inductive Lines

A trade-off exists between dynamic and short-circuit power in sizing inductive interconnect. As shown in Fig1, an optimum interconnect width at

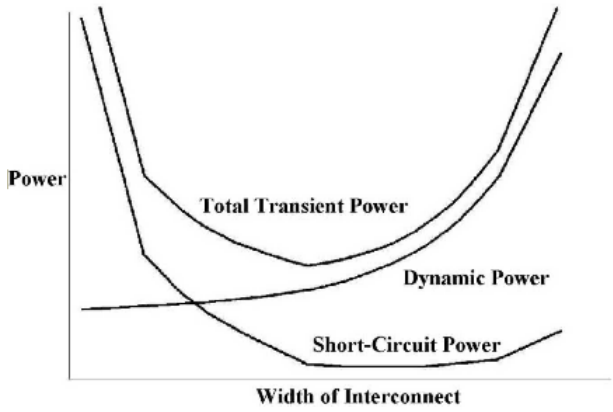


Figure.1: Dynamic, short-circuit, and total transient power as a function of the connect line width

which the total transient power is a minimum exists for overdriven lines. This trade off does not occur if the line is under driven, as described in section 3.

Transient power dissipation is composed of dynamic power and short-circuit power [2]. For the circuit shown in Fig. 2, both Inv1 and Inv2 dissipate transient power during switching. The change in the line width primarily affects the dynamic power of Inv1.P1d and the short-circuit power of Inv2 P2sc Closed form expressions for the dynamic and short-circuit power are given by (1) and (2), respectively [9]. The dynamic power of Inv2 depends on the load capacitance, and is not affected by the wire size. The change in the short-circuit power of Inv1 is negligible, assuming a fixed signal transition time at the input of Inv1

$$P_{id} = f V_{dd}^2 C, \quad (1)$$

$$P_{2sc} = f (1/12) k_2 \tau_o (V_{dd} - 2 V_{t2})^3 \quad (2)$$

Where f is the operating frequency, C1 is the total capacitance driven by Inv1, K_2 and V_{t2} are the trans conductance and threshold voltage of Inv_2, respectively, and τ_o is the transition time of the signal at the input of Inv_2.

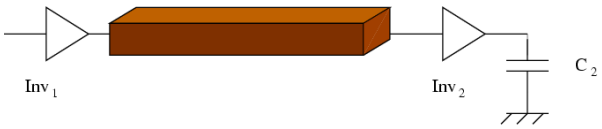


Figure.2: CMOS inverter driving another inverter through a long interconnect line

Only C_1 and τ_0 are affected by a change in the line width. Changing the line width has a significant effect on the transition time, as described in section 3. To determine the optimum width, closed form expressions for both C_1 and τ_0 are provided in subsections 2.2 and 3.1, respectively.

2.2 Transmission Line Model

To obtain a closed form solution for the optimum width, expressions for the line impedances which model the interconnect are presented. Neglecting the line dielectric losses, a lossy transmission line is represented by the line resistance R, inductance L, and capacitance C, all per unit length. R, L, and C are expressed in terms of the line dimensions in (30-(5) respectively.

$$R = \rho / W_{int\,T} \qquad (3)$$

where ρ,T and W_{int} are the line resistivity, thickness, and width, respectively. Assuming a single line, C is given by [16]

$$\frac{C}{\in_{ox}} = 1.13\frac{W_{INT}}{H} + 1.44\left(\frac{W_{INT}}{n}\right)^{0.11} - 1.47\left(\frac{T}{H}\right)^{0.42} \qquad (4)$$

Note that C increases super linearly with the line width, which increases the dynamic power $P_{1d.}$ L is the self-inductance of the line and is given by [12]

$$L = 200\left(\ln\left(\frac{2l}{W_{INT}+T}\right) + 0.5 + 0.22\frac{W_{INT}+T}{l}\right) \qquad (5)$$

The self-inductance decreases with increasing line width. Note that the line inductance may increase if the total area of the interconnect is fixed, since the mutual inductance can increase with smaller line-to-line spacing. For a single line, however, the interconnect inductance decreases with increasing width.

The inductive time constant of a line can be characterized by $\sqrt{}$ l/R [10].

This time constant increases with increasing line width, as the reduction in resistance is much greater than the reduction in the inductance. An increase in the inductive time constant and line capacitance affects the transition time as described in section 3.

2.3 Simultaneous Wire and Driver Size

The geometric width of the driver also plays an important role in the total transient power dissipation. Two complementary effects occur. As the driver size increases, the transition time of the output signal decreases and, consequently, the short-circuit power of the load gate decreases. At the same time, the driver gate input capacitance increases as the width of the driver becomes larger, increasing the power required to charge the gate capacitance. A general expression for the total transient power dissipation including the power dissipation due to the driver input gate capacitance is

$$P_{tdrive} = P_{id} + P_{2sc} + P_{drive} \tag{6}$$

Where $P_{drive} = f V_{dd}^2 C_{drive}$ and C_{drive} is the driver gate input capacitance.
Equation (6) is therefore a function of both the wire width and the driver size.
To achieve the global minimum for the transient power dissipation, both of these design variables need to be simultaneously determined.

3. TRANSITION TIME FOR A SIGNAL AT THE FAR END OF AN INTERCONNECT LINE

Wire sizing techniques do not consider line-matching characteristics as the line width changes. For inductive interconnect, the matching response plays an important role in the signal characteristics. It is shown in this section that, for an under driven line, the transition time increases as the line becomes wider. A closed form expression of the signal transition time at the far end of a line is presented in subsection 3.1.The effect of wire sizing on the line matching characteristics and the transition time is described in subsection 3.2.

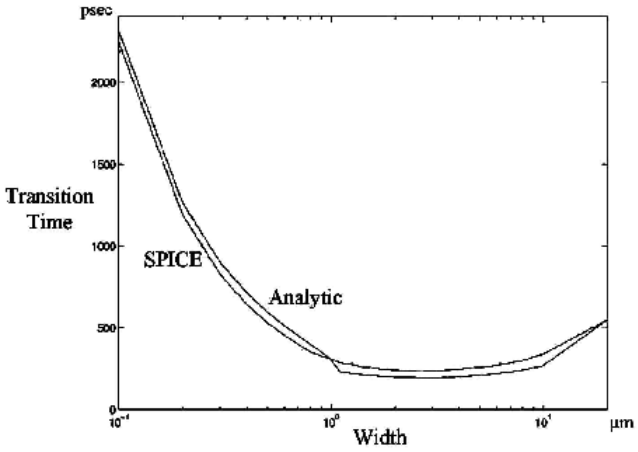
3.1 CLOSED FORM EXPRESSION FOR THE TRANSITION TIME

To determine a closed form expression for the high-to-low signal transition time at the far end of an inductive interconnect line, a lumped RLC equivalent circuit is used to

model the interconnect impedance [2]. Assuming the PMOS transistor of the driving inverter is off, an analytical expression for the signal at the far end of the line is

$$V(t)= V_c (\tau_p OFF) e^{- \alpha n(t- \tau p \ off)} \quad (7)$$

Where $\tau_p OFF$ is the time at which the PMOS transistor of the driver turns off, and α_n is a constant that depends upon R , C, L, and the driver transistor characteristics such as the transconductance, mobility, and threshold voltage. $V_c (\tau_p OFF)$ is the voltage at the load capacitance at $\tau_p OFF$. The transition time is expressed by $\tau_0 = t_{10\%} - t_{90\%}$ where $t_{10\%}$ and $t_{90\%}$ are the times at which the signal reached 10 % and 90% of the final value, respectively.The transition time based on this analytical expression is compared to SPICE in Fig. 3



Figur.3: Analytical solution of the trasistion time as compared with SPICE for different line widths

The values of R, C and L are determined from (3) –(5) based on H = 2 μm, T =2μm , ρ= 2.5 μΩcm and l= 5 mm. A 0.24μm CMOS inverter with W_n = 15 μm and W_p = 30 μm is assumed.The maximum error in the analytical expression as compared to SPICE is less than 20% and is typically around 14%.

As shown in Fig3, as the line width increases, the signal transition time decreases until a minimum transition time is reached. The signal transition time increases again after exceeding a certain line width. The behavior of the transition time in terms of the line impedances is described in the following section.

3.2 EFFECTS OF CHANGING THE INTERCONNECT WIDTH ON THE LINE CHARACTERISTICS

To describe the signal behavior in terms of the interconnect width, an equivalent circuit of an inverter driving an inductive interconnect line is used. The characteristic impedance of a lossy line is given by the well-known formula $Z_{lossy} = \sqrt{R + jwL/ jwC}$. The input signal driving the line is assumed to be a ramp signal. Different approximations have been made to estimate Z_{lossy} in terms of the per unit length parameters [14,15]. A general form for Z_{lossy} is $Z_o + g R$ where g is a constant which depends on the line parameters.

For the high-to-low input transition, the NMOS transistor is assumed to be off. The inverter can be replaced with an ideal voltage source with a variable output resistance R_{tr} as shown in Fig 4.

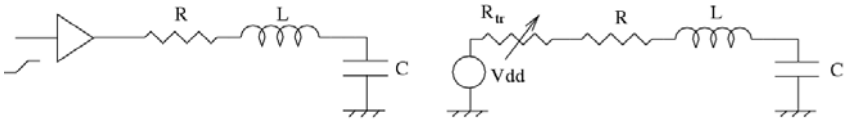


Figure.4: Equivalent circuit of an inverter driving an *RLC* interconnect line

At small interconnect widths; the characteristic line impedance is large as compared to the equivalent output resistance of the transistor. Thus, the line is overdriven and the waveform at the far end of the line contains overshoots and undershoots (the under damped condition).Z_{lossy} decreases with increasing line width, and the line remains under damped until Z_{lossy} equals R_{tr}.. A further increase in the line width under drives the line, as Z_{lossy} becomes less than R_{tr} [13]. As the line width is increased, the line driving condition changes from overdriven to matched to under driven.

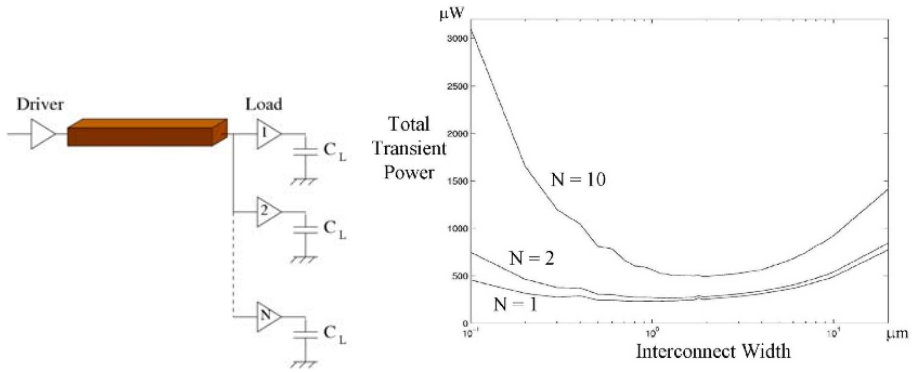
For an overdriven line, increasing the line width makes the line more inductive as the resistance decreases linearly while the inductance has a logarithmic dependence on the width (for a single line). As described in [3] , the line impedance approaches becoming lossless, and the attenuation constant approaches zero at large line widths. This effect reduces the signal transition time. A further increase in the line width decreases Z_{lossy} and matches the line impedance with the driver impedance. At this width, the transition time reaches a minimum, as shown in Fig 3.Increasing the width further under drives the line. At this width, the capacitance begins to dominate the line impedance. The line becomes highly capacitive which further increases the transition time, increasing the short-circuit power dissipation in the load inverter. For an overdriven line, the short-circuit power dissipation changes with the line width as shown in Fig. 1. However, for an under driven line, an increase in the line width increases the short-circuit power. If the line is under driven, the line should be made as thin as possible to minimize the total transient power.

4. INTERCONNECT WIDTH OPTIMIZATION FOR MINIMUM POWER

Using the closed form expressions for C and τ_o, the transient power components can be expressed in terms of the line width. A criterion for determining the optimum interconnect width is applied in this section to a simple example circuit and compared with SPICE.

The dynamic power of a driver increases with the interconnect width as the line capacitance increases. The short-circuit power within the load gate decreases as the line becomes wider (more inductive). When the width reaches the matched condition, the short-circuit power is minimum. An increase in the interconnect width beyond the matching condition increases the short-circuit power, since the transition time increases (see Fig. 3). For an inverter driving N gates, as shown in Fig. 5a, the total transient power is given by

$$P_{tDrive} = P_{tDrive} + N P_{2sc} + P_{drive}$$



(a) (b)

Figure.5: Inverter driving N logic gates, a0 circuit structure, b0 total transient power dissipation as determined by SPICE

For a specific driver size, the total transient power dissipation is a function of the line width. Given a set of line parameters, the optimum line width can be obtained by determining the interconnect width which minimizes P_{tDrive}. For circuit specifications as described in subsection 3.1, the total simulated power dissipation for different loads, N = 1,2,and 10, is shown in Fig. 5b. A comparison between the analytic solution and simulation is listed in Table 1. The error between the analytic solution and SPICE for the chosen range of values is less than 5%.

Number of Loads N	$W_{INT\ Optimum}$ (μm)		Error (%)
	Analytical	SPICE	
1	1.08	1.10	-1.9
2	1.13	1.15	-1.8
10	1.99	1.90	+4.8

For N = 10, the total transient power dissipation of a symmetric driver is shown in Fig6. Considering the driver size as a design variable, a different local minimum for the transient power dissipation exists for each driver size. Furthermore, for each line width, a minimum transient power dissipation also exists for each driver size. A global minimum for the transient power is obtained by determining the optimum value of each design variable. Considering the driver size as a design parameter, (8) is a function of two variables, permitting the global minimum for the power dissipation to be obtained. For the example circuit shown in Fig. 5a, the minimum power is achieved at W_{INT}= 2.8 μmand W = 57 μm .

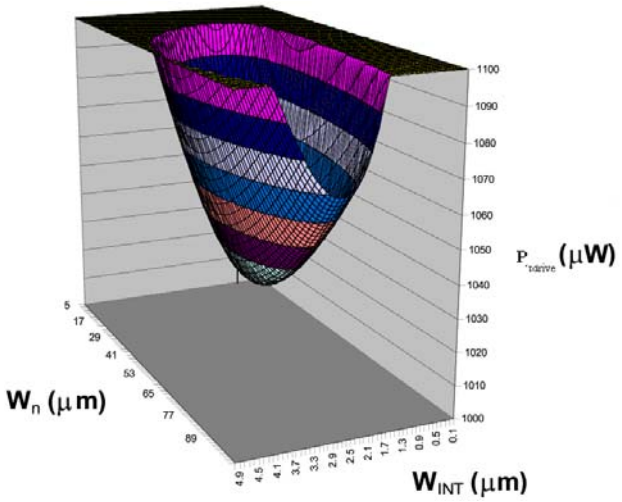


Figure.6: Total power dissipation with different wire and driver sizes where N=10.

5. EFFECTS OF INTERCONNECT RESISTIVITY AND LENGTH ON POWER

To evaluate the effectiveness of the optimum solution, different interconnect line parameters are considered. To demonstrate the importance of the optimum solution

on inductive lines, the optimum width is obtained for two line lengths, l = 1mm and 5 mm. The transient power dissipation is determined for three line widths, thin, optimum, and wide. As listed in Table 2, the optimum width of a copper line reduces the total transient power by 68.5% for l = 5 mm as compared to 28.6% for l = 1 mm. For aluminium, a reduction of 77.9% is achieved as compared to 37.8%. As the line become longer (i.e. more inductive), the power decreases further. The more inductive the interconnect, the more sensitive the power dissipation is to a change in the line width. Wire width optimisations is, therefore, more effective for longer inductive lines.

Also listed in Table 2 is that the power reduction in aluminium is greater than that in copper. The reduction in power in these inductive lines increases further as the lines become more resistive (see, for example, aluminium lines versus copper lines in Table 2.)Comparing the optimum width with the minimum width, the reduction in power is greater in more highly resistive lines.

Resistivity ρ μΩcm	Total Transient Power Dissipation (μW)				
	Resistive line(I=1 mm)				
	Optimum	Thin	Reduction	Wide	Reduction
1.7 (copper)	583	817	28.6%	880	33.8%
2.5(Aluminium)	606	976	37.8%	813	25.4%
	Inductive Line(I=5 mm)				
1.7 (copper)	1121	3563	68.5%	1931	41.9%
2.5(Aluminium)	1236	5592	77.9%	1973	37.4%

6. CONCLUSION

It is shown in this paper that a trade off exists between the dynamic and short-circuit power in inductive inter connect. The short-circuit power of an overdriven interconnect line decreases with the line width, while the dynamic power increases. When the line exceeds the matched condition, the short-circuit power also increases with increasing line width. For a long inductive interconnect line, an optimum interconnect width exists that minimizes the total transient power dissipation. A closed form solution is presented for determining this optimum width. This solution has high accuracy, producing an error of less than 5%. The optimum line width is shown to be more effective in reducing the total transient power as the line becomes longer. With aluminum interconnect, a reduction in power of about 80% and 37% is obtained as compared to thin and wide wires, respectively. For copper interconnect, a reduction in power of 68% and 42% is obtained for the same conditions. Greater power reduction is achieved for optimally sized lines with higher resistively as compared to minimum

width lines. The optimum interconnect width depends upon both the driver size and the number of gates being driven. With this solution, the optimum driver and wire size can be simultaneously determined.

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