A Universal CMOS Voltage Interface Circuit

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Abstract— **A CMOS interface circuit to transfer a digital signal between two circuits of different supply voltages is described. The interface can be used, for example, between 3 volt and 5 volt or higher voltage families. The principal characteristics of the interface circuit are: no static power dissipation, high speed, and high speed buffering [1].**

I. Introduction

Over the past decade, CMOS has become the dominant semiconductor technology. Today, practically all high performance digital circuits are based on CMOS. When scaling a CMOS technology, the supply voltages are decreased to control the magnitude of the electric fields inside the transistors. In addition to controlling the velocity of the electron flow, another beneficial aspect of voltage scaling is a quadratic decrease in dynamic power dissipation with supply voltage as expressed by $P_D = C_L V_{DD}^2 f$. However, a tradeoff occurs, since decreasing the power supply also decreases the circuit speed. As a consequence, different circuit blocks operating at different power supplies are often found in modern processors, such as high speed blocks operating at 5 volts for the critical paths, while the rest of the processor operates at 3.3 volts. Multiple on-chip power supplies are also found in other circuit families such as in mixed-signal circuits. Another less critical requirement is to provide a voltage interface between different families of integrated circuits.

Therefore, high performance interfaces are frequently necessary. The signal transfer between low-to-high voltage levels and high-to-low voltage levels has to be performed with minimum delay and power in order to maintain any advantages obtained from using multiple power supplies. The proposed interface circuit fulfills these requirements while also providing no practical limitations on the magnitude of the voltage levels of the two CMOS families as well as maintaining the same circuit configuration and transistor sizes for both the low-to-high and high-to-low voltage interfaces.

A detailed description of the operation of the proposed interface circuit is presented in Section II. Some sizing considerations for the interface circuit are summarized in Section III. Simulation results and performance characterization of the interface circuit are described in Section IV. Finally, some conclusions are presented in Section V.

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II. Operation of the Interface Circuit

A classical CMOS interface circuit for converting a low voltage (*e.g.,* 3 V) signal into a high voltage (*e.g.,* 5 V) signal is shown in Fig. 1. If Out1 is low,

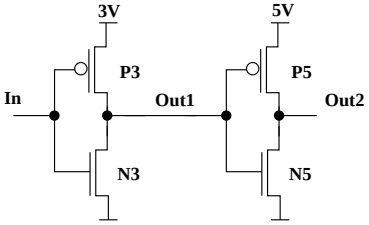

Fig. 1. A classical interface between a low voltage and a high voltage CMOS family.

P5 is on, N5 is off, and Out2 is high. If Out1 is high, both P5 and N5 are on. To make Out2 go low, N5 must have a higher transconductance than P5. Significant static power dissipation is therefore generated during the time Out1 is high. A small P5, however, affects the low-to-high transition of Out2, increasing this transition time. Different interface circuits have been developed to solve these problems and provide an efficient interface [2–6].

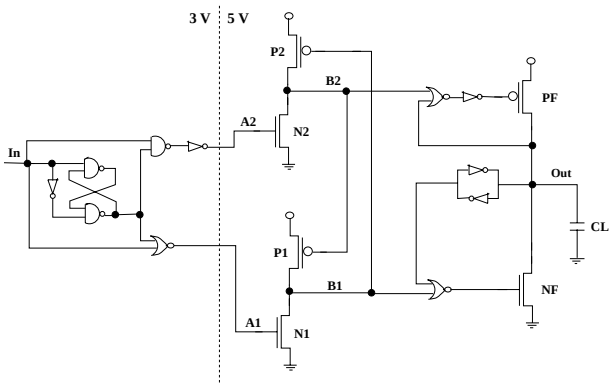

Fig. 2. Schematic of the proposed CMOS voltage interface circuit.

A schematic of the proposed interface circuit for a 3 V to 5 V interface is shown in Fig. 2. Note the 3 V – 5 V demarcation line. A1 is high when In is low and A2 is high when In is high. A1 and A2 are latched and in an alternate state for each input transition.

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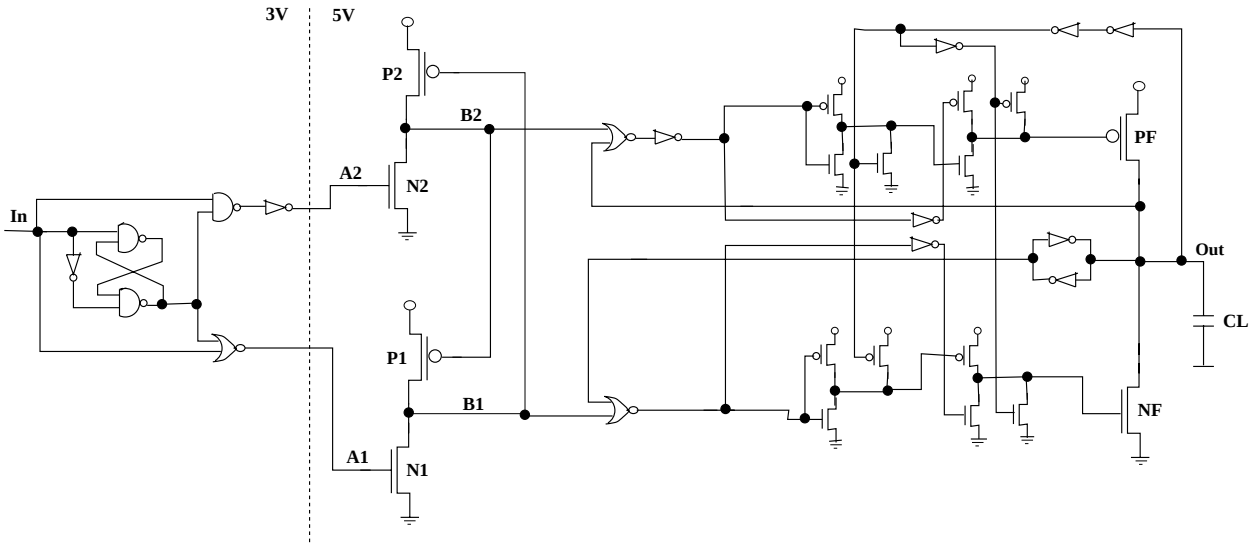

Fig. 3. Schematic of the proposed CMOS voltage interface circuit with a three stage output HD buffer-like circuit

Accordingly, the 3 volt block acts as a single input – two output converter. Note that A1 and A2 drive two NMOS transistors, N1 and N2. B1 is low when In is low and B2 is low when In is high. Using the nulling transistors and nulling process concept [1], P1 and P2 are the nulling transistors for N1 and N2 through the feedback paths B1–P2 and B2–P1. Briefly (see [1]), the nulling transistors restore the initial state of the internal nodes of the buffer without loading the signal path, permitting higher speeds and lower power dissipation to be realized as compared to other techniques used to drive a capacitive or RC load. For a specific stage of the buffer, the nulling transistors are separated from the signal path and are sized smaller than the corresponding output drive transistor of the related stage. The maximum time allocated for the nulling process of one stage is $t_{null} \approx T/2k$, where T is the period of the input signal of the buffer assuming a 50% duty factor, and k is the number of stages of the buffer.

Returning to the interface circuit, if In is low, A1 is high, N1 is on, N2 is off, B1 is low, P1 is off, P2 is on, and B2 is slowly pulled high due to the nulling process. P1 and P2 are sized smaller than N1 and N2 according to the nulling requirements [1]. Note that at this point, the 3 V to 5 V interface has been completed. The 3 volt input converter provides non-overlapping A1 and A2 outputs to eliminate any static power dissipation and to provide glitch-free operation. If A1 is high, B2 shifts high and B1 shifts low. A1 and A2 are non-overlapping, so A1 and A2 are both low before A2 becomes high. To increase the time during which both A1 and A2 are low, a supplemental non-inverting delay, not shown in Fig. 2, is inserted between In and the latch input.

When A2 is high, B2 becomes low, beginning the nulling process of B1. At this point, B1 is low, B2 is low, N1 is off, P1 is on, N2 is on, and P2 is on. Note that until B1 is nulled, the P2–N2 path dissipates a power similar to a short-circuit power [7, 8] (which becomes zero when the transition is completed). A similar action occurs for the P1–N1 path during the high-to-low input transition. Versions of this circuit exist that eliminate this small short-circuit current, but the additional hardware dissipates more power than is saved.

The high-to-low transition of B1 and B2 is fast, while the low-to-high transition of both the B1 and B2 outputs is slow, the current being sourced by the small nulling transistors, P1 and P2, respectively. To improve the speed of the low-to-high transition, an HD buffer-like circuit structure [1] is used with B1 and B2 as inputs. A one stage buffer is shown in Fig. 2, while in Fig. 3, a three stage buffer is shown.

The signals that require an interface typically also require buffering. The proposed interface circuit also provides a high speed buffering capability. Note in Fig. 2 that the fast high-to-low transition of B2 generates a low-to-high output transition through the PF transistor while NF is off, and the fast high-to-low transition of B1 generates a high-to-low output transition through the NF transistor while PF is off. Also note that due to the output feedback connections to the two NOR gates, the NF (PF) transistor is on only during the B1 (B2) transition until the output transition is completed. For the remaining time, similar to the HD buffer [1], NF and PF are off. As for the HD buffer, a small latch on the output is required to maintain the output state.

III. Sizing considerations

All the gate elements of the input converter are minimally sized. N1 and N2 are equal in size. N1 and N2 represent a standard load equivalent to a tapering factor of $e = 2.7$ [9, 10] for a minimum sized inverter ($W_{N1} = W_{N2} \approx 11$ x W_{min}). P1 and P2 are sized to

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complete the nulling process in less than the output buffer delay, avoiding output glitches [1].

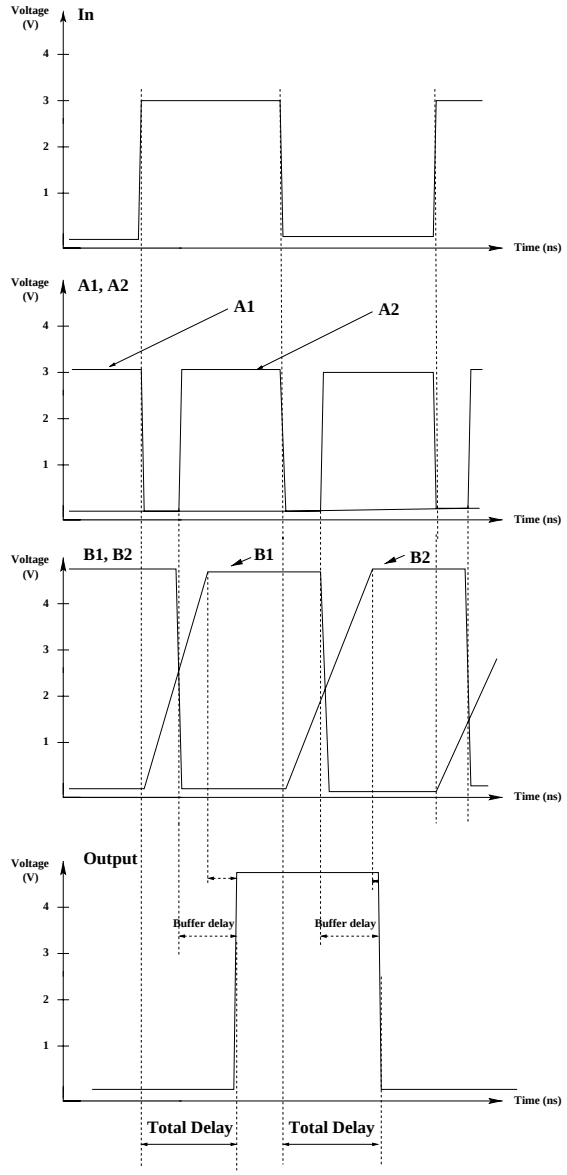

Fig. 4. Waveforms for the typical operation of a 3 V to 5 V interface.

Consider A2 high. The buffer pulls the output high through PF (see Fig. 2). If P1 does not complete the nulling process of B1 before the output signal transition is completed, the high output turns on NF through the feedback loop (both inputs of the NF NOR gate are low), creating a glitch on the output as well as a DC path between NF and PF. Typically P1 (P2) is smaller or the same size as N1 (N2), providing up to one third the transconductance of N1 (N2). P1 (P2) must therefore be properly sized to complete the nulling process of B1 (B2).

The two NOR gates at the input of the buffer are sized to a load equivalent to a tapering factor of $e = 2.7$ [9, 10] for N1 and N2. The remaining transistors are sized in a similar way as the HD buffer [1]. For a low-to-high voltage interface, V_{OH} of the low voltage circuit must be larger than V_T of N1 and N2. For a high-to-low voltage interface (for example 5 V to 3 V), N1 and N2 must be high voltage (5 V) transistors with the same device parameters as the high voltage (5 V) circuitry in order to maintain device reliability.

IV. Simulation Results

Simulations of the circuit shown in Fig. 2 based on Cadence-Spectre and a 1.2 μm CMOS technology are described in this section. The same devices are used in both the high voltage as well as the low voltage circuitry. In this example, $C_L = 1$ pF, the two power supplies are 3 V and 5 V, and the input signal changes at a rate of 100 MHz with 0.1 ns transition times.

The input-to-output delay of the 3 V to 5 V and the 5 V to 3 V interface circuits is summarized in Table I. The listed delays are shown: from the input to the low-to-high transition of A1 and A2, from the input to the high-to-low transition of B1 and B2, and from the input to the output low-to-high and high-to-low transitions. The low-to-high transitions of A1 and A2 and the high-to-low transitions of B1 and B2 are the signal transitions of primary interest.

TABLE I
The delay (in ns) at different points of the circuit for both the 3 V to 5 V and 5 V to 3 V interfaces

Interface	A1	A2	B1	B2	out 0-1	out 1-0
3 V to 5 V	1.10	1.25	1.40	1.55	1.75	1.90
5 V to 3 V	0.64	0.76	0.67	0.79	1.35	1.25

The operation of a typical 3 V to 5 V interface is shown in Fig. 4. Simulations exhibit non-overlapping A1 and A2 signals. B1 and B2 are the initial nodes where the voltage levels change and the 5 V (or 3 V for the 5 V to 3 V interface) swing is generated. For both interfaces, the size of the final stage of the buffer is $NF = 50\,\mu$m and $PF = 150\,\mu$m.

TABLE II
Delay components and output transition times (in ns) for both the 3 V to 5 V and 5 V to 3 V interfaces

Interface	ICD	ISD	BD	TT
3 V to 5 V	1.20	0.30	0.30	0.42
5 V to 3 V	0.70	0.03	0.60	0.65

In Table II, the total delay for the two interface circuits is composed of three delays within the circuit (with reference to Table I):

- The input converter delay (ICD) is the average of the delays from the input to A1 and to A2 (see Fig. 2 and Table I).
- The interface stage delay (ISD) is the average of the delays from A1 to B1 and from A2 to B2 (see Fig. 2 and Table I).

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• The buffer delay (BD) is the average of the delays from B1 to the output and from B2 to the output (see Fig. 2 and Table I).

The output transition time (TT) is also noted in Table II, defined between the 10% and 90% points of a signal.

Note that there are important differences between the 3 V to 5 V and the 5 V to 3 V interface circuits. These differences are due to the use of the same transistors with the same device parameters for both the 3 V and 5 V circuitry. The converter for the 5 V to 3 V interface operates at 5 V at a higher speed as compared to the 3 V to 5 V interface circuit operating at 3 V. The buffer, operating at 3 V for the 5 V to 3 V interface, is slow as compared to the 3 V to 5 V interface operating at 5 V. The interface stage has a fast response for the 5 V to 3 V interface due to the 5 V voltage swing on the N1 and N2 gates and only a 3 V output swing, as compared to the 3 V to 5 V interface. Note also that for the 5 V to 3 V interface, due to the high threshold voltage of the transistors, the output transition time is slower.

V. Conclusions

A circuit structure for use as an interface between any two CMOS voltage families is described. The circuit operates at high speed while eliminating any static power dissipation. The 3 V to 5 V and 5 V to 3 V interface circuits are analyzed and delay data are presented to exemplify this general purpose interface circuit structure.

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