Peak Noise Prediction in Loosely Coupled Interconnect

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Abstract— **Interconnect in VLSI circuits is best modeled as a lossy transmission line in high speed integrated circuits. Analytical expressions for the coupling noise between adjacent interconnect are presented to estimate the peak noise voltage on a quiet line based on the assumption that these interconnections are loosely coupled, where the effect of the coupling noise on the waveform of an active line is small. These closed form expressions are also applied to the condition of a varying load impedance. The estimated error of the peak noise amplitude at the near end of the quiet line is less than 15% under high loss and non-matching load conditions.**

I. Introduction

The trend in modern high speed, high density VLSI circuits is decreasing feature sizes as well as increasing chip dimensions. The delay of these highly scaled circuits is now dominated by the interconnect [1]. Furthermore, up to 30% of the dynamic power is consumed by the interconnect [2]. In addition to interconnect delay and power consumption, coupling noise (or crosstalk) between adjacent interconnect lines is becoming a primary concern for present and future generations of VLSI circuits [3], [4].

Before the emergence of high speed VLSI circuits, interconnect was modeled as a simple capacitor, a lumped RC, or a distributed RC line in medium speed applications [1], [5]. If the transition times of the input signals are comparable to or less than the time of flight of the signals propagating along the line, inductance should be considered in the interconnect model [6], [7], [8]. The interconnect should therefore be modeled as a lossy RLC transmission line in high speed applications. For simplicity, the interconnect is modeled in this paper as a uniform transmission line [9].

Interconnects in VLSI circuits are multi-conductor lines existing on different physical planes. The capacitance and inductance of the conductor lines can be extracted from the geometric layout [10]. The coupling effects become more significant as the feature size is decreased to deep submicrometer dimensions, because the spacing between conductor lines decreases to improve circuit density and the thickness of the conductors increases in order to reduce the parasitic resistance of the top level metal lines.

Analysis of the coupling noise can be performed in both the frequency domain and the time domain, but most of these analyses result in numerical solutions [11], [12] or an equivalent circuit simulation. The numerical solution is not convenient to use at the system (or chip) level to predict noise effects since it requires significant simulation time and computer memory. Analytical analysis of coupled lossless transmission lines in the time domain has been addressed in [13]. A lossless model, however, is not appropriate for interconnect in VLSI circuits, since the parasitic interconnect resistance cannot be neglected.

An analysis of two coupled lossy transmission lines in a homogeneous medium is presented in this paper. The analytical equations are derived from time domain differential equations using Laplace transforms and the assumption of a loosely coupled interconnect, *i.e.*, the coupling capacitance and the mutual inductance are assumed to be less than 30% of the self-capacitance and the self-inductance, respectively. The peak noise voltage is predicted based on these analytical equations. The accuracy and validity of the analytical equations are also examined in this paper. The coupling noise on the quiet (or victim) line reaches a steady state value over a period of time, but if the peak noise voltage is greater than the threshold voltage of the logic circuit, it may cause a circuit malfunction or dissipate extra power. In practice, the peak noise voltage (or maximum amplitude) is more important than the detailed shape of the noise waveform, since if the magnitude of the peak noise voltage is greater than the logic threshold, a logic malfunction may occur, particularly in noise sensitive digital circuits. Therefore, this analysis is focused on peak noise voltage (or maximum amplitude) estimation rather than modeling the complete noise waveform. The accuracy of the prediction is also applied to high loss transmission lines, where the error is within 15% for the near end coupling noise and 25% for the far end coupling noise. The accuracy of the maximum noise amplitude predicted at the near end is within 15% for a variety of load impedances.

The analytical equations for the coupling noise voltage at both ends of the quiet line are derived in Section II. The predicted coupling noise voltage is compared with simulation in Section III. A discussion of these results is provided in Section IV followed by some concluding remarks in Section V.

II. Derivation of Closed Form Expressions

Consider two coupled lossy transmission lines (shown in Figure 1 with current and voltage definitions), with similar impedance characteristics. Line 1 is the active (or aggressor) line and line 2 is the quiet (or victim) line. Laplace transforms are used to solve the time domain differential equations characterizing this structure. The resulting formulation is

$$\frac{\partial^2}{\partial x^2}V_1(x,s) = A_1V_1(x,s) + B_1V_2(x,s), \quad (1)$$

$$\frac{\partial^2}{\partial x^2}V_2(x,s) = A_2V_1(x,s) + B_2V_2(x,s), \quad (2)$$

where

$$A_1 = B_2 = sRC + s^2LC - s^2L_mC_m, \quad (3)$$

$$B_1 = A_2 = s^2L_mC - s^2LC_m - sRC_m. \quad (4)$$

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R, L, and C are the line resistance, inductance, and capacitance per unit length, respectively. L_m and C_m are the coupling inductance and capacitance per unit length, respectively, between line 1 and line 2. $V_1(x,s)$ and $V_2(x,s)$ are the Laplace transform of the voltages between line 1 and line 2, respectively, and ground.

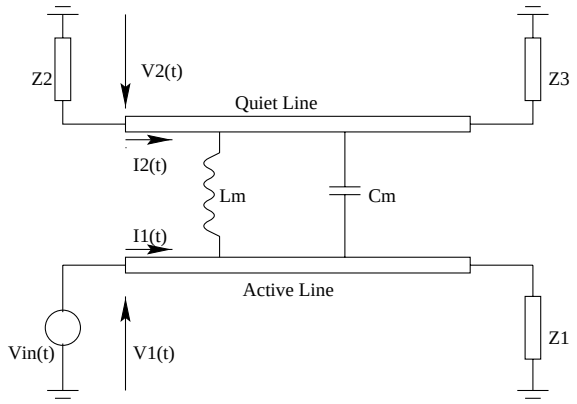

Fig. 1. Two coupled lossy transmission lines

In order to simplify this analysis, a loosely coupled condition is assumed, implying that L_m and C_m are small as compared to L and C such that the third term in (3) can be neglected. To quantify this assumption,

$$\frac{L_m}{L}\frac{C_m}{C} < 0.1. \tag{5}$$

The error is less than 5% with this assumption. Only first order effects are considered, where the voltage on line 1 affects the voltage on line 2 and $V_2(x,s)$ is too small to affect line 1. This situation occurs because the voltage on line 2 is coupled from the voltage on line 1. This assumption requires that those terms in (4) containing L_m and C_m are small, *i.e.*, both L_m/L and C_m/C are small. Combining with (5), the loosely coupled condition can be restated as

$$L_m/L < 0.3 \quad and \quad C_m/C < 0.3. \tag{6}$$

Based on this loosely coupled assumption, (1) and (2) can be simplified to

$$\frac{\partial^2}{\partial x^2}V_1(x,s) = \gamma^2 V_1(x,s), \tag{7}$$

$$\frac{\partial^2}{\partial x^2}V_2(x,s) = \gamma^2 V_2(x,s) + \alpha V_1(x,s), \tag{8}$$

where

$$\gamma = \sqrt{sRC + s^2LC}, \tag{9}$$

$$\alpha = (s^2 L_m C - sRC_m - s^2 LC_m). \tag{10}$$

The solution of (7) is

$$V_1(x,s) = V_+ e^{-\gamma x} + V_- e^{+\gamma x}. \tag{11}$$

V_+ and V_- can be solved based on the terminal conditions of line 1. The general solution of (8) is

$$V_2(x,s) = (a_1 x + c_1)e^{-\gamma x} + (a_2 x + c_2)e^{+\gamma x}. \tag{12}$$

a_1 and a_2 are determined by solving the non-homogeneous differential equation (8), and c_1 and c_2 are calculated by using the boundary conditions on line 2. Therefore, all of these coefficients are determined based on boundary conditions, permitting the general closed form solutions of $V_1(x,s)$ and $V_2(x,s)$ to be determined.

The time domain solution of $V_1(x,s)$ and $V_2(x,s)$ is obtained by applying an inverse Laplace transform. However, in many of these cases, a numerical solution results because certain inverse Laplace transforms cannot be derived explicitly. In order to determine a closed form analytical expression for use in chip level noise analysis, some approximating assumptions are necessary.

$$\begin{aligned}\gamma &= \sqrt{sRC + s^2LC} = s\sqrt{LC}(1 + \frac{R}{sL})^{\frac{1}{2}} \\ &\approx s\sqrt{LC}(1 + \frac{R}{2sL}) \qquad sL \gg R.\end{aligned} \tag{13}$$

The assumption of $sL \gg R$ is equivalent to $\omega L \gg R$ in the frequency domain. Assume the impedances of the load end of line 1 and both ends of line 2 match the line impedance, so that no reflection occurs at each terminal. V_+ and V_- can be determined as

$$V_+ = V_{in}(s) \quad and \quad V_- = 0. \tag{14}$$

c_1 and c_2, and a_1 and a_2 can be calculated based on V_+ and V_-. The induced noise voltage on line 2 for the matching condition becomes

$$V_2(x,s) = a_1 x e^{-\gamma x} + c_1 e^{-\gamma x} + c_2^{+\gamma x}. \tag{15}$$

A. Near-end noise voltage

For the near end coupling noise voltage, *i.e.*, $x = 0$, V_{NE} is

$$V_{NE}(s) = \frac{1}{4}(\frac{sL_m}{R+sL} + \frac{C_m}{C})(1 - e^{-2\gamma l})V_{in}(s). \tag{16}$$

Assume the input is a fast ramp signal $v_{in}(t) = V_{dd}/\tau_r[tu(t) - (t-\tau_r)u(t-\tau_r)]$. The first constraint for τ_r is $\tau_r \leq \tau_0$, where τ_0 is the time of flight delay of the signal through the transmission line and $\tau_0 = l\sqrt{LC}$. This constraint requires that the interconnect inductance cannot be neglected. The second constraint utilizes the assumption of $\omega L \gg R$. The frequency corresponding to this rise time is $\omega = 2\pi * 0.33/\tau_r = 2.0/\tau_r$ [14]. The requirement becomes $2\tau_1/\tau_r \gg 1$, where $\tau_1 = L/R$. $e^{-2\gamma l} \approx e^{-2s\tau_0 l - Rl/Z_0}$, where Z_0 is $\sqrt{L/C}$ – the characteristic impedance of a lossless transmission line. Using an inverse Laplace transform, the near end noise voltage $V_{NE}(t)$ in the time domain is

$$\begin{aligned}V_{NE}(t) &= V_o(t) - e^{-Rl/Z_0}V_o(t - 2\tau_0), \\ V_o(t) &= 0.25(\frac{V_{dd}}{\tau_r}\frac{L_m}{L}(V_p(t) - V_p(t-\tau_r)) \\ &\quad + \frac{C_m}{C}V_{in}(t)), \\ V_p(t) &= \tau_1(1 - e^{-t/\tau_1})u(t).\end{aligned} \tag{17}$$

The near end noise voltage is the summation of both the capacitive coupling noise voltage and the inductive coupling noise voltage. The steady state voltage of the near end noise voltage is zero.

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B. Far-end noise voltage

For the far end noise voltage, where $x = l$, V_{FE} is

$$V_{FE}(s) = -\frac{1}{2}\frac{s^2 L_m C - sRC_m - s^2 LC_m}{\gamma} l e^{-\gamma l} V_{in}(s). \tag{18}$$

For a fast ramp input signal, $V_{in}(s)$ is inserted into (18), permitting an inverse Laplace transform to be used to determine the far end coupling noise voltage $V_{FE}(t)$ in the time domain.

$$\begin{aligned} V_{FE}(t) \quad = \quad & -\frac{1}{2}\tau_0 e^{-\frac{Rl}{2Z_0}} \frac{V_{dd}}{\tau_r}\left(\frac{L_m}{L}\left(e^{-\frac{t-\tau_0-\tau_1}{2\tau_1}}\right.\right. \\ & u(t-\tau_0-\tau_1) - e^{-\frac{t-\tau_0}{2\tau_1}} u(t-\tau_0)\Big) \\ & -\frac{C_m}{C}(u(t-\tau_0) - u(t-\tau_0-\tau_1) \\ & -\frac{R}{2L}((t-\tau_0)u(t-\tau_0) - \\ & (t-\tau_1-\tau_0)u(t-\tau_0-\tau_1)))). \end{aligned} \tag{19}$$

The inductive coupling noise voltage and capacitive coupling noise voltage behave in the opposite direction at the far end. The far end coupling noise voltage is therefore the difference between these two noise components. The steady state noise voltage at the far end is also zero.

III. Comparison with Simulation

To verify the accuracy of these analytical expressions, (17) and (19), that describe the coupling noise voltage at both ends of a quiet line, a criterion is defined to measure the error of these closed form approximations. This criterion quantifies the error between the predicted peak noise voltage and the simulated peak noise voltage, permitting the accuracy of these analytical equations to be determined. The criterion is defined as

$$\epsilon_{peak} = |V_p - V_s|/|V_s|, \tag{20}$$

where V_p is the value of the peak noise voltage predicted by the analytical expressions, and V_s is the peak noise voltage obtained from a circuit simulator (SPICE). The equivalent circuit used in the SPICE simulation is shown in Figure 2.

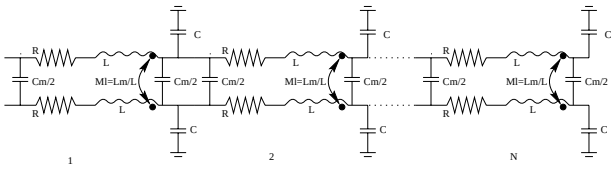

Fig. 2. The SPICE equivalent circuit of two coupled lossy transmission lines

The parameters used in the SPICE simulation are $R = 5\ \Omega/cm$, $C = 1\ pF/cm$, $L = 2\ nH/cm$, $L_m/L = 0.2$, $C_m/C = 0.1$, $l = 2\ cm$, $V_{dd} = 5.0\ V$, $\tau_r = 80\ ps$, and $N = 20$. The load at each end is $Z_1 = Z_2 = Z_3 = Z_0 = \sqrt{L/C} = 44.72\ \Omega$. Both the analytical and simulation results are depicted in Figures 3 and 4 for the near end and the far end coupling noise voltage, respectively. The error of the peak noise voltage is less than 1% at the near end and within 1.5% at the far end. The analytically derived noise waveform deviates at the far end since the phase difference is neglected.

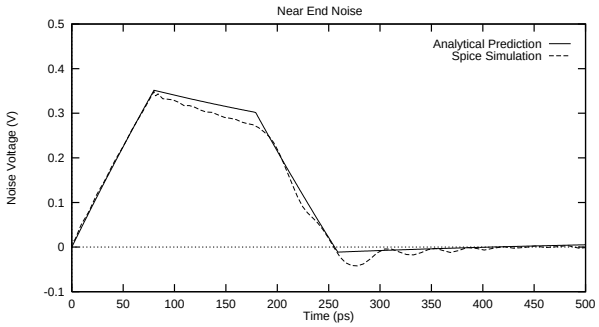

Fig. 3. Near end noise

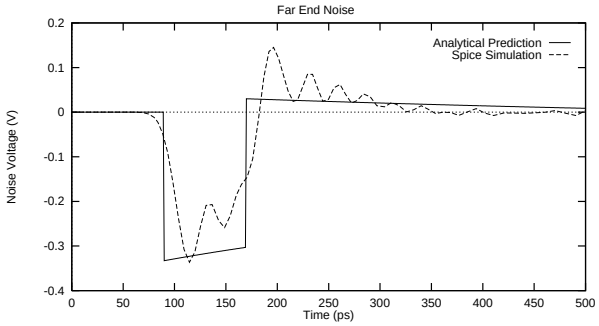

Fig. 4. Far end noise

IV. Discussion

In the design of high speed VLSI circuits, it is important to be able to predict coupling noise at the system (or chip) level. This information permits circuit or layout based design techniques to be used to avoid circuit malfunctions or extra power consumption caused by coupling noise. The design cycle and cost can therefore be reduced as well as circuit reliability improved.

The constraint that the rise time is less than the time of flight is one important assumption, *i.e.*, $2\tau_1/\tau_r \gg 1$ and $\tau_r < \tau_0$. If $\tau_r < \tau_0$, the interconnect inductance must be considered in the interconnect model. If $2\tau_1/\tau_r \gg 1$, *i.e.*, $\omega L > R$, the interconnect should be modeled as a low loss transmission line. Three different regions of operation are defined: condition 1: $\tau_1/\tau_r = 1$, condition 2: $\tau_1/\tau_r = 2$, and condition 3: $\tau_1/\tau_r = 4$. The total line resistance (Rl) changes from 0 to $0.5Z_0$ for each condition. The deviation of the peak noise voltage from SPICE simulation is shown in Figures 5 and 6 at the near end and at the far end, respectively. The error is within 15% at the near end and 25% at the far end for these conditions. If the interconnect is modeled as a high loss transmission line ($Rl \leq 0.5Z_0$), these analytical equations are highly accurate (less than 15% error).

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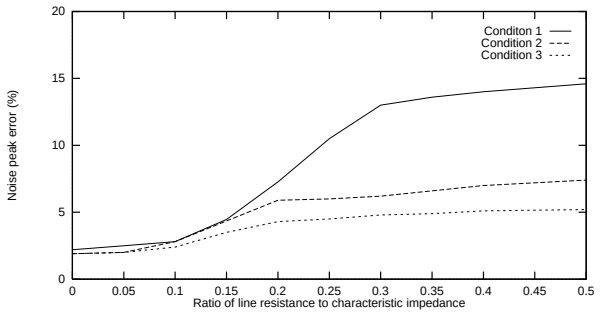

Fig. 5. Error of peak noise estimation of lossy interconnect at the near end

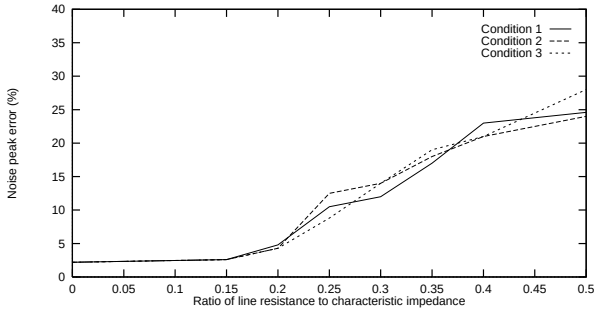

Fig. 6. Error of peak noise estimation of lossy interconnect at the far end

To obtain an accurate noise voltage waveform, an analysis of the phase characteristics of the signal traveling along the transmission line is required. This analysis, however, is prohibitive due to the computational complexity. In digital circuits, the amplitude of the peak noise voltage is more important than the shape of the noise waveform because the peak voltage can be compared with the logic threshold in order to avoid logic malfunctions.

The other assumption is that the load impedance matches the line impedance. An analysis is necessary to quantify the deviation of the predicted noise amplitude for the condition of a non-matching load. If the load impedance does not match the line impedance, the coupling noise will oscillate before the signal reaches a steady state voltage because the signal is reflected back from the load. The maximum amplitude of the noise voltage (the absolute value of the peak noise voltage) is used to measure the deviation between simulation and the analytical results. Both the load end impedances of line 1 and line 2 are varied, where Z_1/Z_0 is in the range of 0.2 to 50 and Z_3/Z_0 is in the range of 0.5 to 10. The deviation at the near end is shown in Figure 7, where R is defined as the ratio of Z_3/Z_0. The horizontal axis is the ratio of Z_1/Z_0. The error is within 15% except for small load impedances, a situation not typically seen in CMOS VLSI circuits.

V. Conclusion

Analytical equations are presented in this paper to serve as a means for efficiently and accurately estimating the peak noise voltage in lossy interconnects. Errors

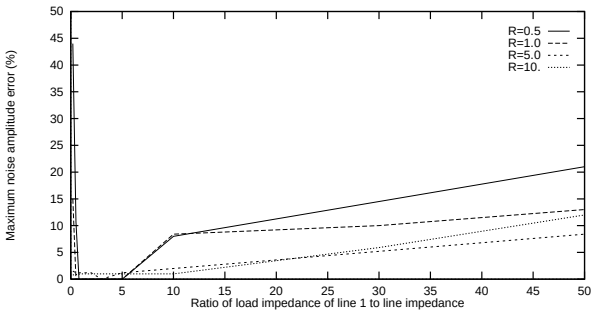

Fig. 7. Error of maximum noise voltage for non-matching load impedances

within 15% are demonstrated at the near end and 25% at the far end. These analytical equations can be used to estimate crosstalk in CMOS VLSI circuits.

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