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Wire shaping of *RLC* interconnects ☆

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Abstract

The optimum wire shape to produce the minimum signal propagation delay across an *RLC* line is shown to exhibit a general exponential form. The line inductance makes exponential tapering more attractive for *RLC* lines than for *RC* lines. For *RLC* lines, optimum wire tapering achieves a greater reduction in the signal propagation delay as compared to uniform wire sizing. For *RLC* lines, exponential tapering outperforms uniform repeater insertion. As technology advances, wire tapering becomes more effective than repeater insertion, since a greater reduction in the propagation delay is achieved. Optimum wire tapering achieves a reduction of 36% in the propagation delay in long *RLC* interconnect as compared to uniform repeater insertion.

Wire tapering can reduce both the propagation delay and power dissipation. Optimum tapering for minimum propagation delay reduces the propagation delay by 15% and power dissipation by 16% for an example circuit. The optimum tapering factor to minimize the transient power dissipation of a circuit is described in this paper. An analytic solution to determine the optimum tapering factor that exhibits an error of less than 2% is provided. Wire tapering is also shown to reduce the power dissipation of a circuit by up to 65%.

Wire tapering can also improve signal integrity by reducing the inductive noise of the interconnect lines. Wire tapering reduces the effect of impedance mismatch in digital circuits. The difference between the overshoots and undershoots in the signal waveform of an example clock distribution network is decreased by 34% as compared to a uniformly sized network producing the same signal characteristics.

Keywords: Inductive interconnects; Interconnect shaping; Power dissipation; On-chip inductance; Inductive noise; Signal integrity; Propagation delay

1. Introduction

With the decreased feature size of CMOS circuits, on-chip interconnect now dominates both circuit delay and power dissipation. Interconnect design has therefore become a dominant issue in high-speed integrated circuits (ICs). The interconnect width in particular is a primary design choice in the interconnect design process. Many algorithms have been proposed to determine the optimum wire size that minimizes a cost function such as delay. As shown in [1,2], the optimum interconnect shape which minimizes the signal propagation delay in an *RC* interconnect is an exponential function. Different extensions to this work have been applied to consider other circuit parameters such as fringing capacitance [3–19].

Wire tapering increases the interconnect width at the near end (the driver end) of the line as shown in Fig. 1. Wire tapering is usually applied to long lines, increasing the importance of the line inductance [20,21] in the optimization process of tapered lines. No previous work has been published (to the authors' best knowledge) that describes the optimum wire shape to minimize the propagation delay of an *RLC* line. Previous work in tapered *RLC* lines [7] uses the optimum shape for *RC* lines without demonstrating

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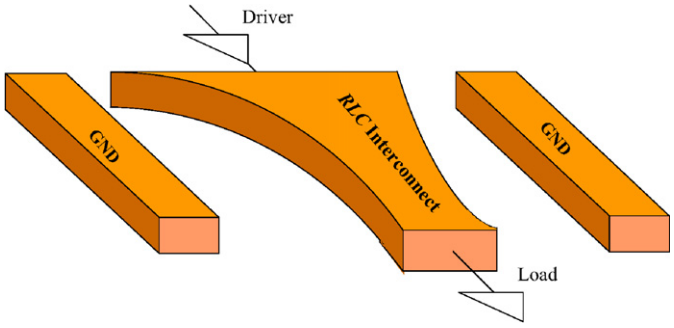

Fig. 1. Coplanar tapered *RLC* interconnect.

that the shape is optimum for *RLC* lines. Furthermore, the optimum tapering factor has not been presented. Moreover, additional issues such as the efficiency of wire tapering over other techniques to drive long interconnect lines and the power dissipation of tapered interconnect have not been considered in *RLC* lines.

The research described in [22] shows that wire tapering improves signal speed by only 3.5% as compared to uniform wire sizing if an optimum repeater system is used to minimize the propagation delay of an *RC* line. Uniform wire sizing is an efficient technique to improve circuit performance [23]. As compared to tapered sizing, uniform wire sizing is also easier to implement if a repeater system is available. The inductance, however, has not been considered in the line model described in [22]. Furthermore, for practical reasons, a repeater system is not always possible. Moreover, repeater insertion increases the power dissipation due to the additional capacitance of the repeaters. It is shown in this paper that, for minimum signal propagation delay, exponential wire tapering is the optimum shape for an *RLC* interconnect. An analytic expression to determine the optimum tapering factor for minimum propagation delay is also provided. Tapered *RLC* lines are compared with other performance enhancement techniques in this paper. As described here, tapered *RLC* lines can achieve a greater reduction in delay as compared to tapered *RC* lines. Whenever possible, uniform repeater insertion is used as an efficient technique to reduce the signal propagation delay [24]. Also described in this paper, wire tapering not only outperforms uniform wire sizing but also outperforms uniform (optimum) repeater insertion. For *RLC* lines, exponential tapering achieves the lowest propagation delay as compared to uniform wire sizing with or without repeaters.

Not only propagation delay but also the power dissipation characteristics are affected by wire sizing. As described in [25–27], wire sizing for *RLC* interconnects can decrease the total power dissipated by a circuit. Wire tapering as a wire sizing technique is shown to reduce power dissipation as well as propagation delay [27]. An analytic expression to determine the optimum tapering factor to produce the minimum transient power dissipation is described in this paper.

In addition to the reduced propagation delay and power dissipation with tapered lines, tapered *RLC* interconnects may exhibit enhanced signal integrity, reducing the inductive noise. Noise reduction has become an important issue in the design of modern integrated circuits. Particularly for *RLC* interconnects, noise can cause signal degradation and even cause a circuit to malfunction. The line inductance may also produce overshoots and undershoots in the signal waveform, increasing the noise in the circuit. This issue of signal integrity in tapered lines is further discussed in the paper.

The paper is organized as follows. In Section 2, the optimum wire shape that produces the minimum signal propagation delay of an *RLC* line is characterized. Different constraints on interconnect tapering are discussed in Section 3. In Section 4, a comparison between tapered *RC* and *RLC* lines is described. Wire tapering is presented in Section 5 as an option to minimize the transient power dissipation of a circuit. In Section 6, line tapering is compared with uniform repeater insertion. Signal integrity in tapered *RLC* networks is discussed in Section 7. Some simulation results are presented in Section 8. In Section 9, some conclusions are provided.

2. Optimum wire shape for minimum propagation delay

The signal propagation delay of a distributed *RLC* interconnect is described in [28,29]. Two time constants characterize the signal speed and behavior in long interconnects, the resistive–capacitive (*RC*) time constant and the inductive–capacitive (*LC*) time constant (or the time-of-flight through the line $t_f = \sqrt{L_{int} C_{int}}$), where C_{int} and L_{int} are the line capacitance and inductance, respectively). For highly resistive (less inductive) lines, an *RC* delay model is sufficient to characterize the signal delay. The optimum tapering relation for these lines is an exponential tapering factor [1,2]. If the inductive behavior of the line dominates the resistive behavior, the time-of-flight can dictate the time for the signal to propagate across the line [30]. The optimum shape that minimizes the propagation delay of an *LC* line is the shape function that minimizes the time-of-flight.

Ignoring the fringing capacitance, the line inductance and capacitance per unit length, respectively, can be expressed in terms of the line width by the following simple relationships [31],

$$L_{int}(W) = \frac{L_0}{W(x)}, \tag{1}$$

$$C_{int}(W) = C_0 W(x) + C_c, \tag{2}$$

where L_0 is the line inductance per square, C_c is the coupling capacitance with the adjacent lines per unit length, and C_0 is the line capacitance per unit area. $W(x)$ is the line width as a function of x, the distance from the load as shown in Fig. 2. The separation between the shaped line and the adjacent lines is assumed to be equal to the

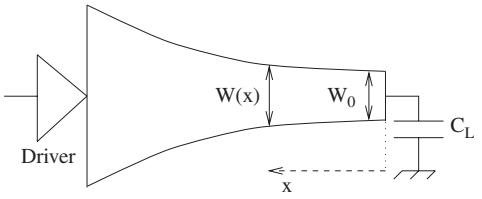

Fig. 2. *RLC* line tapered by a general width tapering function $W(x)$.

separation before shaping the line. The coupling capacitance is weakly dependent on line width.

The time-of-flight for the signal is

$$t_f = a\sqrt{\int_0^l \frac{L_0}{W(x)}\int_0^x (C_0 W(y) + C_c)\,dy\,dx}, \tag{3}$$

where l is the line length and a is a constant. a equals $\sqrt{2}$ for a uniform line. If functions F and $u(x)$ are defined as

$$F \equiv \frac{L_0}{W(x)}\int_0^x (C_0 W(y) + C_c)\,dy,$$

$$u(x) \equiv \int_0^x W(y)\,dy,$$

respectively, and Euler's differential equation is used to minimize (3), as similarly described in [1], the optimum $u(x)$ should satisfy the differential equation,

$$u'(x) = \frac{2L_0C_0}{c}u(x) + \frac{2C_cL_0l}{c}. \tag{4}$$

Thus,

$$W(x) = W_0\,e^{(2L_0C_0/c)x}, \tag{5}$$

where $c = 2C_cL_0l/W_0$. W_0 is obtained by substituting (5) into (3) and differentiating (3) with respect to W_0. Setting the result to zero produces a nonlinear equation which can be solved numerically.

As shown in (5), the optimum tapering function of the width of an *LC* line is an exponential function. For either an *RC* or *LC* line, the general form of the optimum shaping function that minimizes the propagation delay is an exponential function. The *RC* and *LC* models are the two limiting cases of a general *RLC* interconnect. The optimum tapering function of an *RLC* line must satisfy the general exponential form $W(x) = qe^{px}$, where q is the line width at the load end and p is the tapering factor. The optimum value of q and p for an *RLC* line reduces to an *RC* line [1,2] if the line inductance is negligible and to an *LC* line (with $q = W_0$ and $p = 2L_0C_0/c$ in (5)) if the line resistance is negligible. The optimum value of q and p for an *RLC* line is between these two limits.

As described in [21,32,33], for an *RLC* line, the signal propagation delay is minimum when the line is matched with the driver. The matched condition, from [33], is

$$R_{tr} = |Z_{line}(q,p)|, \tag{6}$$

which can be used to determine the optimum tapering function. $Z_{line}(q,p)$ is the lossy characteristic impedance of a line, where

$$|Z_{line}(q,p)| = \sqrt{\frac{\sqrt{R_{line}(q,p)^2 + (\omega(p.q)L_{line}(q,p))^2}}{\omega(p.q)C_{line}(q,p)}}, \tag{7}$$

$$\omega(p.q) = \frac{2\pi}{3t_r(p.q)}, \tag{8}$$

and R_{tr} is the equivalent output resistance of the driver. $R_{line}(q,p)$, $L_{line}(q,p)$, and $C_{line}(q,p)$ are the line resistance, inductance, and capacitance as functions of q and p, respectively. $t_r(p,q)$ is the signal transition time at the near end of the line which is determined from the reduced order model described in [33].

As there is one equation, (6), and two unknowns, q and p, there are two degrees of freedom in designing an *RLC* line tapered for minimum delay. For a width q, there is an optimum tapering factor p_{opt} which satisfies (6) and at which the propagation delay is minimum. Other design constraints, such as the minimum and maximum line width and the power dissipation, are discussed in Section 3 to provide a more power efficient solution.

3. Constraints on optimum tapering for *RLC* lines

Tapering an interconnect assigns a smaller width for the line at the far end. The line width is greater at the near end, as shown in Fig. 2. As discussed in Section 2, the width increases exponentially to produce the minimum propagation delay. By choosing q and solving (6) as a nonlinear equation in one unknown, the optimum tapering factor p_{opt} can be determined. There are two practical limits for choosing q,

(1) $q \geqslant W_{min}$, where W_{min} is the minimum wire width of a target technology.
(2) $q \geqslant W_{max}e^{-pl}$, where W_{max} is the maximum wire width of a target technology.

These two constraints should be satisfied when designing a tapered line. q cannot be smaller than the minimum wire width allowed by the technology. Alternatively, increasing q may result in a width at the near end (the largest width of the line) which may be greater than the maximum available wire width.

Another important design constraint is the power dissipation. Wire sizing affects the two primary transient power components, the dynamic power dissipated in charging and discharging the line capacitance and the short-circuit power dissipated within the load gate. The short-circuit power is minimum when the line is matched with the driver [25–27], which is also the optimum solution for minimum delay.

The dynamic power is linearly proportional to the line capacitance. To minimize the line capacitance, the line width should be as narrow as possible, as the line capacitance increases superlinearly with the width [34]. In

order to satisfy both high-speed and low power design objectives, q should be chosen equal to W_{min}. The optimum value for the tapering factor p_{opt} is obtained by solving (6) for $q = W_{min}$. Optimum wire tapering is compared in Section 4 with uniform wire sizing for both *RC* and *RLC* lines.

4. Tapering versus uniform wire sizing in *RC* and *RLC* lines

Interconnect tapering is more efficient in *RLC* lines than in *RC* lines. Two effects reduce the signal propagation delay of an exponentially tapered *RLC* line. The first effect is the shape of the line structure which minimizes both the *RC* and *LC* time constants.

The second effect is an increase in the inductive behavior of the line. Tapering an interconnect line decreases the line resistance, reducing the attenuation along the line. This effect increases the inductive behavior of the line. The inductive behavior of the line can be characterized by $\zeta = (R_{line}/2)\sqrt{C_{line}/L_{line}}$, the damping factor of a line [20]. As described in [20], when $\zeta < 1.0$, the inductive behavior of a line cannot be ignored. As shown in Fig. 3, the damping factor decreases (for different line thickness T and length l) as the line tapering factor increases, making the line behave more inductively. For $\zeta > 1.0$ (the dotted lines), the damping factor does not consider the inductive behavior of the line since the line is underdamped. The inductive effect of a line where $\zeta > 1.0$ is negligible.

The line inductance shields part of the line capacitance and decreases the equivalent output resistance of the gate that drives the line. The signal propagation delay decreases as the inductive behavior of the line becomes more pronounced [33]. This effect makes line tapering more attractive in long *RLC* lines.

Another criterion to optimize the interconnect width for minimum propagation delay is uniform wire sizing.

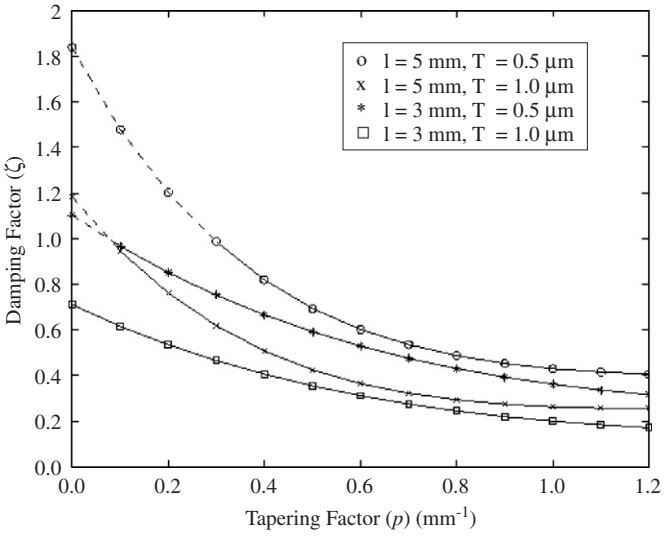

Fig. 3. Interconnect damping factor as a function of tapering factor for different line parameters.

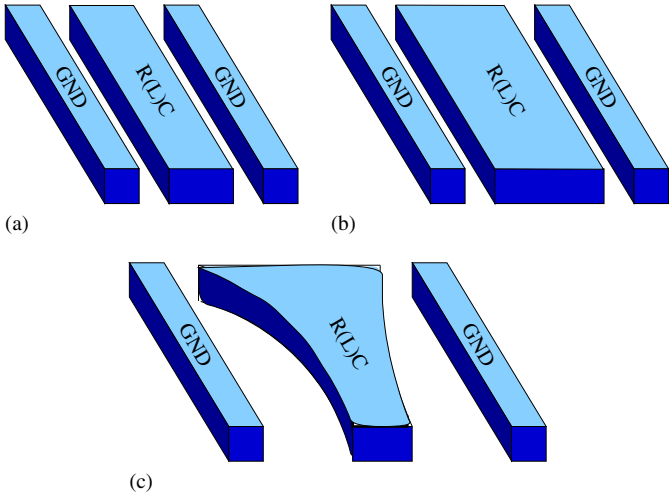

Fig. 4. Coplanar interconnect: (a) minimum width, (b) uniform sizing, (c) exponential tapering.

A minimum width coplanar interconnect line is illustrated in Fig. 4 for two sizing criteria, uniform sizing and exponential tapering.

A uniform wire size is composed of a constant interconnect width along the line length. Exponential wire tapering outperforms uniform wire sizing as discussed in Section 2. As with wire tapering, uniform wire sizing can decrease the line resistance, making the inductive behavior greater; however, the superlinear increase in the line capacitance limits the effect of the line inductance on reducing the signal propagation delay. Wire tapering, however, produces a smaller delay than the delay achieved from uniform wire sizing. Optimum wire tapering produces a greater delay reduction in *RLC* lines than in *RC* lines since the delay is further reduced due to the inductive behavior of the line as described in [33]. The line inductance makes tapering more efficient than uniform wire sizing in *RLC* lines.

For an *RLC* line, tapering not only reduces the propagation delay, but also decreases the total power dissipation as compared to uniform wire sizing. An increase in the inductive behavior of the line reduces the signal transition time at the load, reducing the short-circuit current and, consequently, the total transient power dissipation [25,35]. Simulation results are presented in Section 8.1 that illustrate the efficiency of exponential wire tapering on both the propagation delay and power dissipation of *RLC* lines. Exponential tapering is shown in Section 5 to minimize the total transient power dissipation of a circuit.

5. Interconnect tapering for minimum power dissipation

Wire sizing for *RLC* interconnects can decrease the total power dissipation of a circuit since the power dissipated in the load can be traded off with the power dissipated by the driver [25–27]. Uniform wire sizing decreases the transition

time at the load, reducing the short-circuit power of the load gate. Tapered wire sizing also reduces the attenuation along the interconnect line, decreasing the signal transition time at the load. A tradeoff, therefore, exists between the short-circuit power of the load gate and the dynamic power of the driver in long tapered interconnect.

The power components of an inverter driving a load of two inverters through a long interconnect is shown in Fig. 5. As the tapering factor increases, the power dissipation in the load gates (inverters) decreases. The signal transition time becomes smaller, decreasing the short-circuit power of the load gates. The power dissipated by the driver increases, since the interconnect line capacitance is larger, increasing the dynamic power required to charge the line capacitance. An optimum tapering factor, therefore, exists to achieve the minimum total transient power dissipation.

The work described in [25] provides an analytic solution for the optimum interconnect width for minimum power dissipation. The uniform interconnect width W_{int} is replaced with an exponential function qe^{px}. A minimum interconnect width at the load end $q = W_{\min}$ is assumed. The optimum tapering factor rather than the optimum width is determined from

$$\frac{dP_t}{dp} = fV_{dd}^2 \frac{dC_{\text{line}}}{dp} + \frac{NfG}{0.8}\left(\frac{dt_{10\%}}{dp} - \frac{dt_{90\%}}{dp}\right) = 0, \tag{9}$$

where G is a function of V_{dd}, threshold voltage V_t, transconductance K of the load gate, and capacitive load C_L. f is the operating frequency, N is the number of driven gates, P_t is the total power dissipation, $t_{10\%}$ and $t_{90\%}$ are the times at which the voltage at the load end reaches 10% and 90%, respectively, $\frac{dt_{10\%}}{dp}$ and $\frac{dt_{90\%}}{dp}$ are described in [25], and $\frac{dC_{\text{line}}}{dp}$ is obtained from the capacitance expression described in the Appendix. The analytic solution to optimize a tapered interconnect line for minimum transient power dissipation is exemplified in Section 8.2. In Section 6, the performance of interconnect tapering is compared with uniform repeater insertion.

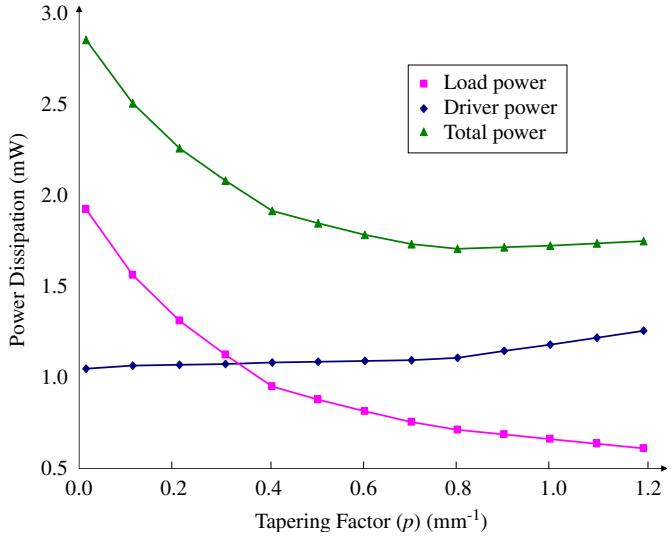

Fig. 5. Power dissipation in a load driven by a long tapered interconnect line.

6. Interconnect tapering versus repeater insertion

No repeaters are assumed to be placed along the interconnect line described in Section 4. Practical reasons may restrict the use of repeaters along the interconnect. If practical, however, repeater insertion can improve the performance of *RC* lines. Repeater insertion is an efficient technique to reduce propagation delay in long *RC* interconnects [42]. Uniform repeater insertion techniques divide the interconnect line into equal sections and employ equal size repeaters to drive each section [24,42]. As compared to repeater insertion with uniform wire sizing, wire tapering improves the speed of an *RC* line by at most 3.5% as described in [22]. Unlike tapered *RC* lines, tapered *RLC* lines can achieve a greater reduction in the propagation delay as compared to uniform repeater insertion. As described in [43,44], wire sizing is more efficient than repeater insertion in *RLC* lines. In *RLC* interconnects, wire sizing decreases the number of repeaters required to achieve the minimum propagation delay. The propagation delay of wide *RLC* interconnect lines with no repeaters is less than the propagation delay of thin lines driven by an optimum repeater system [43,44]. Uniform and tapered sizing of *RLC* interconnects are two wire sizing techniques which outperform repeater insertion. Exponential wire tapering is more efficient than uniform wire sizing as presented in Section 4. Among the three design techniques, exponential wire tapering achieves the minimum propagation delay, since the optimum interconnect shape is exponential and, in general, wire sizing outperforms repeater insertion in *RLC* lines. Some simulation results are presented in Section 8.3 that compare wire tapering with repeater insertion. In Section 7, an additional advantage of wire tapering in *RLC* interconnects is presented.

7. Signal integrity in tapered *RLC* interconnects

Signal integrity is an important design issue in integrated circuits. Particularly for inductive interconnects, the impedance mismatch may cause reflections at both the driver output and the load. The impedance mismatch between the driver and the load in digital circuits may distort the signal, causing overshoots and undershoots in the signal waveform. Tapered interconnect lines can enhance signal integrity as compared to uniformly sized lines. Line tapering reduces the magnitude of the reflections, since the line resistance is higher at the load end. The line resistance dominates the line impedance at the load, reducing the inductive noise of the signal propagating along the line. Moreover, exponential tapering reduces the inductive noise, since the impedance mismatch is distributed along the line and not concentrated at the load.

As described in Section 2, exponential tapering produces a smaller propagation delay as compared to uniform wire sizing. In some interconnect networks (such as clock distribution networks), the delay can be increased to enhance the signal integrity. Line tapering can achieve the same signal characteristics (propagation delay and transition time) of a uniform line while reducing ringing in the interconnect network. An efficient technique for tapering the interconnect lines of a clock distribution network while maintaining the same signal characteristics is described in [45,46]. This technique is used to demonstrate the efficiency of interconnect tapering to improve signal integrity.

The difference between the first overshoot and undershoot $\Delta V_{over-under}$ at the driving point of an interconnect network is treated as a metric to characterize the reflections (the ringing effect). An example clock distribution network is considered in Section 8.4 to demonstrate the improvements in signal integrity achieved when tapered interconnect lines are considered.

8. Simulation results

In order to determine the optimum tapering factor, the line impedance parameters (R_{line}, L_{line}, and C_{line}) are expressed in terms of the design parameters q and p. Closed form expressions for the line parameters are provided in the Appendix.

A 0.24 μm CMOS technology is used to demonstrate the efficiency of tapering an *RLC* line. A 5 mm long interconnect line with $T = 0.5\,\mu m$, $W_{min} = 0.5\,\mu m$, $W_{max} = 20\,\mu m$, and $S_{min} = 1.0\,\mu m$ is considered as an example. A long interconnect driven by a CMOS inverter is modeled by 20 *RLC* sections. The line is shielded by two 1.0 μm wide ground lines, and loaded with N CMOS inverters. In Section 8.1, tapered wire sizing is compared with uniform wire sizing. In Section 8.2, the interconnect line is tapered for minimum power dissipation. A comparison between wire tapering and repeater insertion is presented in Section 8.3. An example clock distribution network is used in Section 8.4 to demonstrate signal integrity in an interconnect network.

8.1. Tapering versus uniform wire sizing

As listed in Table 1, the effect of tapering on three different circuits is evaluated. W_n and W_{nl} are the width of the NMOS transistor of the driving and load inverters, respectively. t_{r-In} is the transition time of the signal at the input of the driving inverter. As described in Section 3, q is chosen to minimize the power dissipation based on the minimum line width W_{min}. The width of each section and the corresponding line impedance parameters are described in the Appendix.

Table 1
Circuit parameters of example circuits

	W_n (μm)	W_{nl} (μm)	t_{r-In} (psec)	q (μm)	p (m^{-1})
Circuit 1	15	5	50	0.5	550
Circuit 2	20	1	50	0.5	600
Circuit 3	15	15	20	1.0	400

The minimum delay is determined for both uniform wire sizing and exponential line tapering. As shown in Fig. 6, wire tapering outperforms uniform wire sizing for all of the circuits. The reduction in the minimum delay is greater for an *RLC* line as compared to an *RC* line, making tapering more efficient in *RLC* lines. A 15% reduction in delay for an *RLC* line as compared to a reduction of 7% for an *RC* line is achieved when exponential tapering is used rather than uniform wire sizing.

In addition to a smaller propagation delay, the total transient power dissipation is lower. A tapered line with q equal to the minimum width reduces the total line capacitance, thereby decreasing the dynamic power (as compared to uniform wire sizing). Furthermore, the power dissipation is further decreased in an *RLC* line since the short-circuit power is lower. The reduction in power dissipation for several *RC* and *RLC* lines is shown in Fig. 7. A reduction in power dissipation of as much as 16% for an *RLC* line as compared to 11% for an *RC* line is achieved when exponential tapering is used rather than uniform wire sizing.

8.2. Tapering for minimum power dissipation

In Section 8.1, wire tapering for minimum signal propagation delay is described for several example circuits. As discussed in Section 5, line tapering can be used to minimize the power dissipation of a circuit. The analytic solution presented in Section 5 is applied to determine the tapering factor for minimum power dissipation. For $W_n = 25\,\mu m$, $W_{nl} = 15\,\mu m$, and $W_{min} = 0.1\,\mu m$, the tapering factor is listed in Table 2. A different number N of load

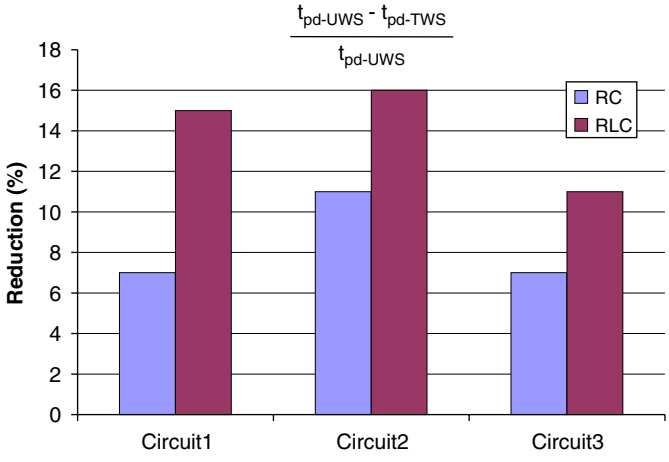

Fig. 6. Reduction in propagation delay. UWS stands for uniform wire sizing and TWS stands for tapered wire sizing.

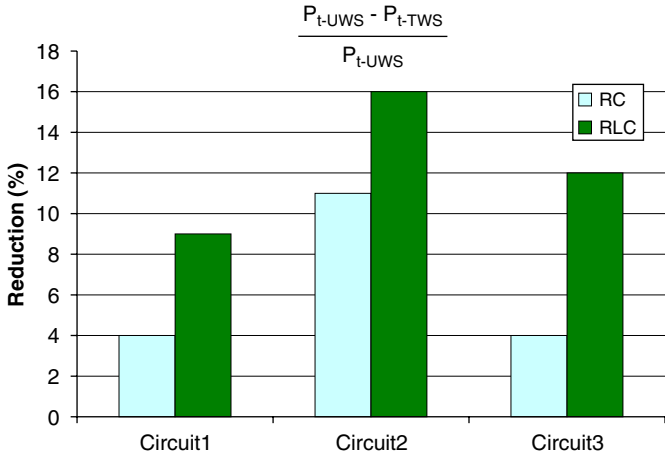

Fig. 7. Reduction in total power dissipation.

Table 2
Exponential tapering for minimum power dissipation

	Exponential tapering for minimum power $p_{opt-Power}$ (mm^{-1})	
Number of loads N	Analytic	Simulation
1	0.76	0.75
2	0.83	0.85
5	0.94	1.20

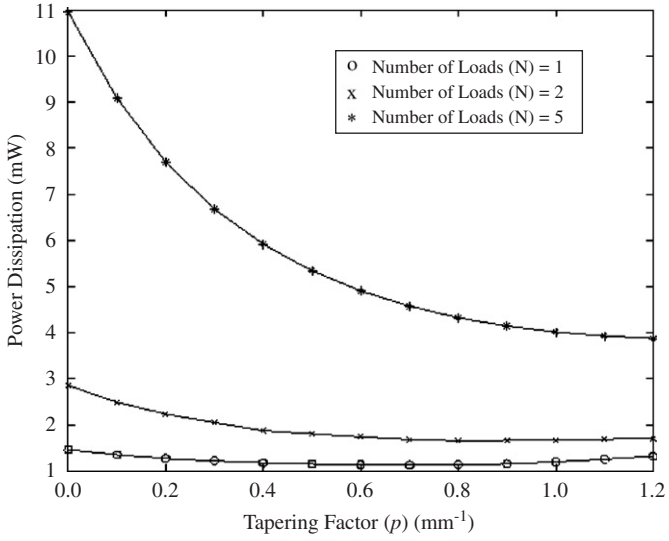

Fig. 8. Power dissipation for different number of loads driven by a long tapered interconnect line.

inverters is considered to determine the total power dissipation of a circuit. The total power dissipation for $N = 1$, 2, and 5 is shown in Fig. 8.

As the number of loads increases, the reduction in power dissipation increases with tapered interconnect lines. A higher per cent of the power is dissipated in the load gates (inverters), decreasing the overall power dissipation.

The tapering factor for minimum power dissipation is determined by the analytic expression and simulation as listed in Table 2. For the tapering factor determined analytically and by simulation, the total power dissipated by the circuit described in Section 8.1 for a different number of loads is listed in Table 3. The per cent reduction in power for each tapering factor rather than a uniform (minimum) interconnect width is also listed. The analytic solution is shown to be highly accurate in determining the tapering factor for minimum power. The lumped model is sufficient to determine the optimum tapering factor. The difference between the reduction in power using the analytic solution and simulation is less than 2%.

Tapering is more efficient in reducing the total power dissipation as the number of load gates increases (greater power is dissipated in the loads). For a large number of loads (e.g., $N = 5$), a significant reduction in power dissipation of around 65% is achieved.

8.3. Tapering versus repeater insertion

In order to verify the efficiency of wire tapering as compared to inserting repeaters in *RLC* interconnects, the propagation delay of a uniform repeater system is determined. The optimum number of repeaters is determined for two values of interconnect widths, $q = 0.5$ and 1.0 μm [28]. The tapering factor is obtained for different driver sizes based on the matched condition, (6). Equally sized repeaters divide the line into sections of equal lengths. For $q = 1.0\,\mu m$, the propagation delay at the end of a uniform line driven by repeaters is listed in the second column of Table 4. For $q = 1.0\,\mu m$, one repeater in the middle of the interconnect line is the optimum solution to drive the interconnect [28]. As listed in the table, for all values of driver (repeater) size, line tapering outperforms repeater insertion. Replacing a repeater system with an exponentially tapered line decreases the overall signal propagation delay. A reduction in delay of up to 24% is achieved using a tapered line.

The minimum permissible interconnect width (assumed in this paper to be 0.5 μm) decreases with advancing technology. For $q = 0.5\,\mu m$, two repeaters are required to achieve the minimum propagation delay using optimum repeater insertion. The propagation delay of this system is listed in Table 5.

As the interconnect width decreases, more repeaters are required to drive the more resistive interconnect. Tapering the line, however, achieves a smaller propagation delay as compared to inserting repeaters. The per cent reduction in propagation delay increases with decreasing line width. With advances in technology, interconnect tapering will become more effective since a greater reduction in propagation delay will be achieved.

8.4. Signal integrity characteristics in an example clock distribution network

An example clock distribution network is used to demonstrate the improvement in signal integrity as wire

Table 3
Total power dissipation using different sizing techniques

Number of Loads N	No tapering ($p = 0$) (mW)	Exponential tapering ($p_{opt-Power}$)			
		Analytic (mW)	Reduction (%)	Simulation (mW)	Reduction (%)
1	1.47	1.129	22.94	1.128	23.00
2	2.86	1.658	41.98	1.654	42.12
5	10.96	4.092	62.66	3.876	64.64

Table 4
Propagation delay for a long interconnect (5 mm) with $q = 1.0\,\mu m$

Driver (repeater) size (μm)	Propagation delay (psec)		
	Uniform repeater insertion	Exponential line tapering	Reduction (%)
10	279	229	18
15	227	179	21
20	199	151	24
25	182	141	23

Table 5
Propagation delay for a long interconnect (5 mm) with $q = 0.5\,\mu m$

Driver (repeater) size (μm)	Propagation delay (psec)		
	Uniform repeater insertion	Exponential line tapering	Reduction (%)
10	325	227	30
15	278	181	35
20	255	163	36
25	244	181	26

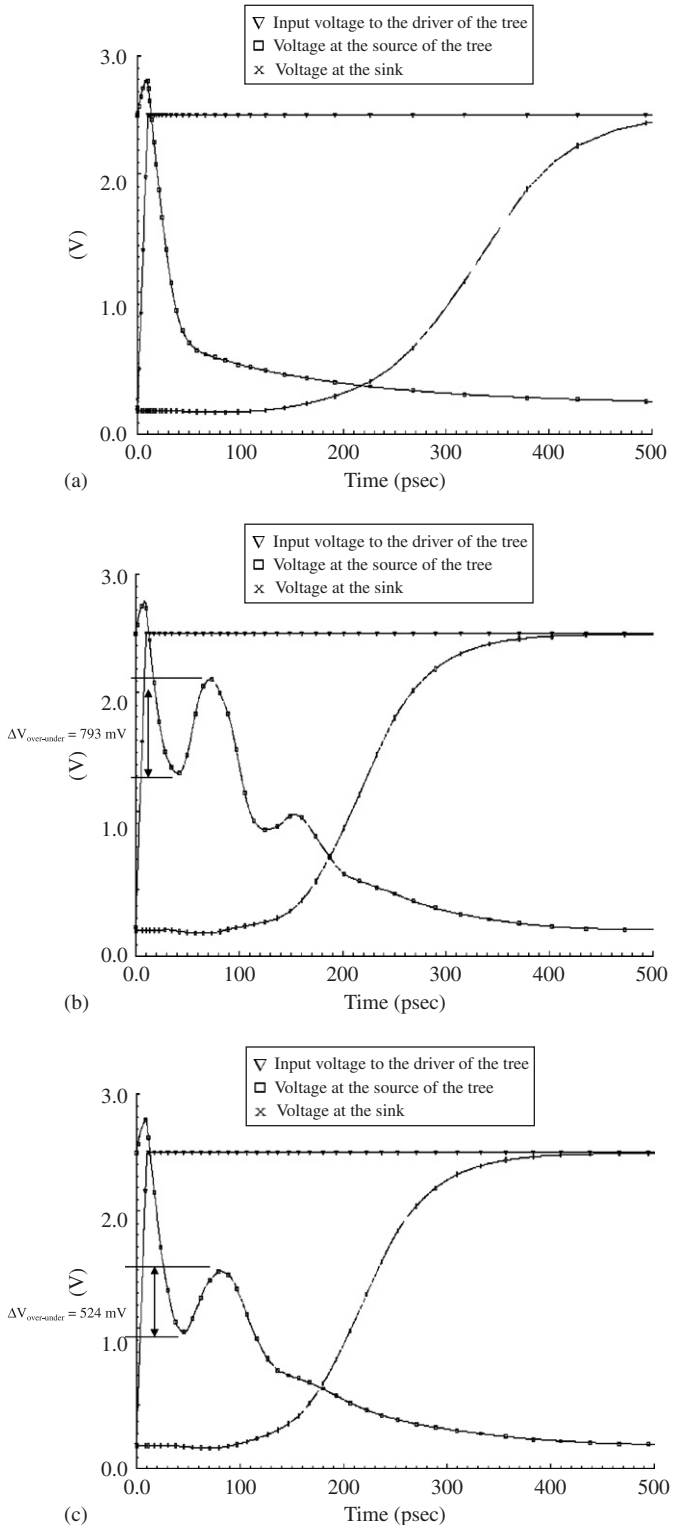

Fig. 9. Waveforms at different nodes within the tree using (a) minimum width lines, (b) uniformly sized lines and, (c) tapered lines.

tapering is applied to size the clock lines. Wide interconnect lines are usually used in clock distribution networks to improve the signal characteristics (propagation delay and signal transition time). A clock distribution network with 64 sinks covering a die area of $3.5 \times 3.5\,mm^2$ is modeled as a distributed *RLC* network. A symmetric capacitive load is assumed at all of the sinks (no clock skew among the sinks). The delay is determined at the sinks of the network for minimum width interconnect lines ($q = 0.5\,\mu m$). The signal waveform at three points; the input and output waveform of the driver of the tree and the sinks (or load) waveform are shown in Fig. 9a. For minimum interconnect width, the line inductance has a negligible effect on the signal waveform.

Uniform interconnect sizing is used to minimize the propagation delay and transition time. Exponential tapering is used to route the interconnect lines within the clock tree. Twice the number of interconnect tracks are used to route the interconnect lines within the clock tree. For wide lines, the interconnect inductance affects the signal waveform. Overshoots and undershoots appear in the signal waveform as shown in Fig. 9b.

Table 6
Propagation delay and $\Delta V_{over-under}$ for different interconnect sizing techniques

		Minimum width	Uniform wire sizing	Tapered wire sizing
Propagation delay	(psec)	325	216	215
$\Delta V_{over-under}$	(mV)	0	793	524
	Reduction (%)	0	0	34%

Wire tapering can be used to achieve the same signal characteristics while reducing the inductive noise [45,46]. The propagation delay and the difference between the first overshoot and undershoot $\Delta V_{over-under}$ which are caused by the ringing effect are listed in Table 6 for the three example circuits.

In Fig. 9a, no overshoots are shown in the waveform since the line width is minimum. The line inductance has no effect on the signal waveform for minimum interconnect width. As shown in Fig. 9c, the difference between the overshoots and undershoots $\Delta V_{over-under}$ caused by the ringing effect decreases from 793 to 524 mV at the source of the tree when tapered lines are used. Tapering the interconnects achieves a reduction in $\Delta V_{over-under}$ of approximately 34%, reducing the inductive noise, thereby improving the signal integrity.

9. Conclusions

The wire shape that produces the minimum signal propagation delay in an *RLC* line is determined in this paper. It is shown that an exponentially tapered interconnect minimizes the time-of-flight of an *LC* line. The general form of the optimum shaping function for an *RLC* line is qe^{px}. The tapering factor p which achieves the minimum delay while lowering the power is determined for different driver and load characteristics.

Wire tapering as compared to uniform wire sizing is more efficient in *RLC* lines than in *RC* lines. The line inductance makes tapering more attractive in *RLC* lines since tapering produces a greater reduction in delay as compared to uniform wire sizing. A reduction in delay of 15% for an *RLC* line as compared to 7% for an *RC* line is achieved when tapering is applied rather than uniform wire sizing.

With a minimum wire width at the far end of the line and an optimum tapering factor, both the propagation delay and power dissipation are reduced. Greater line inductance increases the savings in power in an optimally tapered line as compared to uniform wire sizing. A reduction in power dissipation of 16% for an *RLC* line as compared to 11% for an *RC* line is achieved when exponential tapering is applied rather than uniform wire sizing. Summarizing, tapering improves both the speed and power characteristics of an *RLC* line.

An analytic solution for the tapering factor that produces the minimum transient power exhibits an error of less than 2% as compared to dynamic circuit simulation. The reduction in power increases as the number of driven gates increases. A reduction in the total power dissipation of about 65% is achieved when tapering for minimum power is used rather than uniform sizing with minimum line width.

Tapered wire sizing outperforms both uniform wire sizing and uniform repeater insertion. A reduction in the propagation delay of about 36% is achieved for an example circuit when tapering is used rather than uniform repeater insertion. Wire tapering as compared to repeater insertion becomes more efficient as technology advances, since the reduction in the delay of tapered lines increases.

Wire tapering can improve signal integrity by reducing the inductive noise. Tapered interconnect lines in clock distribution networks can achieve the same signal characteristics of uniformly sized lines, while reducing the reflections along the line. The difference between the signal overshoots in an example clock distribution network decreases by 34% when tapered interconnect is used rather than uniform interconnect that produces the same signal delay and transition time.

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Appendix: Impedance parameters of tapered *RLC* interconnect

Practically, implementing a continuously shaped line is not precisely possible. However, dividing the line into sections of length $l_1 = l/n$, where n is the number of sections, effectively approximates a continuous shape. As technology advances, the minimum interconnect width decreases, allowing a wide range of interconnect widths to be used in sizing the interconnect lines. For precise sizing of the interconnect widths, the difference between the optimum (exponential) size and the approximate implementation becomes negligible.

As shown in Fig. 10, the width of the line sections decreases exponentially as the section approaches the far end, producing an approximation for the optimum shape. For specific geometric dimensions of the signal line and shield lines, the impedance parameters of the line are expressed as functions of the tapering parameters, q and p.

Expressing the line inductance in terms of the dimensions of the wire structure requires knowledge of the current return path. In the coplanar structure shown in Fig. 10, the return path is assumed to be in the adjacent ground lines. This shield structure is common in important

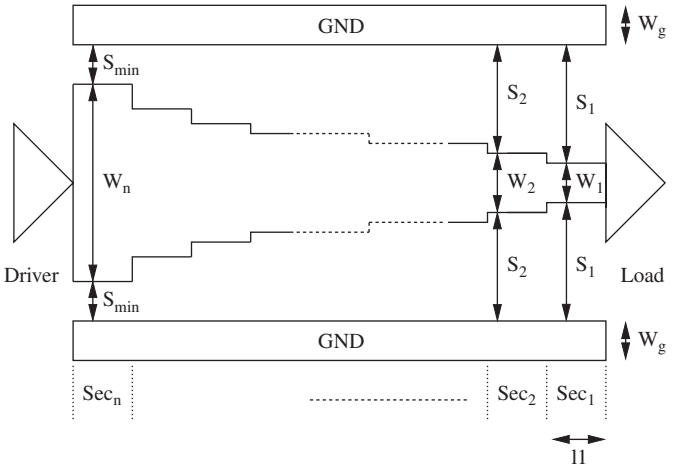

Fig. 10. Coplanar-tapered line.

global interconnects such as clock distribution networks and data busses [36–39].

For a small number of line sections n, the section length is much larger than the other physical dimensions (such as the section width W_i, the separation between the section and the ground S_i, and the line thickness T). Tapering is more effective in long (global) lines (e.g., $l > 1000\,\mu m$) since the line inductance and resistance are significant. These lines are divided into several sections (e.g., $n < 20$), making the ratio between the section length and the other dimensions large (e.g., $l_1/W_i, S_i, T > 100$). Neglecting skin and proximity effects [40] and for $l_1 \gg S_i, W_i$, and T, the line inductance is

$$L_{\text{line}}(q,p) = L_1\left[n\left(A+\frac{3}{2}B(q,p)\right)+\frac{0.22}{l_1}\sum_{i=1}^{n}\frac{1}{W_i(q,p)} - \ln\left(\prod_{i=1}^{n}(qe^{(i-1)pl_1}+T)\right)\right], \tag{10}$$

where

$$L_1 = \frac{\mu_0 l_1}{2\pi},$$

$$A = 0.8637 - 0.5\ln(W_g+T) + \frac{0.11}{(W_g+3T)},$$

$$B(q,p) = \ln SW_g(q,p) - \frac{SW_g(q,p)}{l_1},$$

$$SW_g(q,p) = 2S_{\min} + W_g + qe^{(n-1)pl_1}.$$

The width of each line section is

$$W_i(q,p) = \begin{cases} W_{i-1}e^{pl_1} & \text{for } i>1, \\ q & \text{for } i=1. \end{cases} \tag{11}$$

The inductance of an exponentially tapered line is determined from (10) and compared with the inductance extracted by the field solver FastHenry [41]. The error between the two solutions is less than 0.78% for a tapering factor ranging from 0 to $0.8\,mm^{-1}$.

The total line resistance is

$$R_{\text{line}}(q,p) = R_D l_1 \sum_{i=1}^{n}\frac{1}{W_i(q,p)}, \tag{12}$$

where R_D is the line resistance per square. The total line capacitance is

$$C_{\text{line}}(q,p) = l_1 \sum_{i=1}^{n} C_{\text{Seci}}, \tag{13}$$

where C_{Seci} is the capacitance of each section i per unit length. A closed form expression for C_{Seci} in terms of $W_i(q,p)$ and $S_i(q,p) = S_{\min} + \frac{(W_n - W_i(q,p))}{2}$ is obtained from [34].

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