INTEGRATION, the VLSI journal 48 (2015) 1–9

Contents lists available at ScienceDirect

INTEGRATION, the VLSI journal

journal homepage: www.elsevier.com/locate/vlsi

# Energy efficient adaptive clustering of on-chip power delivery systems ☆

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ARTICLE INFO

*Article history:*
Received 17 December 2013
Received in revised form
13 June 2014
Accepted 16 June 2014
Available online 7 July 2014

*Keywords:*
On-chip power delivery
SMPS
LDO
Power supply co-design

ABSTRACT

Efficient on-chip power delivery is a significant design challenge in heterogeneous real time systems with multiple power domains. The power efficiency of the overall heterogeneous power delivery system has recently been shown to be a strong function of the clustering of the power supplies – the specific configuration in which the power converters and regulators are co-designed. A recursive clustering algorithm with polynomial computational complexity is proposed for a dynamically controllable power distribution system. The algorithm is evaluated on IBM power grid benchmark circuits, yielding up to a 21% increase in power efficiency, and orders of magnitude speedup in runtime.



## 1. Introduction

The delivery of high quality power to the on-chip circuitry with minimum energy loss is a fundamental requirement of all integrated circuits (ICs). The supply voltage, current density, and parasitic impedance, however, do not scale well with each technology generation, degrading the quality of the power delivered from the off-chip power supplies to the on-chip load circuitry. The challenge becomes even more significant as the diversity of modern systems increases and dynamic voltage scaling (DVS) becomes an integrated part of the power management process. Recently, hundreds of on-chip power domains with tens of different supply voltage levels have been reported, and thousand-core ICs are being considered [1–7]. Commercial products integrating tens of power domains with different supply voltages are already commercially available (e.g., Toshiba HD Decoding Chip with 25 power domains [6], and Samsung Exynos 4 Quad Core with 28 LDO regulators [7]). The number of on-chip power domains and voltage supplies is expected to significantly increase. Dynamic voltage scaling and fine grain power management are becoming commonly used within commercial products. ICs will be partitioned into a fine grain structure, and the power will be individually delivered and dynamically managed within each domain. In this configuration, the co-design of many hundreds of on-chip power converters and regulators will be necessary. This paper is intended to provide a methodology for managing power in this environment of many hundreds of distributed on-chip power regulators.

To maintain a high quality power supply despite increasing off- and on-chip parasitic impedances, hundreds of power converters should ultimately be integrated on-chip, close to the loads within‘ the individual multiple power domains [8]. Power efficient switching mode power supplies (SMPS) [9–17] are composed of, among other elements, passive elements that significantly increase the physical size, making distributed regulation impractical. Alternatively, linear power supplies exhibit a relatively small area [18–27], an important characteristic for on-chip integration. The power efficiency of linear power supplies degrades with increasing dropout voltage, making conversion with linear converters power inefficient with large dropout voltages.

Recently, a principle of separation of power conversion and regulation has been introduced [28] that addresses the issue of power efficiency in distributed power supply systems. To optimize the power efficiency of the overall system, power should be primarily converted with a few power efficient switching supplies, delivered to on-chip voltage clusters, and regulated with linear low dropout (LDO) regulators within the individual power domains. The separation principle with multiple voltage clusters is illustrated in Fig. 1 by a heterogeneous power delivery system with multiple power domains, off-chip/in-package/on-chip SMPS power converters, and on-chip LDO power regulators.

Several schemes for heterogeneous power delivery [29,8,30–32] that consider tens to hundreds of on-chip power regulators have

☆This research is supported in part by the Binational Science Foundation under Grant no. 2012139, the National Science Foundation under Grant no. CCF-1329374, and by grants from Qualcomm, Cisco Systems, and Samsung.

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http://dx.doi.org/10.1016/j.vlsi.2014.06.003
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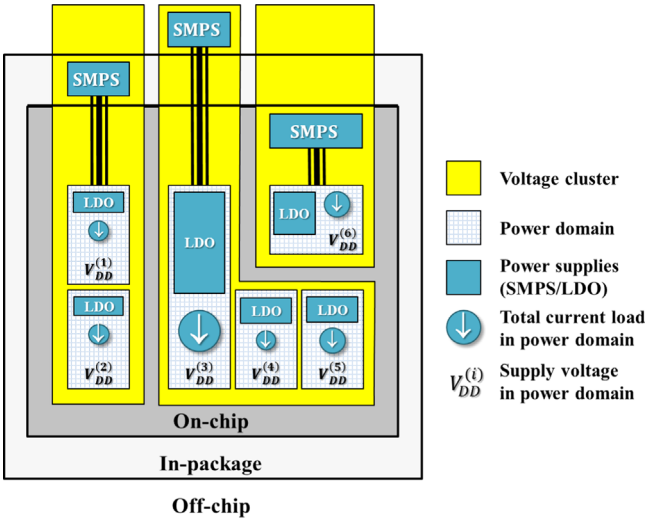


**Fig. 1.** Heterogeneous power delivery with multiple power domains.

recently been proposed. Optimizing the power delivery process in terms of the co-design of the on-chip voltage regulators, decoupling capacitors, and current loads have been proposed in [29,8,30–32]. The stability of a distributed power delivery system where several power supplies drive the same low impedance power grid is an additional concern, and should be addressed as power delivery systems become more complicated with multiple on-chip power regulators operating off the same grid. The co-design of hundreds to thousands of on-chip regulators with multiple switching converters is a new design objective. In energy efficient systems, the voltage and current are dynamically scaled within the individual power domains, affecting the voltage drop across the LDO regulators and the overall efficiency of the power delivery system. Optimal real time clustering of the power supplies decreases the voltage drop within the LDO regulators, increasing overall power efficiency. Exhaustive approaches for clustering power supplies are computationally impractical in DVS systems with hundreds to thousands of power domains. Other existing approaches for on-chip power delivery are *ad hoc* in nature and not optimal. A computationally efficient methodology to co-design in runtime switching converters and on-chip LDO regulators within a heterogeneous system is proposed in this paper, achieving high quality power and efficiency within limited on-chip area. The power savings with the proposed approach are evaluated with IBM power grid benchmarks, demonstrating up to a 24% increase in power efficiency with the proposed voltage clusters. Significant speedup is exhibited with the proposed recursive clustering algorithm, exhibiting polynomial computational complexity.

The rest of the paper is organized as follows. The effects of the number of power supplies, on-chip power supply voltages, and clustering topology on the power efficiency of a static and dynamically controlled heterogeneous power delivery systems are described, respectively, in Sections 2 and 3. A computationally efficient algorithm for optimally clustering power supplies is demonstrated in Section 4. Separation of power conversion and regulations in benchmark circuits is evaluated in Section 5. The paper is concluded in Section 6.

## 2. Power efficiency in heterogeneous power delivery systems

To exploit the different advantages of both switching and linear converters, a heterogeneous power delivery system is considered that converts the power in off-chip or in-package switching power supplies and regulates the on-chip power with compact linear power supplies, minimizing the LDO voltage drops and on-chip power losses. With tens of off-chip or in-package SMPS converters and up to thousands of power domains regulated by individual on-chip LDO regulators, the design complexity of the power delivery system has significantly increased. The design complexity has further increased due to the multiple number and output voltage levels of the SMPS converters.

The concept of clustering in a heterogeneous power delivery system is introduced in this section. The choice of the number and output voltage levels for the SMPS converters, and clustering topology of the on-chip power supplies are also described.

In a power delivery system with thousands of on-chip voltage regulators driven by multiple power converters, several topologies exist to determine the LDO input and SMPS output voltages. The voltage at the output of an LDO is determined by the power requirements of the regulated power domain. The voltage drop within the on-chip voltage regulators is therefore based on the power supply clustering and power domain specifications, affecting the overall power efficiency of a distributed heterogeneous system. For a finite number of power supply clusters, an optimal clustering exists that minimizes the voltage drop across the distributed LDO regulators which maximizes the efficiency of the power delivery system. Efficiently determining the optimum power clustering is the primary objective of this work. The key to determining the optimal clusters is understanding how the efficiency varies with different parameters in a heterogeneous power delivery system. Efficiently determining the optimum power clustering is critical for maximizing the power efficiency of the overall power delivery system.

To explore the efficiency of the proposed heterogeneous power delivery system, consider a system with $S$ off-chip or in-package SMPS converters and $L$ on-chip LDO regulators, delivering power to $L$ power domains with $N$ different supply voltages $\{(V_{DD}^{(i)}, I_{DD}^{(i)})\}_{i=1}^{N}$. Intuitively, LDO regulators that control power domains with similar supply voltages should be assigned to the same voltage cluster. Thus, to explore the power efficiency of a heterogeneous power delivery system, $L=N\geq S$ is assumed. The $i$th SMPS supplies power to $l_i$ LDO regulators ($\Sigma l_i = L = N$), forming the $i$th voltage cluster. The proposed heterogeneous system is illustrated in Fig. 2 with off-chip converters. Note that the SMPS, LDO regulators, and supply voltages are assumed to be ordered such that

$$V_{SMPS}^{(i)} < V_{SMPS}^{(j)} \quad \text{if } \{i<j\}, \tag{1}$$

$$V_{LDO}^{(i,m)} < V_{LDO}^{(j,n)} \quad \text{if } \{i<j\} \text{ or } \{i=j,\ m<n\}, \tag{2}$$

$$V_{DD}^{(i)} < V_{DD}^{(j)} \quad \text{if } \{i<j\}, \tag{3}$$

where $V_{SMPS}^{(i)}$ is the output voltage of the SMPS in the $i$th cluster, $V_{LDO}^{(i,m)}$ is the output voltage of the $m$th LDO in the $i$th cluster, and $V_{DD}^{(j)}$ is the voltage supplied to the $j$th power domain. Thus, the cluster topology $K$ of the power supplies is determined by the distribution of the LDO regulators within the SMPS clusters $K=\{l_i\}_{i=1}^{S}$. Alternatively, to determine the optimal power supply clustering, it is sufficient to determine the number of voltage regulators in each SMPS cluster that minimizes the voltage drops. This observation suggests that the optimal power clustering can be determined from the optimal clusters in systems with fewer power supplies. To recursively determine the optimal power supply clustering, an analytic expression for the power efficiency as a function of the number of power supplies and power domain requirements is required.

The power loss within an LDO increases with larger dropout voltage ($V_{SMPS}^{(i)} - V_{LDO}^{(i,m)}$) and higher quiescent current $I_{LDO,Q}^{(i,m)}$, limiting

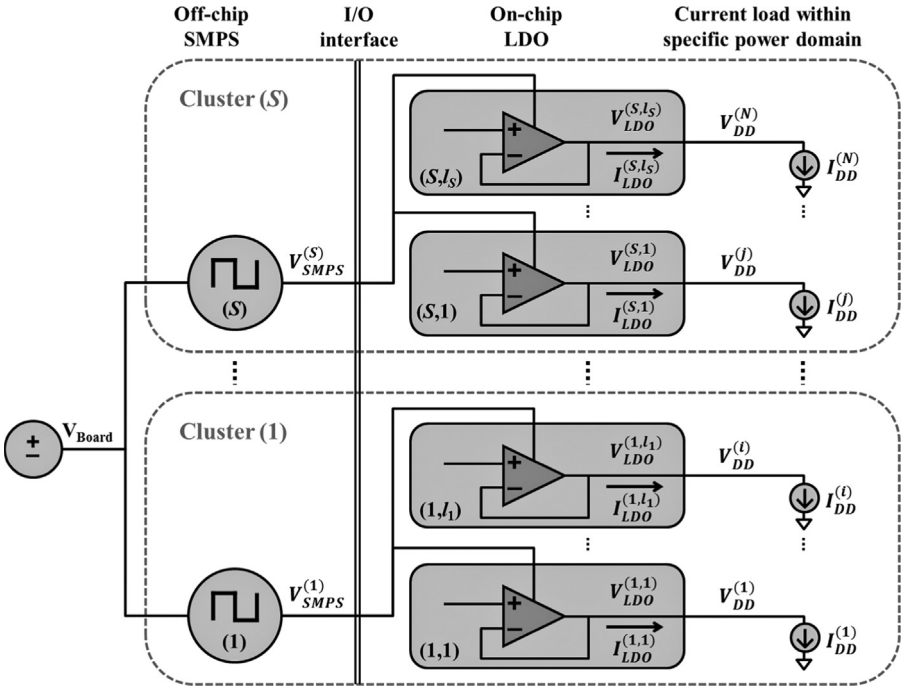


**Fig. 2.** Heterogeneous power delivery system with $S$ off-chip switching converters, $L=N=\Sigma l_i$ on-chip linear regulators, and $N$ on-chip power domains.

the power efficiency of the LDO $\varphi_{LDO}$,

$$\varphi_{LDO}^{(i,m)}=\frac{V_{LDO}^{(i,m)}}{V_{SMPS}^{(i)}}\cdot\frac{I_{LDO,Q}^{(i,m)}}{I_{LDO}^{(i,m)}}. \tag{4}$$

Alternatively, the leakage current within an LDO significantly decreases with adaptive current bias [26,33–35], yielding a current efficiency higher than 99.95% ($I_{LDO}^{(i,m)}+I_{LDO,Q}^{(i,m)}\approx I_{LDO}^{(i,m)}$). The switching power supplies also exhibit high, ideally 100% power efficiency. Thus, the power efficiency of a heterogeneous power delivery system $\varphi$ shown in Fig. 2 is primarily limited by the voltage efficiency of the linear regulators, yielding

$$\varphi=\frac{\sum_{i=1}^{N}V_{DD}^{(i)}I_{DD}^{(i)}}{\sum_{i=1}^{S}(V_{SMPS}^{(i)}\cdot\sum_{m=1}^{l_i}I_{LDO}^{(i,m)})}. \tag{5}$$

Thus, in a heterogeneous system with a specific number of power domains, the efficiency of a power delivery system is a strong function of the number and output voltage of the SMPS converters, respectively, $N$ and $\{V_{SMPS}^{(i)}\}_{i=1}^{S}$, and the clustering topology of the on-chip power supplies $\{l_i\}_{i=1}^{S}$ (see (5)).

The voltage supplied by an LDO to a power domain cannot be stepped up. The output voltage of each SMPS is therefore higher than the output voltage of the LDO regulators within an SMPS cluster, yielding $V_{SMPS}^{(i)}\geq V_{LDO}^{(i,m)}$, $\forall 1\leq m\leq l_i$. Alternatively, the power efficiency of a power delivery system increases with smaller LDO dropout voltages ($V_{SMPS}^{(i)}-V_{LDO}^{(i,m)}$, $\forall 1\leq m\leq l_i$). Thus, to minimize the power loss within the $i$th SMPS cluster, the output voltage of an SMPS is

$$V_{SMPS}^{(i)}=\max_{1\leq m\leq l_i}V_{LDO}^{(i,m)}+V_{Drop}, \tag{6}$$

where $V_{Drop}$ is the minimum dropout voltage across the output transistor of an LDO. The voltage at the SMPS output should be as low as possible as long as the voltage is higher than all of the LDO output voltages within the cluster. The preferred SMPS output voltage in (6) with the power efficiency $\varphi$ described by (5) yields the optimum power efficiency for a specific choice of clusters,

$$\varphi=\frac{\sum_{i=1}^{N}V_{DD}^{(i)}I_{DD}^{(i)}}{\sum_{i=1}^{S}(\max_{1\leq m\leq l_i}V_{LDO}^{(i,m)}+V_{Drop})\sum_{m=1}^{l_i}I_{LDO}^{(i,m)}}. \tag{7}$$

Intuitively, the granularity of the voltage levels supplied to the on-chip regulators increases with a larger number of SMPS converters $S$, lowering the voltage drop across the on-chip distributed regulators. The maximum power efficiency of a heterogeneous power delivery system occurs when $S=L=N$, yielding

$$\varphi=\frac{\sum_{i=1}^{N}V_{DD}^{(i)}I_{DD}^{(i)}}{\sum_{i=1}^{N}(V_{DD}^{(i)}+V_{Drop})I_{DD}^{(i)}}. \tag{8}$$

The 100% power efficiency limit is approached with $V_{Drop}\ll V_{DD}^{(i)}$, $\forall i$.

In a practical heterogeneous power delivery system, the number of SMPS converters is smaller than the number of on-chip LDO regulators ($S<L$). Several options therefore exist to include the on-chip LDO regulators within SMPS clusters, affecting the power efficiency of the overall power delivery system. To illustrate the effect of the clustering topology on the power efficiency of a power delivery system, a heterogeneous system is considered with two switching converters and three linear regulators, supplying equal current $I_{DD}$ to three power domains $\{V_{DD}^{(i)}\}=\{1.8\text{ V}, 1.1\text{ V}, 1.0\text{ V}\}$. Assume $V_{Drop}=0.1$. The power supply clusterings $K_1=\{1,2\}$ and $K_2=\{2,1\}$ for the heterogeneous system with $S=2$ and $L=N=3$ are shown in Fig. 3. The voltage at the output of the switching converters is determined from (6), yielding a power efficiency (from (10)), $\varphi(K_1)=91\%$ and $\varphi(K_2)=80\%$. Determining the optimal clustering of the on-chip power supplies is an important challenge in a heterogeneous power efficient system.

## 3. Dynamic control in heterogeneous power delivery systems

Power domain DVS is an important capability for efficiently managing the power budget in hundred- and thousand-core ICs, further increasing the design complexity of a power delivery system. As the voltage supplied by an LDO to a power domain

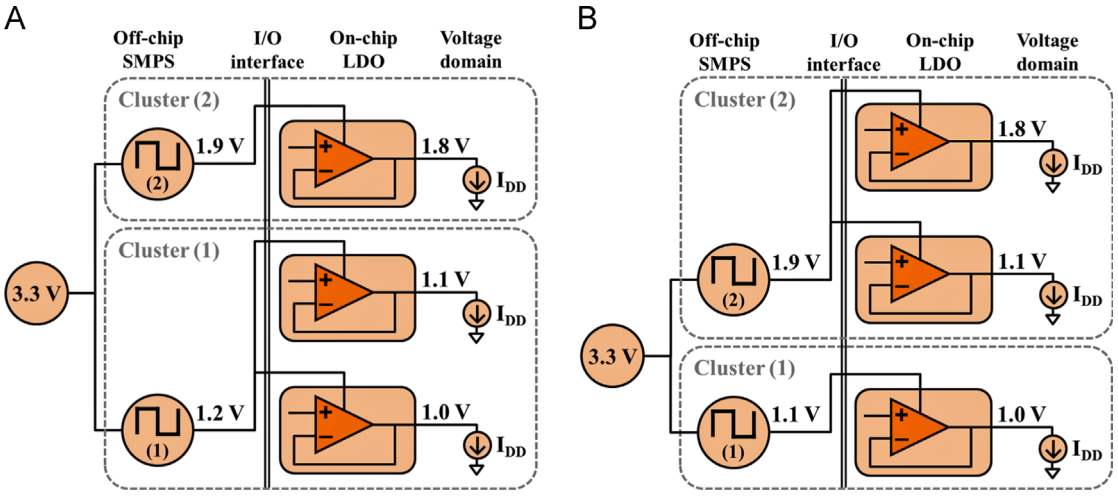


**Fig. 3.** Power supply clusterings for a heterogeneous power delivery system with $S=2$ and $L=N=3$, (a) $K_1=\{1,2\}$ and (b) $K_2=\{2,1\}$.

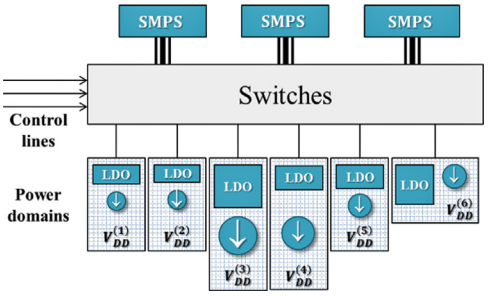


**Fig. 4.** Heterogeneous power delivery with multiple dynamically controllable power domains.

changes, the voltage dropout within the LDO varies. As a result, the power saved during low power operation is dissipated within the regulators. Varying load currents affect the efficiency of the power supplies in a similar way. Thus, in a system with fixed power supply clusters, the energy efficiency of a power delivery system is not optimal. To avoid excessive dissipation of power, SMPS clusters should be dynamically reconfigured in every time slot $\Delta t$ based on the temporarily required voltage and current levels within the individual power domains. A heterogeneous system for real time power management in modern high performance integrated circuits is illustrated in Fig. 4.

The power savings due to both dynamic control over the power delivery process and power switching losses should be considered. The optimal power supply clusters are determined during each control time slot, decreasing the voltage dropout within the regulators and increasing the overall energy efficiency with shorter time slots. Alternatively, the duration of the control time slot $\Delta t$ is inversely proportional to the power dissipated by a MOSFET switch in the $i$th power domain,

$$P_{SW}^{(i)} = f_{sw} \cdot t_{ave} \cdot V_{Off} \cdot I_{DD}^{(i)}, \tag{9}$$

where $f_{sw}=1/\Delta t$ is the system switching frequency, $t_{ave}$ is the MOSFET average on/off time, $V_{Off}$ is the switch off voltage, and $I_{LDO}^{(i,m)}+I_{LDO,Q}^{(i,m)} \approx I_{LDO}^{(i,m)}$. Power losses of the proposed system, therefore, increase with higher switching frequencies, and are considered here to determine the preferred duration of the control time slot $\Delta t=1/f_{sw}$. The optimal power efficiency in (5) with switching power losses is

$$\varphi = \frac{\sum_{i=1}^{N} V_{DD}^{(i)} I_{DD}^{(i)}}{\sum_{i=1}^{S}(V_{SMPS}^{(i)} + f_{sw} \cdot t_{ave} \cdot V_{Off}) \sum_{m=1}^{l_i} I_{LDO}^{(i,m)}}. \tag{10}$$

Both analog and digitally controlled LDO regulators with voltage drops as low as 0.15 V down to 0.05 V have recently been reported [36,37,34,38], yielding $V_{Drop} \approx V_{Off}$. Thus, for a sufficiently long control time slot $\Delta t = 1/f_{sw} \gg t_{ave}$, the power dissipated within the switches is significantly lower than the power dissipated within the LDO and can therefore be neglected. Modern MOSFET switches are capable of switching within tens of nanoseconds [39], exhibiting a practical target for the $\Delta t \gg t_{ave}$ requirement in dynamically controlled heterogeneous systems. Alternatively, a real time power delivery management system poses a significant computational challenge. Thus, a computationally efficient method to co-design the on-chip power supplies in modern high performance circuits is required.

## 4. Computationally efficient power supply clustering

The optimal clustering topology with minimum power losses can be obtained by exhaustively comparing the power efficiency $\varphi$ (see (10)) for all possible clusterings, and choosing the configuration with the maximum efficiency. The number of possible clusterings, however, grows exponentially with $S$, producing a computationally infeasible solution. To efficiently determine the preferable power supply clusters, an alternative computationally efficient solution is required. A power supply clustering algorithm with $\mathcal{O}(N^2 \cdot S)$ is described in this section. A recursive analytic expression is provided for power supply clustering with $L$ LDO regulators and $S$ SMPS in smaller power delivery systems ($l<L$ LDO regulators and $s=S-1$ SMPS). Recursive power supply clustering, similar to exhaustive power supply clustering, yields the optimal power supply clusters.

The key idea behind the proposed algorithm is determining the number of voltage regulators within a high voltage SMPS cluster in $\mathcal{O}(N)$. Once the number of LDO regulators in a high voltage SMPS cluster is determined, the problem of power supply clustering is reformulated for the remaining LDO regulators and a smaller number of SMPS clusters. To exemplify the proposed solution, consider a heterogeneous system with three switching converters ($S=3$) and five linear regulators ($L=5$), supplying equal current $I_{DD}$ to five power domains ($N=5$) $\{V_{DD}^{(i)}\}=\{3.3\text{ V}, 2.6\text{ V}, 1.8\text{ V}, 1.6\text{ V}, 1.0\text{ V}\}$. The optimum power supply clustering $K_{OPT}(5,3)=\{l_1,l_2,l_3\}$, $\Sigma l_i=5$ is determined recursively based on the number of LDO regulators in the high voltage cluster $l_3$, and lower order optimal supply clustering $K_{OPT}(4,2)$, $K_{OPT}(3,2)$, and $K_{OPT}(2,2)$. A single recursive step is illustrated in Fig. 5, demonstrating three possible alternatives for clustering with one ($l_3=1$), two ($l_3=2$), and three

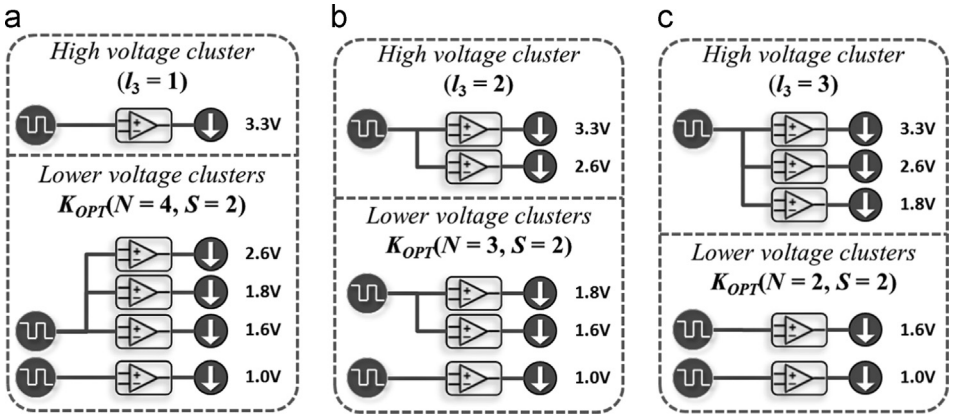


**Fig. 5.** A single step of the recursive power supply clustering algorithm for a heterogeneous power delivery system with $S=3$ and $L=N=5$, (a) a single LDO ($l_3=1$), (b) two LDO regulators ($l_3=2$), and (c) three LDO regulators ($l_3=3$) in a high voltage SMPS cluster.

($l_3=3$) LDO regulators within the high voltage SMPS cluster. Given the lower order clustering $K_{OPT}(4,2)$, $K_{OPT}(3,2)$, and $K_{OPT}(2,2)$, the optimum clustering $K_{OPT}(5,3)$ is determined with linear computational complexity by comparing the power efficiencies $\varphi\{K_{OPT}(4,2),1\}$, $\varphi\{K_{OPT}(3,2),2\}$, and $\varphi\{K_{OPT}(2,2),3\}$, and choosing the clustering topology that minimizes the power losses.

For a general clustering algorithm, consider clustering $L$ on-chip LDO regulators within $S$ SMPS clusters to deliver power to $L$ power domains with $N=L$ different supply voltages. The optimal clustering topology of a system with $N$ different supply voltages and $S$ SMPS $K_{OPT}(N,S)=\{l_i\}_{i=1}^{S}$, $\sum l_i = N$ is determined recursively by

$$K_{OPT}(N,S)=\{K_{OPT}(N-n_0,S-1),l_S\}, \tag{11}$$

with the initial conditions,

$$K_{OPT}(N,2)=\{N-l_S,l_S\}, \tag{12}$$

$$K_{OPT}(N,S=N)=\{1,2,\ldots,N\}, \tag{13}$$

where $1\le l_S\le(N-S)$ is the number of LDO regulators in the high voltage SMPS cluster. To maximize the overall power efficiency of the system, the number of LDO regulators in the last SMPS cluster is

$$\varphi(K_{OPT}(N,S))=\max_{l_S}\varphi(\{K_{OPT}(N-l_S,S-1),l_S\}). \tag{14}$$

Once the power supply clusters are recursively determined, the maximum voltage level within each SMPS cluster determines the SMPS output and LDO input voltage based on (6). Pseudo-code of the algorithm for determining the LDO input voltages based on the proposed clustering is shown in Fig. 6.

The LDO input voltages in a system with a single ($S=1$) switching converter and the maximum number of SMPS ($S=N$) are determined, respectively, at lines 2–4 and 5–7. To determine the optimal clustering of a general system with ($1<S<N$) switching converters, lines 8 through 44 are executed. The LDO input voltages for all of the systems with $s\le S$ SMPS and $l\le L$ LDO regulators are determined progressively and stored in matrix $all\_V_{LDO}$. The matrix is allocated and initiated based on (12) and (13) at lines 9–19. The voltage levels at the LDO input voltages are determined in a loop (see lines 21–22) for systems with a progressively increasing number of power supplies. All of the high voltage cluster configurations with a different numbers of LDO regulators are determined at lines 30–32. The power efficiency of different configurations is compared at lines 33–37, determining the most power efficient system. The number of efficiency comparisons required to determine the optimal clustering $K_{OPT}(N,S)$ given all of the optimal clusterings of lower order $K_{OPT}(n<N,s<S)$ is $N-S$. The computational complexity to determine the most power efficient clusters with $N=L$ LDO regulators and $S$ SMPS converters is therefore

$$\sum_{s=1}^{S}\left(\sum_{n=s}^{N}\mathcal{O}(n-s)\right)=\mathcal{O}(N^2\cdot S),\quad N\ge S. \tag{15}$$

To estimate the power efficiency of the recursive power supply clustering algorithm, a heterogeneous power delivery system with 25 supply voltage levels ($N=25$) and 25 on-chip linear regulators ($L=25$) is considered. The number of off-chip switching converters is evaluated for 1 to 25 converters ($1\le S\le 25$). A voltage drop of $V_{Drop}=0.1$ V, and 100 random profiles of domain voltages and currents of, respectively, 0.5–2 V and 0.5–3.5 A, are considered. The maximum power efficiency with an average domain voltage and current of, respectively, 1.25 V and 2 A is evaluated based on (8), yielding 93% power efficiency for $S=25$. The power efficiency of a heterogeneous power delivery system with the power supply clusters determined by a recursive analysis is illustrated in Fig. 7. As expected, a maximum 93% power efficiency is achieved for $S=N$. An average power efficiency above 82% is demonstrated for $S\ge 3$. Thus, the power efficiency of a heterogeneous power delivery system with an optimal voltage clustering exhibits a reasonable power efficiency, despite only three switching converters. The efficiency increases rapidly and saturates with additional SMPS converters. The load current of a single SMPS converter decreases with an increasing number of SMPS converters, degrading the power efficiency of both the converter [4] and the overall power delivery system. Thus, an excessive number of off-chip or in-package converters is avoided with the proposed power supply clustering algorithm, producing a power and area efficient system of power converters and regulators.

## 5. Co-design of power supplies in circuit benchmarks

The efficiency of a heterogeneous power delivery system with separation of power conversion and regulation is compared in this section with other power delivery approaches. Several test cases have been evaluated based on IBM power grid benchmarks [40] to determine the power efficiency with and without power separation. The test cases and simulation results are described in Section 5.1. Power delivery with on-chip regulation in circuits with multiple power domains [30] is considered in Section 5.2.

### 5.1. Power supply clustering of IBM power grid benchmarks

Five test cases have been considered based on IBM power grid benchmarks [40] to evaluate the efficiency of the power separation

```
function V_LDO(1 : N) = Clustering(V_DD(1 : N), I_DD(1 : N), S, V_Drop)
if S == 1
  % There is only one cluster
   V_LDO(:) = max{V_DD(:)} + V_Drop
else if S == N
  % The number of clusters equals the number of the voltage levels
   V_LDO(:) = V_DD(:) + V_Drop
else
  % Initiate a matrix to store all the clusters for lower order systems:
  % all_LDO_input_voltages(s, l, :) stores all the input voltages for a
  % system with s SMPSs and l LDOs.
  all_ V_LDO(:) = zeros(S, L = N, N)
  % Update the initial conditions based on (10) and (11)
  for l = 1 : N
    all_ V_LDO(1, l, 1 : l) = ones(1, l) · (V_DD(l) + V_Drop)
  end
  for s = 1 : S
    all_ V_LDO(s, s, 1 : s) = V_DD(1 : s) + V_Drop
  end
  % Find all the lower order clusters for  s ≤ S SMPSs and l ≤ L LDOs
  for s = 2 to S
    for l = s + 1 to N
      V_LDO,OPT = zeros(1, N)
      η_OPT = 0
      for l_s = 1 to l – s + 1
        % l_s is the number of LDOs in the highest voltage cluster,
        % with the input voltage V_DD(l)
        % (l – l_s) is the number of LDOs in the rest (s – 1) clusters,
        % with the input voltage levels as fetched from all_V_LDO
        V_LDO,TMP(1 : l – l_s) = all_ V_LDO(s – 1, l – l_s, :)
        V_LDO,TMP(l – l_s + 1 : l) = V_DD (l) + V_Drop
        η_TMP = 100 · ∑[V_DD (1 : l) · I_DD (1 : l)] / ∑[V_LDO,TMP(1 : l) · I_DD (1 : l)]
        if (η_TMP > η_OPT)
          % Remember the clustering with the highest efficiency
          V_LDO,OPT = V_LDO,TMP
          η_OPT = η_TMP
        end
      end
      % Update all_V_LDO with the optimal clusters for s SMPSs and l LDOs
      all_ V_LDO(s, l, :) = V_LDO,OPT
    end
  end
  V_LDO(:) = all_ V_LDO(S, L = N, :)
end
```

**Fig. 6.** Algorithm to determine LDO input voltages for power efficient clustering.

principle in circuits with hundreds of power domains and tens of different supply voltages. The voltage map of a $V_{DD}$ and $V_{GND}$ $M$ 6 metal layer at normalized $(x,y)$ locations is depicted in Fig. 8(a). The actual voltage drop in the metal layer $M$ 6 is $V_{DD}-V_{GND}$, as shown in Fig. 8(b) for the *ibmpg* 1 benchmark. Different circuits in *ibmpg* 1 operate with different supply voltages, varying from 0.5 V to 1.5 V. A total number of 66 voltage domains with voltage levels ranging from 0.5 V to 1.8 V with a 0.02 volt shift $\{V_{DD}^{(i)} = 0.5\ V + i \cdot 0.02\ V\}_{i=0}^{i=65}$ is considered in this analysis. Each of the benchmarks is partitioned into voltage domains based on the voltage maps, and the area of each domain is determined. The current within a benchmark circuit is assumed to be uniformly distributed. The current load of a domain is therefore assumed to be proportional to the area of the domain. The voltage within each domain is regulated by an LDO, ensuring that the total number of on-chip LDO regulators is the same as the number of voltage domains. To illustrate the process in which a test case is generated, specifications for several voltage domains in *ibmpg* 1 are listed in Table 1. The total number of nodes processed in *ibmpg* 1 is 30,027. A total current of 10 A is assumed to be consumed by the circuits represented by *ibmpg* 1.

Test cases for the IBM benchmarks, *ibmpg* 2, *ibmpg* 3, *ibmpgnew* 1, and *ibmpgnew* 2, are generated in a similar way. The proposed power supply clustering algorithm is demonstrated in Matlab and applied to all of the test cases on a multi-core system with four Intel(R) Core

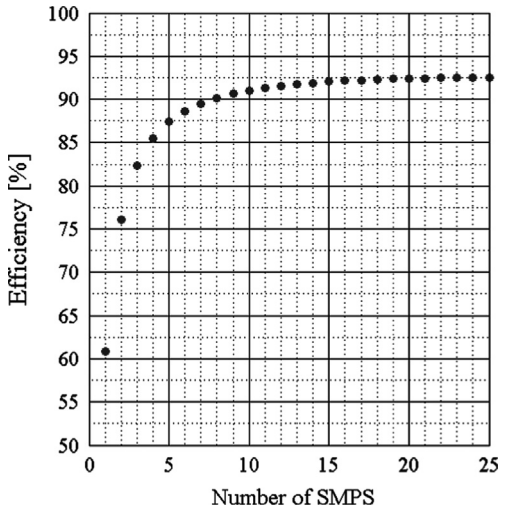


**Fig. 7.** Power efficiency of heterogeneous power delivery system based on a recursive power supply clustering algorithm.

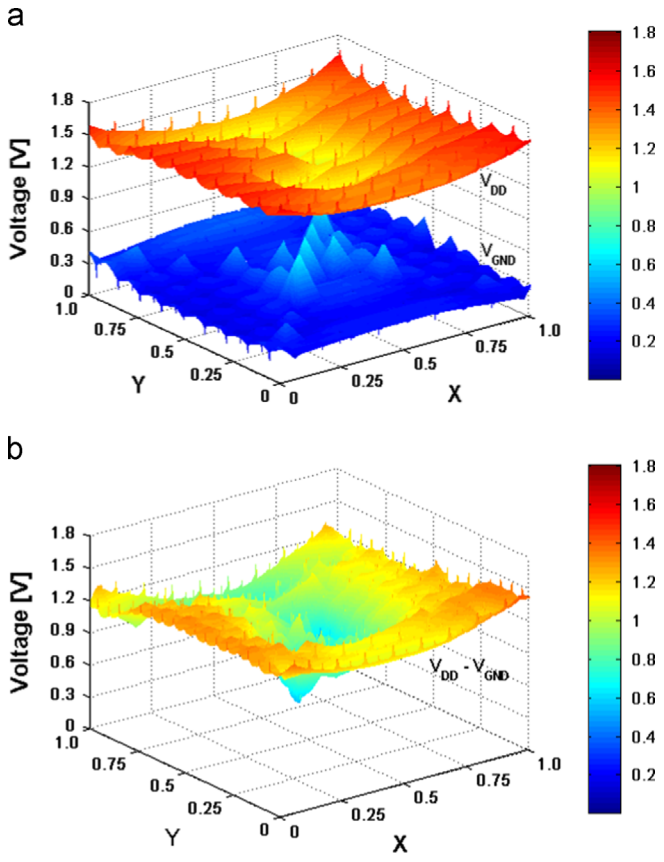


**Fig. 8.** Test case *ibmpg* 1 with (a) $V_{DD}$ and $V_{GND}$ voltage map, and (b) $V_{DD}-V_{GND}$ voltage drop across the circuits in metal layer *M* 6.

(TM) i3-2120 CPU @ 3.30 GHz processors and 2,498 MB memory. A voltage drop of 0.1 V within an LDO is assumed. The power grid specifications and simulation results with and without power supply clustering are listed in Table 2.

Power clustering with the proposed algorithm exhibits orders of magnitude shorter CPU time than the exhaustive approach. Those power grids with a range of LDO output voltages up to 0.20 V (*ibmpgnew* 1 and *ibmpgnew* 2) exhibit a high power efficiency of 93% despite only two SMPS clusters. The power efficiency of these grids increases by 2.5% as compared to a power delivery system without power separation. Increasing the power efficiency in those power grids with a large number of SMPS clusters (94% with ten switching converters) requires excessive area. Alternatively, the *ibmpg* 1 benchmark exhibits a wider range of LDO output voltages, 0.5–1.5 V, and therefore, a low power efficiency of 68% without power supply clustering. The effectiveness of power separation is shown to be significant in *ibmpg* 1 with a 10.2% and 21.1% increase in power efficiency with, respectively, $S=2$ and $S=10$ SMPS clusters as compared to $S=1$. Separation of power conversion and regulation is therefore particularly important in those systems with a wide range of on-chip supply voltages and voltage drops. To provide high quality power in dynamically scaled multi-voltage circuits, the efficiency of the power supply clustering is dynamically evaluated. The proposed power supply clustering algorithm exhibits an order of magnitude smaller CPU runtime as compared with the exhaustive method, while providing identical clusters. With the proposed approach, the switching converters and linear regulators can be co-designed in runtime for power and area efficient management of the energy budget.

**Table 1**
Power grid specifications for 0.8 V, 1.0 V, 1.2 V, 1.4 V, and 1.6 V domains based on *ibmpg* 1 test case.

| Voltage domain id | 15 | 25 | 35 | 45 | 55 |
|---|---|---|---|---|---|
| Supply voltage (V) | 0.8 | 1.0 | 1.2 | 1.4 | 1.6 |
| Number of nodes | 636 | 820 | 1297 | 19 | 0 |
| Area (%) | 2.12 | 2.73 | 4.320 | 0.062 | 0 |
| Supply current (mA) | 212 | 273 | 432 | 6.2 | 0 |

### 5.2. Power supply clustering and existing power delivery solutions

The separation principle is illustrated in circuits $C_1$ and $C_2$ with multiple power domains $V_{DD}^{(A)}=1.4$ V, $V_{DD}^{(B)}=1.2$ V, and $V_{DD}^{(C)}=1.0$ V, and the on-chip voltage conversion and regulation scheme used in [30]. A maximum voltage drop ($V_{Drop}$) of 5% of the input voltage at the I/O interface ($V_{SMPS}$) is allowed at POLs within all of the power domains ($V_{Drop}\leq 0.05V_{SMPS}$). The total area of the circuits, $C_1$ and $C_2$, is similar. The area of $C_1$ is dominated by the low power domain *C*, while the area of $C_2$ is dominated by the high performance power domain A. The current density *J* and normalized area per power domain are listed in Table 3 for both circuits. To support on-chip voltage conversion and regulation within the power domains *A*, *B*, and *C* in $C_1$ ($C_2$), a single input voltage $V_{SMPS}=1.45$ V ($V_{SMPS}=1.50$ V) is used in the original configuration without power separation [30]. Note that the input voltage $V_{SMPS}=1.45$ V ($V_{SMPS}=1.50$ V) is higher than the highest supply voltage $V_{DD}^{(A)}=1.4$ V to maintain the required margin for on-chip voltage regulation with a reasonable number of 50 (60) on-chip LDO regulators in $C_1$ ($C_2$). Alternatively, the power can be converted separately off-chip or in-package for each power domain and regulated on-chip within each power domain. The input voltages and power efficiency for on-chip voltage regulation with and without separation of power conversion and regulation is listed in Table 4 for both circuits. In the proposed configuration, three off-chip or in-package SMPS supply three different voltages, $V_{SMPS}^{(A)}=1.47$ V, $V_{SMPS}^{(B)}=1.26$ V, and $V_{SMPS}^{(C)}=1.05$ V to, respectively, power domains *A*, *B*, and *C*, yielding a power efficiency as high as 95.2%. To regulate the on-chip voltage with the required number of LDO regulators, the voltage at the output of each SMPS is designed with a margin of 5% of the required on-chip supply voltage ($V_{DD}^{(i)}=1.05V_{DD}^{(i)}$). Without separating power conversion and regulation, the choice of off-chip supply voltage is determined by the supply voltage in the high performance power domain, exhibiting a higher voltage drop ($V_{SMPS}-V_{DD}^{(C)}=0.45$ V in $C_1$) and a lower power efficiency (77.3% in $C_1$) in low power circuits. Alternatively,

**Table 2**
Power efficiency in circuits with and without separation of power conversion and regulation.

| Benchmark | Voltage domains/LDO regulators | | Power efficiency with $S$ voltage clusters (%) | | | | | CPU time [s] | |
|---|---|---|---|---|---|---|---|---|---|
| | Number | Voltage range (V) (MAX (V) − MIN (V)) | Without power separation $S=1$ $S=1$ | With power separation | | | | Proposed clustering | Exhaustive clustering |
| | | | | $S=2$ | $S=3$ | $S=5$ | $S=10$ | | |
| ibmpg1 | 49 | 1.46 − 0.50 = 0.96 | 68.093 | 78.301 | 82.421 | 86.484 | 89.231 | 18.268 | > 100,000 |
| ibmpg2 | 21 | 1.52 − 1.12 = 0.40 | 77.222 | 86.953 | 89.193 | 90.955 | 92.109 | 0.641 | > 100,000 |
| ibmpg3 | 15 | 1.70 − 1.44 = 0.26 | 88.603 | 91.905 | 92.819 | 93.578 | 94.116 | 0.195 | > 100,000 |
| ibmpgnew1 | 11 | 1.72 − 1.52 = 0.20 | 90.342 | 92.859 | 93.471 | 94.070 | 94.267 | 0.083 | 113.893 |
| ibmpgnew2 | 11 | 1.72 − 1.52 = 0.20 | 90.388 | 92.852 | 93.487 | 94.070 | 94.269 | 0.080 | 108.238 |

**Table 3**
Parameter setup for circuits $C_1$ and $C_2$.

| Power domain | $J$ (A/unit area) | Normalized area | |
|---|---|---|---|
| | | Circuit $C_1$ | Circuit $C_2$ |
| $A$ | 2/3 V | 1 | 6 |
| $B$ | 1/2 V | 2 | 2 |
| $C$ | 1/3 V | 6 | 1 |

**Table 4**
On-chip voltage regulation with and without separation of power conversion and regulation.

| Circuit | Without power separation [30] | | With power separation (current work) | | | |
|---|---|---|---|---|---|---|
| | $V_{SMPS}$ (V) | $\varphi$ (%) | $V_{SMPS}^{(A)}$ (V), | $V_{SMPS}^{(B)}$ (V), | $V_{SMPS}^{(C)}$ (V) | $\varphi$ (%) |
| $C_1$ | 1.45 | 77.3 | 1.47 | 1.26 | 1.05 | 95.2 |
| $C_2$ | 1.50 | 90.7 | 1.47 | 1.26 | 1.05 | 95.2 |

an enhanced choice of $V_{SMPS}^{(i)}$ voltages is possible by separating power conversion and regulation, exhibiting a lower voltage drop ($V_{SMPS}^{(i)} - V_{DD}^{(i)} \leq$ 0.07 V in $C_1$) and a higher power efficiency (95.2% in $C_1$).

## 6. Conclusions

On-chip power regulation and delivery are necessary for delivering high quality power to modern high performance integrated circuits. Dynamic power management is employed in modern systems to efficiently manage the energy budget. For efficient adaptive power management, power should be converted with efficient power converters and dynamically regulated with ultra-small on-chip regulators. To avoid excessive usage of switching converters, the power efficiency as a function of the number of SMPS clusters is determined.

Dynamically co-designing tens of power converters with hundreds to thousands of on-chip regulators is a primary concern in an energy efficient power delivery system. An exhaustive solution that determines the on-chip power supply clusters with the highest power efficiency is, however, computationally inefficient and impractical in real time systems. Thus, an algorithm to recursively cluster a heterogeneous power supply system with polynomial computational complexity is presented. An order of magnitude speedup is exhibited with the proposed algorithm as compared with exhaustive clustering. Up to a 21% increase in power efficiency is demonstrated on IBM benchmarks with more than two switching converters. A dynamically controlled heterogeneous integrated power delivery system is shown to be a computationally and power efficient alternative to existing *ad hoc* methodologies that employ either switching or linear on-chip power supplies.

To achieve a power efficient system, power should be primarily converted off-chip, in-package, and/or on-chip with power efficient switching supplies, and regulated with ultra small linear low dropout regulators at the point-of-load. To dynamically co-design tens of power converters with hundreds to thousands of on-chip regulators, the optimal clustering of the on-chip LDO regulators within the SMPS voltage clusters is determined that maximizes in runtime the power efficiency of the overall power delivery system.

A systematic methodological solution is required that integrates the proposed clustering algorithm within an on-chip power delivery and management platform. Different architectures, analog circuits for sensing, sophisticated routing algorithms, and dynamic control of the on-chip power in terms of the quality of power and efficiency of the overall power delivery system are topics of future interest.

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