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Scaling trends of power noise in 3-D ICs

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ABSTRACT

Power supply noise in three-dimensional integrated circuits (3-D ICs) considering scaled CMOS and through silicon via (TSV) technologies is the focus of this paper. A TSV and inductance aware cell-based 3-D power network model is proposed and evaluated. Constant TSV aspect ratio and constant TSV area penalty scaling, as two scenarios of TSV technology scaling, are discussed. A comparison of power noise among via-first, via-middle, and via-last TSV technologies with CMOS scaling is also presented. When the TSV technology is a primary bottleneck in high performance 3-D ICs, an increasing TSV area penalty should be adopted to produce lower power noise. As a promising TSV technology, via-middle TSVs are shown to produce the lowest power noise with CMOS technology scaling.

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1. Introduction

With the increasing requirement for high performance integrated circuits (ICs), a greater number of transistors is integrated onto a die and the die area has become larger [1,2]. CMOS technology scaling supports high integration levels, leading to greater on-chip average and transient currents [3,4]. To achieve larger ICs and higher speeds, the global interconnect has become longer and operating frequencies have increased, producing higher resistance and inductance within power distribution networks [5,6]. Both *IR* drops and *L di/dt* noise within the power network have therefore increased. Increasing power supply noise can lower performance and/or produce faulty circuit operation. Moreover, scaling the global interconnect produces longer signal delays and greater crosstalk, which offsets many of the advantages of technology scaling. The increase in performance will therefore soon saturate with technology scaling [7,8]. New techniques are required to increase performance.

Three-dimensional integrated circuits (3-D ICs) exploit the vertical dimension, providing a promising technique to extend scaling [9]. Vertical integration in 3-D ICs yields smaller die area and higher levels of integration. In addition, short vertical TSVs lead to both higher system performance and lower power dissipation. 3-D stacked layers also make heterogeneous integration possible, enhancing the functionality of modern systems. The key technology to achieve the advantage of 3-D ICs is the through silicon vias (TSVs), the vertical metal connections passing through the silicon wafer between two adjacent layers [9]. In terms of functionality, TSVs can be categorized as signal, thermal, and P/G TSVs. P/G TSVs are the type of TSV considered in this work.

The introduction of P/G TSVs in 3-D power distribution networks leads to significant challenges in managing power noise in 3-D ICs. As important components of a 3-D power network, P/G TSVs introduce additional *IR* drop and *L di/dt* noise. In addition, power distribution networks interact with different device layers through the P/G TSVs. The analysis presented in this paper of power noise in 3-D TSV-based ICs considering TSV technology scaling is intended to support the 3-D power network design process. Parameters such as the TSV radius, length, pitch, and distribution topologies can affect power noise in 3-D systems. A physical model and circuit model of a TSV are shown in Fig. 1.

The rest of this paper is organized as follows. In Section 2, two scenarios for scaling TSVs are proposed to provide an intuitive understanding of the different methods for scaling interconnect and related effects on on-chip power noise. Inductive coupling effects of TSVs among large P/G TSV arrays are reviewed in Section 3. A discussion of TSV distribution topologies from the perspective of equivalent inductance is also provided. In Section 4, a closed-form expression to calculate the inductance of a TSV within a TSV array is presented. In Section 5, a cell-based 3-D power distribution network model is proposed to effectively evaluate power noise in 3-D systems. In Section 6, simulation results for both TSV

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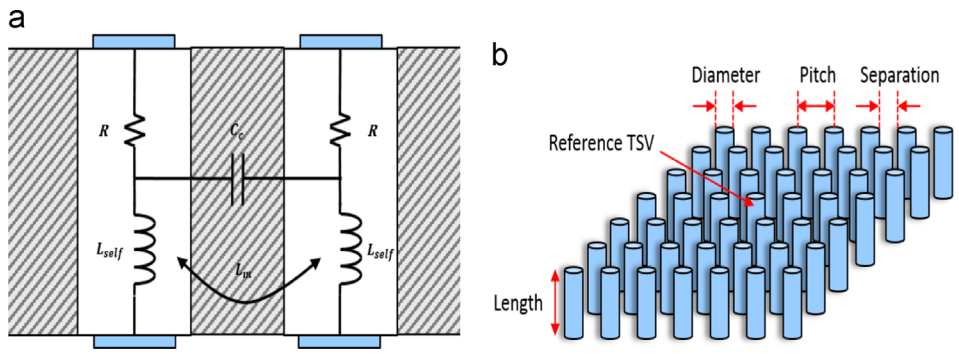


Fig. 1. TSV, (a) circuit model, and (b) physical model.

and CMOS scaling are presented. Tradeoffs among different TSV parameters and related design implications are also discussed. The paper is concluded in Section 7.

2. Analysis of TSV scaling behavior

3-D integration is a promising technique to increase performance and reduce power consumption in modern systems. Power noise however is a significant concern in 3-D ICs. An analysis of scaling trends of power noise is helpful to efficiently develop 3-D power networks and to make tradeoffs between *IR* drop and *L di/dt* noise. Technology scaling in 3-D ICs refers to active device scaling, interconnect scaling, and TSV scaling. As shown in Fig. 2, the size (e.g., length, radius, and pitch) of the TSVs is decreased to achieve a higher density of communication between each layer. The geometric parameters of a TSV, as predicted by ITRS, are listed in Table 1 [6], which describes the gradual trend of the minimum geometric parameters of a TSV from 2011 to 2018. The aspect ratio (*AR*) listed in Table 1 refers to the ratio of the length and diameter of a TSV, *L*/*D*.

The TSV impedance is determined based on geometric parameters such as the length (*L*), pitch (*P*), radius (*r*), and aspect ratio, affecting power noise (*IR* and *L di/dt*) in 3-D TSV-based ICs [10]. Based on the closed-form expressions of the electrical parameters of 3-D via [10], the inductance of a TSV is

$$DC: \begin{cases} L_{self} = L \cdot \alpha \frac{\mu_0}{2\pi}\left[\ln\left(\frac{1+\sqrt{1+\left(\frac{1}{2b}\right)^2}}{\frac{1}{2b}}\right)+\frac{1}{2b}-\sqrt{1+\left(\frac{1}{2b}\right)^2}+\frac{1}{4}\right] \\ L_{mutual} = L \cdot \beta \frac{\mu_0}{2\pi}\left[\ln\left(\frac{1+\sqrt{1+a^2}}{a}\right)+a-\sqrt{1+a^2}\right], \end{cases} \tag{1}$$

$$f_{asym}: \begin{cases} L_{self} = L \cdot \alpha \frac{\mu_0}{2\pi}\left|\ln(4b)-1\right| \\ L_{mutual} = L \cdot \beta \frac{\mu_0}{2\pi}\left[\ln\left(\frac{1+\sqrt{1+a^2}}{a}\right)+a-\sqrt{1+a^2}\right], \end{cases} \tag{2}$$

$$a = \frac{P}{L}, \tag{3}$$

$$b = \frac{L}{D}, \tag{4}$$

$$c = \frac{r}{P}, \tag{5}$$

where *r*/*P*, *L*/*D*, and *P*/*L* are introduced to provide greater intuition into scaling behavior. The physical characteristics of these parameters are listed in Table 2.

Based on (1)–(5), L_{self} is dependent on the TSV length and *L*/*D*, and L_{mutual} is dependent on the TSV length and *P*/L. During an analysis of power noise in 3-D systems, L_{self} is dependent on the specific *AR* scenario. Alternatively, L_{mutual} can be determined for specific *P*/*L* scenarios. The parameter *P*/*L*, however, does not provide any physical meaning. *P*/*L* can be determined by *L*/*D* and *r*/*P*. The TSV area penalty (*r*/*P*) is therefore introduced here to make the power noise analysis process more intuitive for 3-D systems. The TSV area penalty is determined by the ratio of the TSV cross-sectional area to the 3-D IC footprint [11]. As the IC footprint becomes larger, the performance advantages brought by TSVs are less. The area penalty of a TSV is an important design criterion in 3-D integration.

Table 1
Roadmap of global interconnect for 3-D ICs [5].

TSV parameters	2011 to 2014	2015 to 2018
Minimum TSV diameter (*D*)	4 to 8 μm	2 to 4 μm
Minimum TSV pitch (*P*)	6 to 16 μm	4 to 8 μm
Minimum TSV length (*L*)	20 to 50 μm	20 to 50 μm
Maximum TSV aspect ratio (*AR*)	5:1–10:1	10:1–20:1

Two scenarios for scaling TSVs are proposed to efficiently analyze power noise in 3-D ICs. Assuming a constant TSV area penalty, the scaling trend of power noise is analyzed for different aspect ratios. Alternatively, assuming a constant aspect ratio, the scaling trend of power noise is evaluated for different TSV area penalties. Thus, both the effects of the TSV aspect ratio and TSV area penalty on 3-D power supply noise are discussed in this paper.

3. Inductive coupling effects in TSV arrays

Models have been proposed to analyze a paired TSV, as shown in Fig. 1(a) [12,13]. In a paired TSV, only coupling between two adjacent TSVs is considered. These models have been validated by commercial electromagnetic solvers [12,13]. A practical structure of a P/G TSV, however, is a large array of tens to thousands of TSVs, as shown in Fig. 1(b). An example TSV-based 3-D processor-memory system exhibits a physical footprint of 100 mm^2 with a 25 μm pitch between P/G TSVs [9]. The total number of P/G TSVs in a single layer in this system is 160,000, structured within a 400×400 array. A paired TSVs model is therefore insufficient to accurately analyze a single TSV within a large array of TSVs.

The surrounding TSVs affect the electromagnetic field within TSV arrays, making coupling among TSVs an issue. There are two types of coupling effects, capacitive and inductive coupling [1,22,25]. Due to the computational complexity of inductance and the long range phenomenon of inductive coupling, a computationally efficient and accurate analysis of inductive coupling effects is necessary.

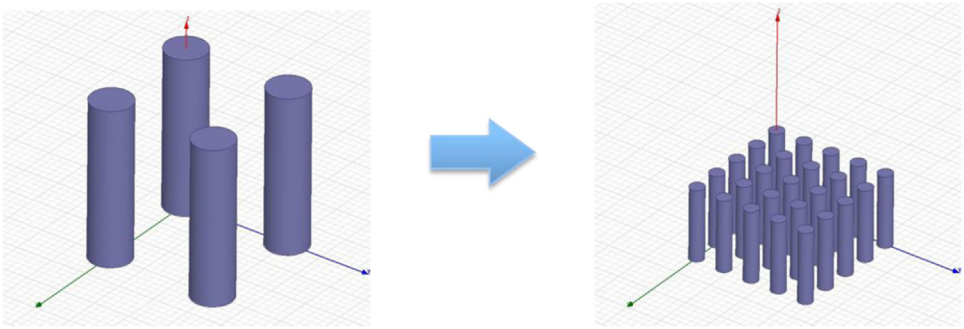


Fig. 2. Scaling of TSV, yielding higher TSV density with decreasing pitch, length, and diameter.

Table 2
Proposed TSV geometric parameters with physical effects.

	Modified parameters		New parameter
Expressions	L/D	P/L	P/r
Property	TSV aspect ratio	Determined by P/r and L/D	TSV area penalty
Effect	L_{self}	L_{mutual}	Current distribution

3.1. Long range phenomenon

The electrical parameters characterizing a TSV can be affected by the variation of an electromagnetic field. These parameters include the coupling capacitance C_C between adjacent TSVs and the equivalent self L_{self} and mutual inductance L_m of a TSV. The resistance of a TSV is determined by the material, geometric, and signal frequency of the reference TSV [10]. Capacitive coupling between TSVs is a short range effect due to the attenuative properties of an electric field. The coupling capacitance therefore does not significantly change between a paired TSV model and an array-based TSV macromodel. Alternatively, inductive effects of a TSV occur over long distances since a magnetic field is a long range phenomenon [26]. In this way, the surrounding TSVs in an array-based TSV macromodel have a significant effect on the inductance of a reference TSV.

The effect of the surrounding TSVs on a reference TSV in terms of the capacitance and inductance is shown in Fig. 3, which illustrates the long range property of inductive coupling. The capacitive effects of the surrounding TSVs on a reference TSV can therefore be ignored. Long range inductive effects are however considered, as described in the following subsections.

3.2. Distribution type of P/G TSVs

The P/G TSV distribution topology is the arrangement and relative position of different P/G TSVs. Three typical distribution topologies are discussed in this paper, grouped, lined, and uniform [24] (see Fig. 4). As shown in Fig. 4, the top view of three typical topologies for distributing P/G TSVs is considered, a grouped, lined, and uniform distribution. The grouped distribution is composed of a group of power and ground TSVs on each side of a unit area (see Fig. 4a). The lined distribution consists of lines of power TSVs interdigitated with lines of ground TSVs over the entire surface (see Fig. 4b). Alternatively, the uniform distribution consists of power and ground TSVs regularly spread over the entire surface (see Fig. 4c).

In the analysis of a P/G array-based TSV macromodel, another phenomenon, called proximity effects, should be considered, particularly when the operating frequency is sufficiently high [14,23]. The proximity effect describes a phenomenon where the direction of the current within two parallel interconnects affects the current distribution within these two adjacent conductors. This current redistribution phenomenon is due to the effects of the alternating magnetic field caused by a change in direction of the current flow. The proximity effect affects the analysis of an array-based TSV macromodel since the direction of the current in power and ground TSVs is assumed to flow in opposite directions. Due to the proximity effect and the long range phenomenon of inductive coupling, different distribution topologies of P/G TSVs can affect differently the characteristics of a 3-D power network. Hence, a detailed analysis and assessment of different TSV distribution topologies are necessary.

In the analysis of these three distribution topologies, a similar TSV radius, length, and separation between adjacent TSVs are assumed for each of the topologies. The only difference is the arrangement of the power and ground TSVs. Under this assumption, a negligible difference in resistance or capacitance exists among these three distribution topologies. Alternatively, the inductive effect varies with different distribution topologies. These P/G TSV distribution models have been evaluated by the Ansys Q3D Extractor [15], a quasi-static EM solver, to compare the equivalent inductance of each topology.

The equivalent inductance of the three TSVs distribution topologies with different array sizes is shown in Fig. 5. Each shade in the histogram refers to a specific TSV distribution topology. As the size of the TSV array increases, the equivalent inductance of the grouped TSV topology becomes larger than the inductance of the other distribution topologies. The equivalent inductance of the lined distribution topology is lower than the inductance of a uniform distribution for a 3×3 array and 7×7 array. The inductance, however, fluctuates significantly with array size in the lined distribution topology. The uniform distribution exhibits a relatively small and stable equivalent inductance.

The difference between the equivalent inductance of the different TSV distribution topologies can be described by the inductive current loops. A power and ground TSV constitutes a current loop, where the partial inductance of the power TSV decreases due to the mutual effect of the ground TSV. The equivalent inductance of a P/G TSV decreases if the P/G TSV is surrounded by TSVs with current passing in opposite directions (generating a negative mutual inductance, as shown in Fig. 7). Alternatively, the equivalent inductance of a P/G TSV increases if the P/G TSV is surrounded by TSVs with current passing in the same direction (generating a positive mutual inductance). In practical TSV distribution topologies, as illustrated in Fig. 4, both effects exist. The contribution of these two effects to the equivalent inductance of the reference TSV depends strongly on the topology of the TSV distribution and the size of the TSV array. The equivalent inductance therefore varies with different TSV topologies and array sizes.

As important component of on-chip power noise, simultaneous switching noise [16], become less significant with decreasing equivalent inductance [16]. As compared to the grouped and lined TSV distributions, the uniform distribution exhibits a low and relatively constant equivalent inductance. The uniform TSV

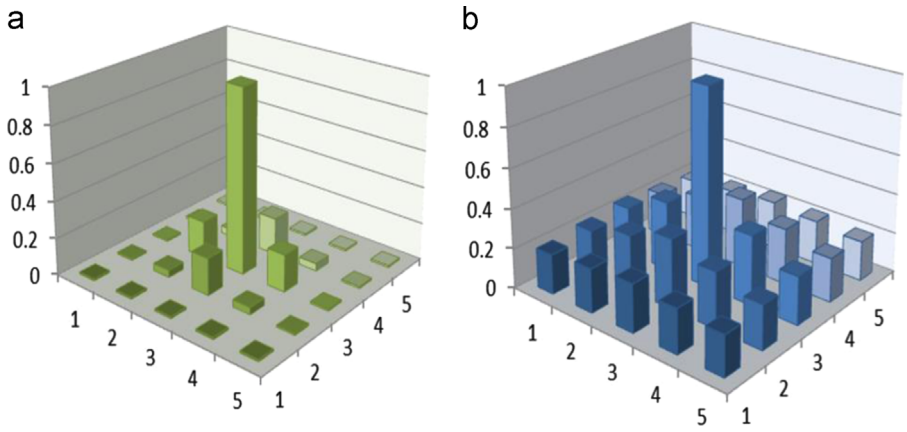


Fig. 3. 5×5 array-based TSV macromodel, (a) capacitive effect, and (b) inductive effect of surrounding TSVs normalized, respectively, to the equivalent capacitance and inductance of a reference TSV.

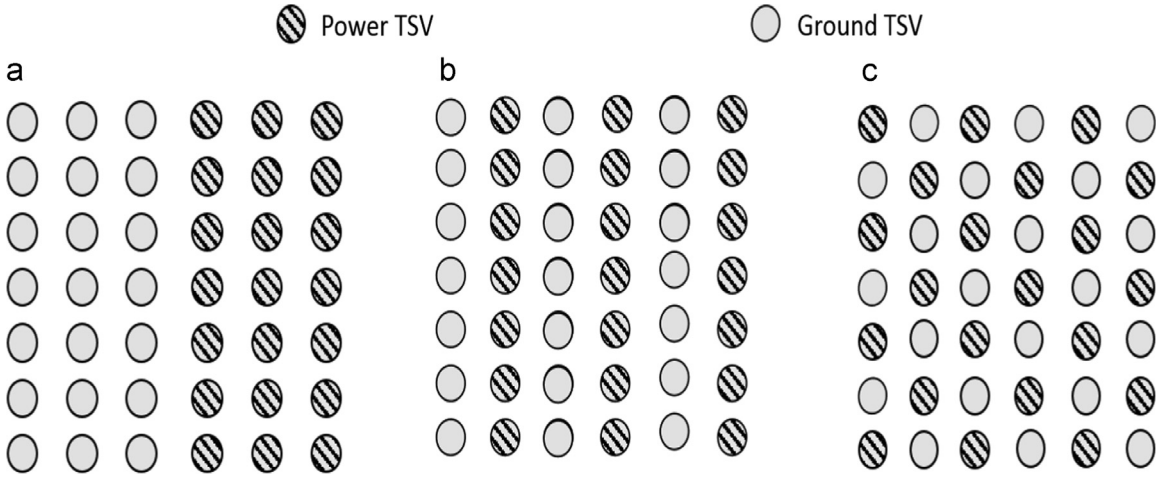


Fig. 4. Three typical power/ground TSV distribution topologies, (a) grouped TSV distribution, (b) lined TSV distribution, and (c) uniform TSV distribution.

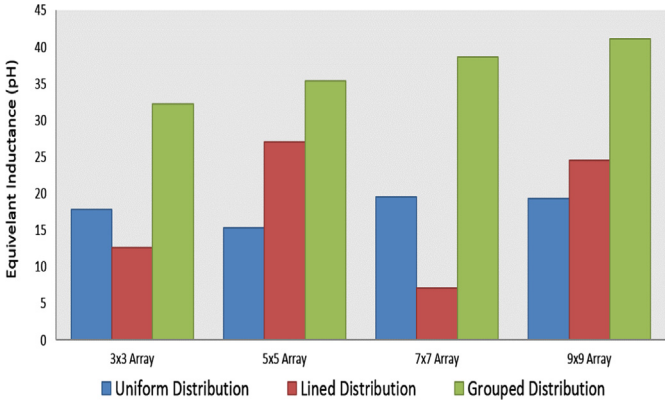


Fig. 5. Equivalent inductance of three TSV distribution topologies for different array sizes.

distribution is therefore a better topology for 3-D power distribution networks from the perspective of lower on-chip power supply noise.

4. Inductance model of large array of TSVs

From the discussion of the three TSV topologies, a uniform TSV distribution is shown to be the most promising topology. In the following analysis, all of the TSV topologies are therefore assumed to be a uniform TSV distribution topology. The equivalent inductance of TSVs in a 3×3, 5×5, 7×7, and 9×9 array has been evaluated with Ansys Q3D. A practical P/G TSV array can, however, be as large as 400×400 TSVs [18]. Although the equivalent inductance extracted from a quasi-static EM solver is highly precise, the time and memory requirement of Ansys Q3D is intractable with large arrays. A compact model to determine the TSV inductance in a fast and precise manner is therefore highly desirable.

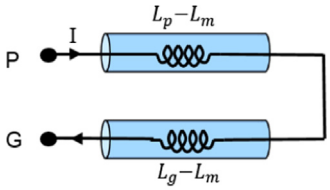
A current loop model is shown in Fig. 6, where a power TSV represents the signal path, and a ground TSV represents the corresponding return path. L_{eq} refers to the equivalent inductance of the power TSV. L_p and L_m are, respectively, the partial inductance of the power TSV and the mutual inductance. The equivalent inductance of a power TSV is $L_{eq} = L_p - L_m$. Note that the relationship between L_p and L_m depends upon the current direction of these two parallel interconnect.

As shown in Fig. 7, the partial inductance is applied to a 3×3 array-based P/G TSV model. L_{eq} is $L_5 + L_{15} - L_{25} + L_{35} - L_{45} - L_{65} + L_{75} - L_{85} + L_{95}$, where L_{eq} represents the equivalent inductance of a reference TSV, L_5 in Fig. 7. The others terms represent the mutual inductance between the reference TSV and the surrounding TSVs. For example, L_{15} represents the mutual inductance between TSV L_5 and TSV L_1.

A more general uniform TSV distribution array is shown in Fig. 8. The TSV in the center of the array is assumed to be the reference TSV. The 5×5 TSV array shown in Fig. 8 is composed of four groups, each group surrounded by a dashed circle with six TSVs. This 5×5 TSV array is a centrosymmetric model with the center of symmetry at the

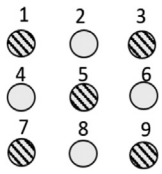
reference TSV. All of the groups therefore exhibit the same inductive effect on the reference TSV. Thus, only one group of TSVs is considered here to analyze the effect of the inductance on the surrounding TSVs. For an $m \times n$ case, the equivalent inductance is

$$L_{eq} = L_{self+} + 4(-1)^{m+n}\beta\frac{\mu_0}{2\pi}\sum_{i=1}^{m}\sum_{j=0}^{n}\left[\ln\left(\frac{\frac{L}{P}+\sqrt{\left(\frac{L}{P}\right)^2+m^2+n^2}}{\sqrt{m^2+n^2}}\right)\left(\frac{L}{P}\right) + \sqrt{m^2+n^2} - \sqrt{\left(\frac{L}{P}\right)^2+m^2+n^2}\right]P, \quad (6)$$



$$L_{eq} = L_p - L_m$$

Fig. 6. Current loop model represented by a partial inductance.



$$L_{eq} = L_5 + L_{15} - L_{25} + L_{35} - L_{45} - L_{46} + L_{75} - L_{85} + L_{59}$$

Fig. 7. Partial inductance in a 3×3 array-based TSV model.

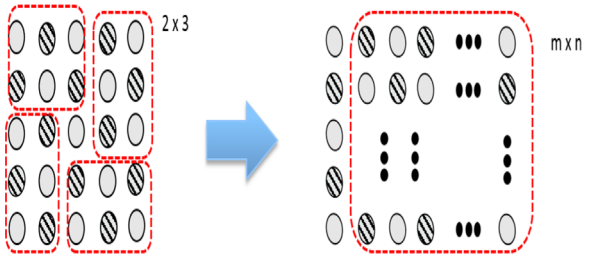


Fig. 8. Equivalent inductance model from a 5×5 TSV array to a general uniform TSV distribution.

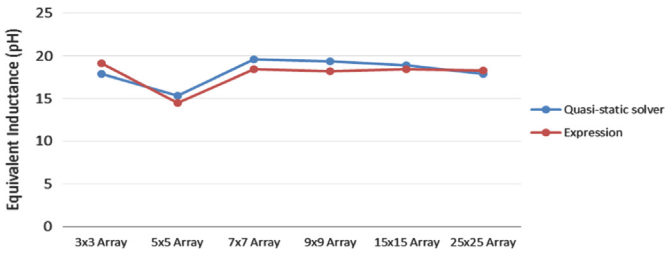


Fig. 9. Accuracy of closed-form expression as compared to EM solver.

where the individual impedances are described in closed-form expressions [10]. As shown in Fig. 9, the expression (as compared to the EM solver) exhibits a maximum error of less than 7% for 3×3, 5×5, 7×7, and 9×9 TSV arrays.

The primary advantage of the proposed expression for determining the equivalent inductance is computational complexity, as listed in Table 3. The run time to evaluate a 9×9 TSV array for Ansys Q3D is up to 3 min, as compared with less than one second using (1). This time difference increases with larger TSV array size. Array sizes of 400×400 are intractable with Ansys Q3D, while for the closed-form expression, an accurate solution is produced in 105 s. Hence, a much faster computational speed is achieved with tolerable (less than 7%) error.

5. Model of cell-based 3-D power distribution network

Modern power distribution networks are hierarchical and can contain billions of nodes [1]. Simulating such a large network is computationally expensive [7,8]. In addition, the magnitude and switching frequency of the current passing through the power network are affected by the operating states (e.g., busy or idle) and load functions (e.g., ALU, TLB, and memory). Hence, the temporal and spatial uncertainty of the current makes simulating an IC level power network difficult both from accuracy and computational efficiency perspectives.

A cell-based power distribution network model is introduced in this paper as a simple and effective way to analyze power supply noise in 3-D ICs. As shown in Fig. 10(a), power distribution cells represent the power network within a circular region, around the P/G TSVs within each layer. A pair of P/G TSVs and the surrounding power distribution cells constitute an analytic unit to analyze power noise in 3-D ICs. This analytic unit is a cell-based 3-D power network model within a 3-D power distribution network.

The cell-based 3-D power network is divided into two sub-networks, a power TSV sub-network and a ground TSV sub-network. In the power TSV sub-network, current is drawn from the package to power the TSVs through controlled collapse chip connection (C4) balls. The current is distributed to the power distribution cells in different layers within the power TSVs. The current is distributed to all of the active devices by a power distribution cell within a 2-D power network. The power noise generated by the P/G TSVs and each 2-D power network is considered here. Due to the symmetric characteristics of the power and ground TSV sub-networks in the proposed model, the power noise generated in the ground TSV sub-network is the same as the noise generated in the power TSV sub-network, as illustrated in Fig. 10(a). Only the power noise emanating from the power TSV sub-network is therefore considered in the following discussion.

The top view of a single power distribution cell [6] is shown in Fig. 10(b). The shaded area within the dashed circular curve is the effective area of the power distribution cell. The smaller shaded circular area is the cross-section of the power TSV. r_{cell} is the radius

Table 3
Comparison of computational time between closed-form expression and EM solver.

CPU time	3×3 array	5×5 array	7×7 array	9×9 array	15×15 array	25×25 array	400×400 array
Quasi-static solver	5 s	29 s	1 min 29 s	3 min 29 s	23 min 44 s	127 min 46 s	–
Algorithm	0.019 s	0.024 s	0.030 s	0.037 s	0.063 s	0.135 s	105 s
Improvement	260	1200	3000	5600	23,000	57,000	–

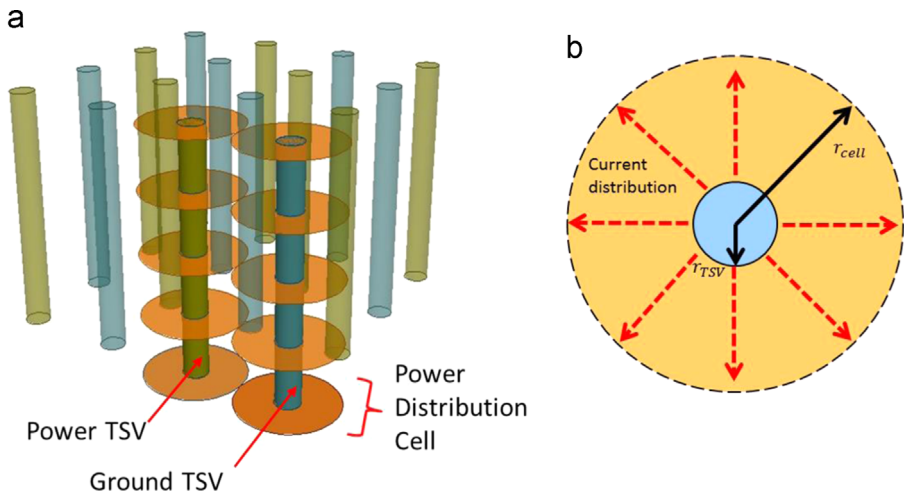


Fig. 10. Model of cell-based 3-D power distribution network, (a) panoramic view of a single pair P/G TSVs, and (b) top view of power distribution cell.

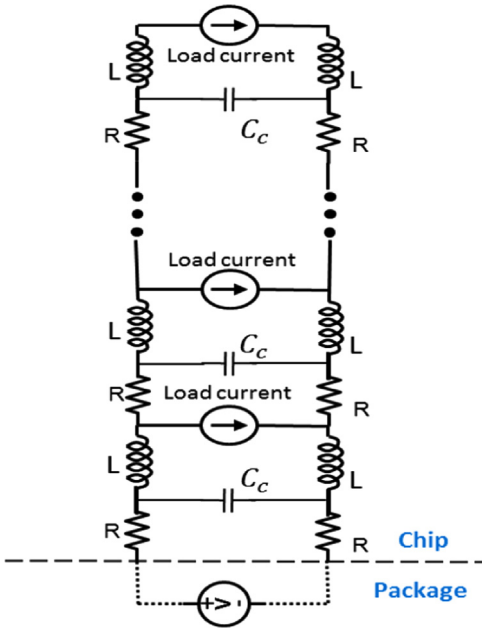


Fig. 11. Electrical model of cell-based power supply noise within a 3-D system.

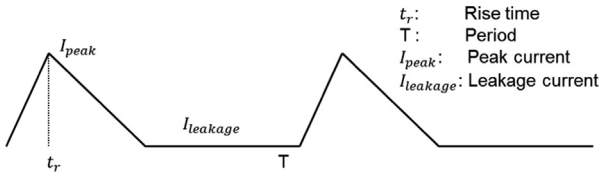


Fig. 12. Triangular waveform of current source.

of the power distribution cell and r_{TSV} is the radius of the power TSV. The dashed arrows depict the direction of the current flow within the cell area.

In the cell-based power network model, several assumptions have been made to simplify the analysis of power noise scaling trends in 3-D systems. The current passing through different power TSVs is the same. The power cells within and among different cell-based power networks are the same area. In addition, the average current per unit area is assumed to be constant [3], implying that the total average current in each individual cell is constant. Based on these assumptions, an individual power TSV only distributes current to the power distribution cells around a single P/G TSV pair. In this way, the interactions and mutual effect among cells around different TSV pairs cancel, simplifying the analysis of power supply noise in large scale systems.

The circuit model of a cell-based 3-D power distribution network is shown in Fig. 11. Note that the circuit model is valid for 3-D systems utilizing the via-last technique [7]. As shown in Fig. 11, the dashed line at the bottom of the figure refers to the boundary between the package and IC. The voltage source V is the voltage between the power TSV and ground TSV. R and L are, respectively, the equivalent resistance and inductance of the P/G TSVs within each circuit layer. C_C is the coupling capacitance between two adjacent TSVs. The switching loads within each individual power distribution cell are typically represented by a triangular waveform characterizing the current source, exhibiting an average current consumption within this power cell [17]. The triangular waveform is shown in Fig. 12.

6. Simulation results and analysis

Three scaling scenarios are discussed in this section. These scenarios are, respectively, constant TSV area penalty, constant TSV aspect ratio, and constant TSV technology scaling. Cadence Spectre is used to simulate the scenarios [19]. The circuit model applied in the different scenarios is the model proposed in Section 5 (see Fig. 11). Three parameters in this model change with TSV technology scaling: the equivalent inductance of the TSV L, equivalent resistance of the TSV R, and coupling capacitance between a paired TSV C_C. Based on closed-form expressions [10], the equivalent resistance and coupling capacitance of a TSV are determined. Alternatively, the equivalent inductance of an array of TSVs is determined from the inductance expression proposed in Section 4. Since the value of these parameters changes significantly with different scenarios, specific data are shown for each scenario in the following subsections. Other parameters are listed in Table 4 [7], such as the technology, operating frequency, and physical area.

6.1. Constant TSV area penalty scaling scenario

An important parameter in fabricating TSVs is the TSV aspect ratio, which tends to increase with TSV technology scaling [6]. TSV scaling yields a higher density of TSVs, and a smaller TSV diameter [20]. Several approaches to produce a high aspect ratio copper filling process for TSVs have been developed [20,21]. In addition,

Table 4
Parameters for constant TSV area penalty/AR scenario [7].

Parameter	Constant TSV area penalty
CMOS technology	32 nm
Operating frequency	2.5 GHz
Die area	100 mm^2
Total layers	10
TSV technology	Via-last
Power supply voltage	1 V

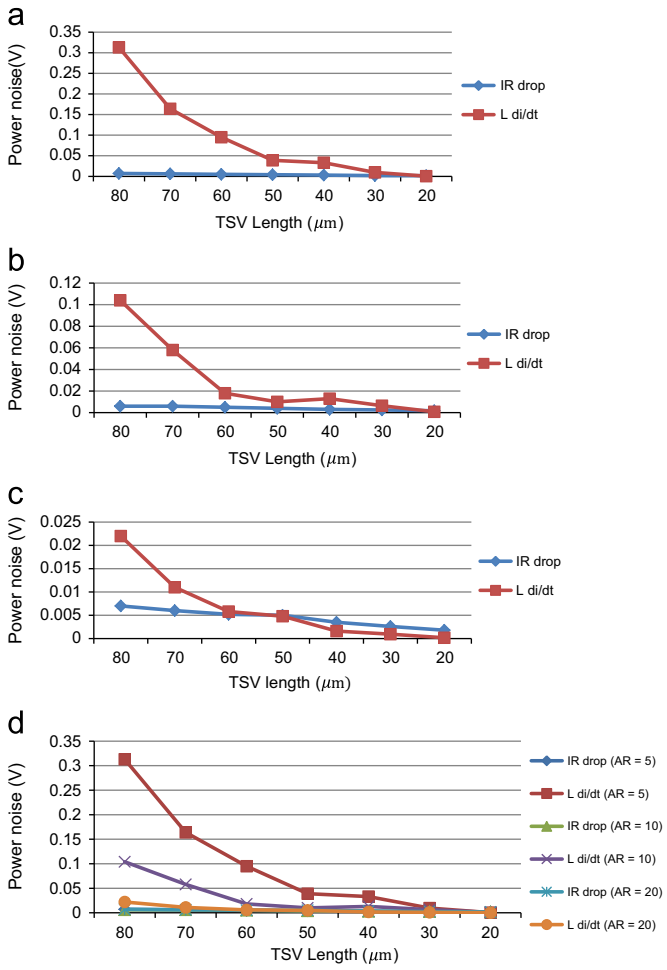


Fig. 13. Resistive and inductive power noise in 3-D systems with different TSV scaling scenarios, (a) $AP=1\%$, $AR=5{:}1$, (b) $AP=1\%$, $AR=10{:}1$, (c) $AP=1\%$, $AR=20{:}1$, and (d) comparison of these three scenarios.

some advantages of high aspect ratio TSVs are introduced, such as integrating higher density TSVs and producing smaller area TSVs [20,21]. A power noise analysis of high aspect ratio TSV-based 3-D systems is therefore desirable.

Different aspect ratios (AR) are considered based on the trend of high aspect ratio TSVs [6,20]. $AR>8$ is considered a high aspect ratio [20]. Test cases of $AR=10$ and $AR=20$ are therefore chosen to investigate power noise in 3-D systems with higher AR. The test case of $AR=5$ is also considered to compare the effects on power noise of high aspect ratio TSVs and low aspect ratio TSVs.

TSV length has evolved from 80 μm to 20 μm based on the development of different TSV fabrication technologies [6]. Since a TSV consumes significant physical area, it is assumed that 1% of the total area is required for the TSVs in a high performance 3-D system [7]. Several TSV area penalties are considered in the next subsection to evaluate this effect on power noise in 3-D systems.

A comparison of *IR* drop and *L di/dt* noise is shown for each TSV scaling scenario in Fig. 13. *IR* drops are much smaller than *L di/dt* noise due to the excellent conductivity of copper as the TSV filling material. The relatively large inductive power noise is also due to the high frequency current passing through the P/G TSVs within a 3-D system.

As shown in Fig. 13(a)–(c), both *IR* drop and *L di/dt* noise decrease with TSV scaling, where the inductive noise is larger than the resistive noise when the TSV length is longer than 50 μm (see Fig. 13(c)). Scaling trends of resistive noise for different scenarios are similar. The scaling trends of inductive noise, however, change significantly. As the filling material of the TSVs in the via-last technology, copper has lower resistivity, leading to smaller *IR* drops. In addition, due to the high operating frequency (see Table 4), the high rate of change of the current passing through the TSVs generates greater *L di/dt* noise, increasing *L di/dt* noise as compared to *IR* drop noise. This difference between resistive and inductive noise decreases with TSV scaling, as shown in Fig. 13. In each case, the TSV aspect ratio remains the same, suggesting that the TSV radius decreases at the same rate S as the TSV length is scaled. Based on the power cell model (see Section 5), the current passing through the TSVs decreases by S^2. This behavior explains why *L di/dt* noise decreases faster than *IR* drop noise, and becomes less than the *IR* drops when the TSV length is shorter than 50 μm in the $AR=20{:}1$ case (see Fig. 13(c)). Constant TSV aspect ratio scaling is therefore an effective method to lower inductive noise, particularly when the TSV length is less than 50 μm.

A comparison of resistive and inductive noise for the three different scenarios is provided in Fig. 13(d). Increasing the TSV aspect ratio is an efficient method to reduce power noise in 3-D systems. Under the same TSV length conditions, a higher TSV aspect ratio offers a much smaller power cell area, passing much less current through the TSVs. The inductive noise therefore decreases significantly with increasing TSV aspect ratio. Moreover, the technology for increasing the TSV aspect ratio is more effective than the technology for scaling the TSV length. For example, the inductive power noise of TSVs shorter than 80 μm for the $AR=5$ and $AR=20$ cases are, respectively, 0.31 V and 0.029 V. The TSV length in the $AR=5$ case should be scaled to 30 μm to achieve the same noise in the $AR=5$ case when the TSV length is 80 μm. The length of a via-last TSV is limited by both the wafer thinning process and the thickness of the metal layer [9]. When the TSV length becomes the bottleneck for decreasing power noise, a higher aspect ratio TSV should be adopted to lower power noise in 3-D ICs. Tradeoffs should therefore be considered between the TSV length and the TSV aspect ratio for different TSV and metal interconnect technologies.

6.2. Constant TSV aspect ratio scaling scenario

TSVs require active device and metal layer area, producing larger die sizes. For example, a 5 μm × 5 μm square shaped TSV occupies the same area as 10 typical logical gates in a 45 nm technology [21]. In this way, global interconnect lengths increase, worsening the performance of 3-D systems. A nine layer 3-D processor-memory stack requires at least 3% more area to maintain power noise below 10% [7]. A power noise analysis of 3-D systems assuming different TSV area penalties is therefore desirable.

A higher TSV aspect ratio enhances the performance of 3-D systems, as mentioned above. The TSV aspect ratio for the constant TSV aspect ratio scenario is assumed to be 10:1. Three specific cases, TSV area

penalty=1%, TSV area penalty=0.5%, and TSV area penalty=0.25%, are chosen to evaluate a small area TSV while providing high speed.

The waveform of power noise in the test case of TSV area penalty=0.25% is shown in Fig. 14. Scaling trends of resistive and inductive power supply noise under the constant TSV aspect ratio scaling scenario are shown in Fig. 15. The large difference in scaling trends between resistive and inductive noise is noted. A comparison of *IR* drop and *L di/dt* noise among the three different scenarios is illustrated in Fig. 15(d). Increasing the TSV area penalty is an efficient method to reduce power noise in 3-D systems. For example, the inductive power noise of a 70 μm long TSV with a TSV area penalty=0.25% and TSV area penalty=1% are, respectively, 0.239 V (larger than the 10% V_{dd} noise requirement) and 0.059 V (within the 10% V_{dd} noise requirement). This result can be explained by the increased volume for current to pass vertically due to the larger TSV cross-section. For the same TSV length, the cross-sectional area of each TSV is the same in the constant TSV aspect ratio scaling scenario. In this way, a larger TSV area penalty supports a greater number of P/G TSVs. As compared with a 1% TSV area penalty, the 0.25% TSV area penalty integrates three times more TSVs within a 3-D system. Based on the assumption that the die size and current density of a power cell are maintained constant for different scenarios, a greater number of TSVs yields a smaller power cell, passing less current into each P/G TSV. In this way, inductive noise drops significantly with increasing TSV area penalty.

To maintain high performance and high efficiency TSV integration in 3-D systems, the TSV area penalty however cannot be large. Tradeoffs among the TSV area penalty, TSV technology, and power supply noise in 3-D ICs should therefore be carefully considered during the design of a 3-D power distribution network. When the TSV technology becomes a primary bottleneck in high performance 3-D ICs, increasing the TSV area penalty will produce less power noise. For example, the inductive power noise for 40 μm long TSVs with a TSV area penalty=0.25% and *AR*=10:1 is 0.083 V. The same power noise can be achieved by using P/G TSVs with an 80 μm length TSV with area penalty=1% and *AR*=10:1, or by using TSVs with 60 μm length, TSV area penalty=1%, and *AR*=5:1.

6.3. Constant TSV technology scaling scenario

The effects of two different TSV scaling scenarios on power supply noise in 3-D ICs have been discussed in previous subsections. CMOS scaling trends and TSV fabrication techniques can also affect power noise in 3-D systems. A power noise analysis that considers CMOS technology scaling and TSV fabrication techniques is therefore important. Typical TSV parameters with different fabrication techniques are listed in Table 5. Trends in power supply noise with

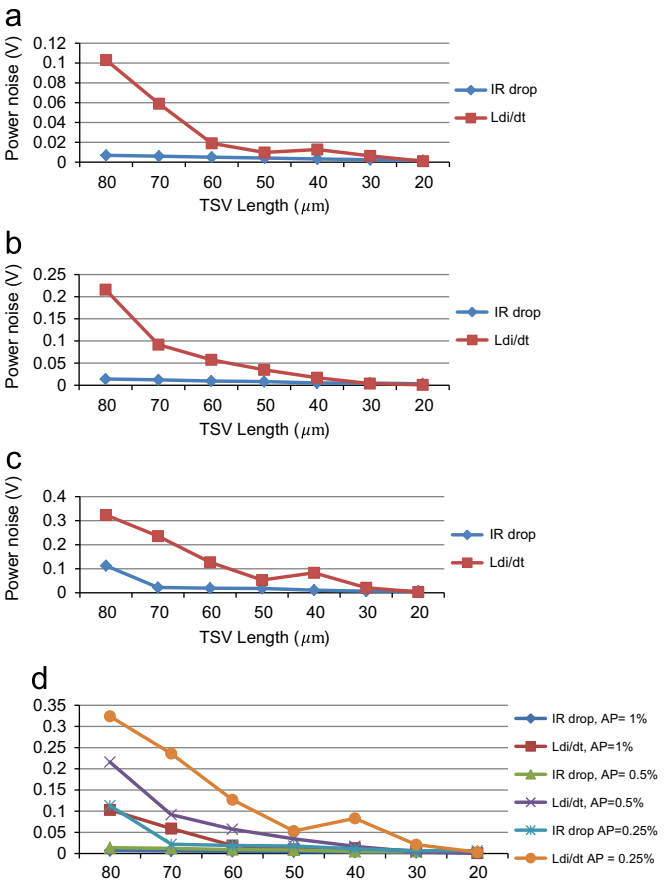


Fig. 15. Resistive and inductive power noise in 3-D systems with different TSV scaling scenarios, (a) TSV area penalty=1%, *AR*=10:1, (b) TSV area penalty=0.5%, *AR*=10:1, (c) TSV area penalty=0.25%, *AR*=10:1, and (d) comparison of these three scenarios.

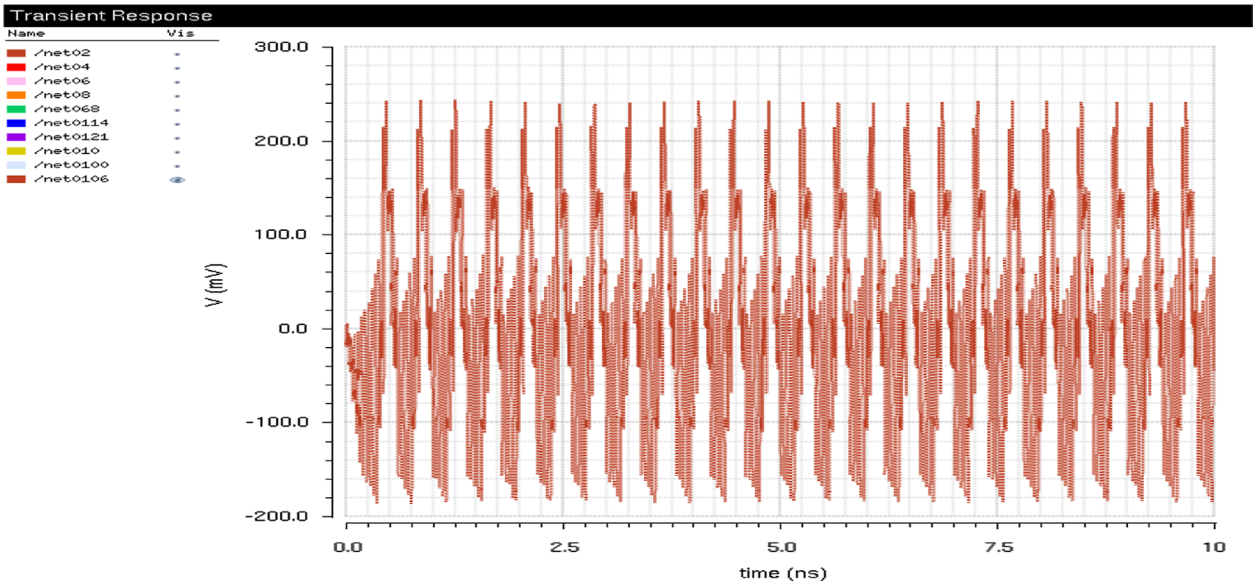


Fig. 14. Waveform of power noise in 3-D systems where TSV area penalty=0.25%, *AR*=10:1, and TSV length=70 μm.

Table 5
Typical parameters for different TSV fabrication technologies [7].

Parameter	Via-first	Via-middle	Via-last
Diameter (μm)	4	4	10
Pitch (μm)	8	8	20
Length (μm)	10	60	60
TSV resistance (Ω)	5.7	0.9	0.02
TSV inductance (pH)	4.2	49.8	34.9
TSV coupling capacitance(fF)	1.2	6.7	6

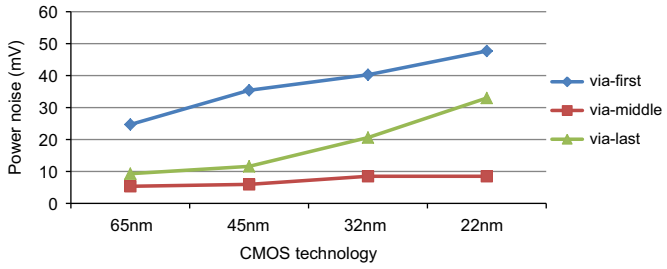


Fig. 16. Power noise as a function of CMOS technology scaling for different TSV fabrication technologies.

CMOS technology scaling, evolving from 65 nm to 22 nm under different TSV fabrication methods, are shown in Fig. 16.

As shown in Fig. 16, power supply noise in TSV-based 3-D ICs increases with CMOS technology scaling. This trend occurs since the current density within each layer and the operating frequency of 3-D ICs tend to increase with CMOS technology scaling. Under the same TSV technology and distribution conditions, larger currents pass through each of the P/G TSVs, generating higher levels of on-chip power supply noise in 3-D ICs.

For these three TSV fabrication techniques, the via-first TSV technology exhibits the highest power noise. This trait can be explained by the higher resistance of a via-first TSV whose filling material is polysilicon (7.2 μΩ m). Alternatively, the via-middle TSV technology seems to be the most advantageous, producing the lowest power noise. The filling material of the via-middle TSV technology is tungsten, which has a similar conductivity to copper [7] (as compared with polysilicon). In addition, the via-middle technology, the same as the via-first technology, has a higher TSV aspect ratio and a fine metal pitch. Both of these characteristics of the via-middle TSV technology produce the lowest power noise for these three cases. As the most common TSV fabrication technology [7], the via-last TSV technology exhibits middle levels of power noise between the via-first and the via-middle TSV technologies. The good conductivity provided by copper significantly decreases the resistive noise in the via-last TSV technology; however, the larger size of the via-last TSV technology worsens the inductive noise.

From a power noise perspective, the via-middle TSV technology is the most promising technology for TSV-based 3-D ICs. However, fabricating via-middle TSVs is the most challenging of the three TSV fabrication technologies from both a time and cost perspective [7]. Although the via-first TSV technology produces the highest power noise, it has several advantages such as no metal routing blockages, higher density, and an easier fabrication process than the via-middle TSV technology. As the easiest fabrication technology, the via-last TSV technology has been widely used. The primary disadvantage of the via-last TSV technology is the large size of the TSVs, generating large inductive noise and requiring significant metal and area resources. Tradeoffs should therefore be considered based on these characteristics and systems applications.

7. Conclusions

Power supply noise in TSV-based 3-D integrated circuits considering CMOS and TSV technology scaling is discussed in this paper. Two scenarios of TSV technology scaling are proposed to efficiently analyze power noise in 3-D systems. Inductive coupling in large TSV arrays is discussed. A comparison of the equivalent inductance among three typical distribution topologies of P/G TSVs shows that a uniform distribution is a better topology for 3-D power distribution networks from the perspective of lower on-chip power supply noise. An accurate and computationally efficient closed-form expression for calculating the equivalent inductance of a TSV is also proposed. A TSV and inductance aware cell-based 3-D power network model is proposed, and a discussion of power supply noise in 3-D systems for different scaling scenarios is presented. Tradeoffs among different TSV geometric parameters, fabrication technologies, and resistive and inductive power supply noise are discussed. The via-middle TSV technology is demonstrated to be a promising TSV technology, producing the lowest power noise.

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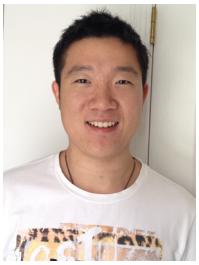

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