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Inductorless dynamic logic based on 2ϕ-Josephson junctions☆

Ana Mitrovic *, Eby G. Friedman [1]

Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY 14627, USA

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ABSTRACT

Despite offering significant performance and energy efficiency advantages over CMOS, superconductive digital circuits face several challenges including scaling limitations. Traditional single flux quantum (SFQ) circuits require synchronous clock signals, leading to complex clock distribution networks. The integration density of SFQ circuits is also hindered by the need for large storage inductors. To overcome these challenges, an inductorless dynamic logic based on ferromagnetic bistable 2ϕ-Josephson junctions (JJ) is proposed. This logic family offers a scalable solution for asynchronous superconductive logic circuits. The behavior of 2ϕ-Josephson junctions is reviewed, and all-JJ dynamic circuits facilitating clockless operation are introduced. Inductorless dynamic AND and OR gates are evaluated in a half adder. The characteristics, margins, and effects of the parasitic inductances on circuit operation are discussed. As compared to RSFQ gates in the same technology (1 kA/cm^2), these logic gates exhibit 59% less delay (9 ps). 2ϕ-JJs require less energy to switch between equilibrium states. As a result, a decrease of 65% in bias current as compared to standard dynamic SFQ circuits is achieved. The reduction in bias current in half flux quantum operation requires 6.7X less energy per transition. Utilizing standard Josephson junctions rather than inductors saves 42 μm^2 and 53 μm^2 of loop inductance area within, respectively, a dynamic AND gate and dynamic OR gate for the 10 kA/cm^2 MIT LL SFQ5ee technology.

1. Introduction

The distribution of clock signals in single flux quantum (SFQ) VLSI circuits poses a significant challenge due to the distinctive feature of clocked logic gates [1]. Data representation in SFQ circuits relies on the presence or absence of an SFQ pulse within a clock period. Clock signals are common to most RSFQ logic gates and are used to read or reset the internal state of a gate after each clock cycle.

The significant complexity of clock distribution networks in SFQ circuits results in a large area and power overhead. SFQ circuits can operate at high clock frequencies, typically tens to hundreds of gigahertz [2,3]. Narrow timing tolerances are therefore another important issue in high speed SFQ circuits.

To address clocking issues in SFQ systems, several synchronization approaches are considered. These approaches include fully asynchronous [4], globally asynchronous locally synchronous (GALS) [5], and dual rail [6]. Clockless SFQ logic gates are crucial to enable efficient asynchronous and combinational SFQ logic [1,7,8].

Another critical challenge in SFQ circuits stems from low integration densities as compared to traditional CMOS technology. Large inductors are an essential component of standard SFQ storage loops and require significant area. Scaling the spacing and width of these inductors is further limited due to mutual coupling [9]. Additionally, these inductors exacerbate flux trapping and coupling noise [10].

Several approaches have been explored to scale SFQ circuits. One approach uses a kinetic inductance that, while promising for existing SFQ technologies, presents fabrication challenges at small scale [9]. Another solution uses a stack of JJs as a substitute for a traditional inductor [11,12]. The introduction of π-Josephson junctions, where a ferromagnetic interlayer induces a π-phase shift in the current–phase relationship (CPR), offers a unique solution for replacing the inductors [13]. The inherent phase shift of a π-JJ, however, can lead to persistent currents [9], degrading the behavior of neighboring cells.

One alternative solution is based on a novel logic family composed of ferromagnetic bistable 2ϕ-Josephson junctions (2ϕ-JJ) [9,14–16]. 2ϕ-JJs exhibit a double well energy–phase relationship and a second harmonic in the CPR, producing half flux quantum (HFQ) pulses when switching [17,18]. This technology enables SFQ circuits composed of

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* Corresponding author.
E-mail addresses: ana.mitrovic@rochester.edu (A. Mitrovic), friedman@ece.rochester.edu (E.G. Friedman).
[1] Fellow, IEEE.

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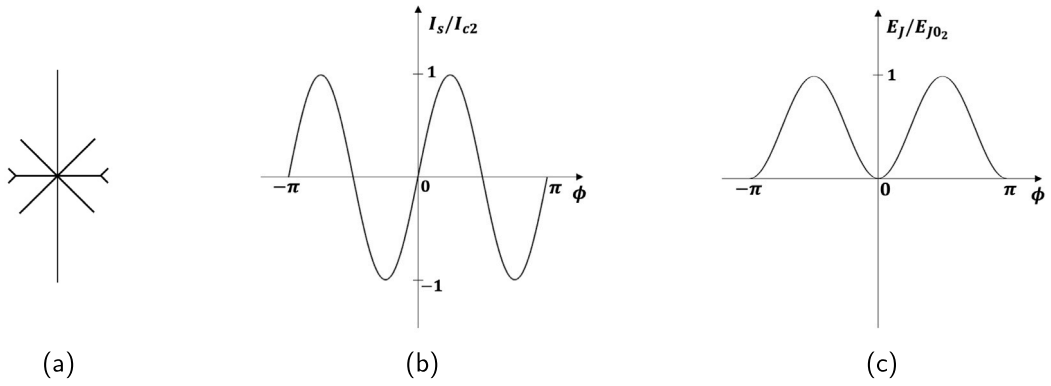

Fig. 1. 2ϕ-Josephson junctions, (a) symbol, (b) current–phase relationship, and (c) energy–phase relationship.

only standard and bistable JJs, avoiding large inductors. The fabrication of 2ϕ-junctions remains an active research challenge, as no standardized process currently supports this type of junction. Evaluation of this approach therefore relies on simulations incorporating 2ϕ-JJ models and standard SFQ process parameters [16].

In this paper, a novel inductorless dynamic logic is proposed based on the dynamic SFQ (DSFQ) logic family [1,19] and bistable Josephson junctions. The behavior of 2ϕ-JJs is reviewed in Section 2. In Section 3, the DSFQ logic family is discussed, and an all-JJ dynamic storage loop is introduced. Inductorless dynamic logic gates, including an AND gate and an OR gate, are proposed in Section 4. Application of these gates within a half adder is described in Section 5. The paper is concluded in Section 6.

2. 2ϕ-Josephson junctions

Conventional Josephson junctions are composed of two superconductive electrodes separated by an oxide layer (*e.g.,* Nb/AlOx-Al/Nb JJs in the MIT LL SFQ5ee fabrication technology [20]). A generalized expression for the CPR of a JJ is [17]

$$I = \sum_{n\geq 1} I_{c_n} \sin(n\phi), \tag{1}$$

where ϕ is the phase difference, and I_c is the critical current of the junction. The CPR of a standard JJ, also referred to as 0-JJ, is characterized by a pure first harmonic. Tunnel junctions with ferromagnetic barriers can however exhibit a suppressed first harmonic and an observable second harmonic in the CPR [17]. The CPR of these bistable junctions is

$$I_s(\phi) = I_{c_1} \sin(\phi) + I_{c_2} \sin(2\phi). \tag{2}$$

In (2), I_{c_1} and I_{c_2} are, respectively, supercurrent amplitudes of the first harmonic and the second harmonic. These junctions are called 2ϕ-JJs. The symbol used for a 2ϕ-JJ is shown in Fig. 1(a). Junctions with a pure second harmonic have been experimentally demonstrated [17,18]. The π-periodic CPR of these junctions is shown in Fig. 1(b).

The energy–phase relationship (EPR) of a 2ϕ-JJ is

$$E_J(\phi) = E_{J0_2} \frac{I_{c_1}}{I_{c_2}} (1 - \cos(\phi)) + \frac{E_{J0_2}}{2} (1 - \cos(2\phi)), \tag{3}$$

where $E_{J0_2} = \Phi_0 I_{c_2}/2\pi$, and Φ_0 is the magnetic flux quantum ($\approx$ 2.07 mV ps). The energy minima in the EPR of a 2ϕ-JJ with a pure second harmonic are located at 0 and πn phase values, as depicted in Fig. 1(c).

Switching a 2ϕ-JJ occurs at a π phase difference, producing an HFQ voltage pulse. This pulse is half the area of an SFQ pulse ($\approx$1.03 mV ps). The energy required for a 2ϕ-JJ to switch is half the energy to switch a standard JJ, improving the power efficiency [14,15]. Utilizing the bistable behavior of these junctions, all-JJ circuits based on the transmission of HFQ pulses have been proposed [15,16]. A similar approach is presented in this paper, replacing the storage inductor with 0-JJs.

Existing experimentally verified 2ϕ-junctions utilize weak ferromagnets or ferromagnetic insulators as junction barriers. In junctions with a weak ferromagnetic barrier, an intrinsic, dominant second harmonic exists in the vicinity of the 0-π transition of the junction [18,21]. The typical range for the critical current density of the sin2ϕ term of these junctions is 0.4 to 1.0 kA/cm^2 [14,18,22]. A robust second harmonic has been predicted and experimentally confirmed in junctions with spin–triplet pairing [17,23–25]. The $I_c R_N$ product of these junctions decreases linearly with thickness between 1 mV and 0.1 mV.

3. All-JJ dynamic logic

Dynamic SFQ is an asynchronous SFQ logic family based on clockless operation [1,19,26,27]. These gates employ self-resetting storage loops, temporarily storing the state of a gate, which resets to the initial state after a period of time. This distinctive feature supports asynchronous operation, leading to a notable reduction in area and energy in the clock distribution network in large scale SFQ circuits. DSFQ gates are also combinational in nature.

A DSFQ storage loop is shown in Fig. 2(a). To enable dynamic operation and temporarily store a pulse, a large storage inductor L ($\approx$10 pH) is used within the DSFQ storage loop. These inductors are difficult to scale and occupy significant area.

In this paper, the issue of large storage inductors is addressed by utilizing 2ϕ-JJs, which transmit an HFQ pulse. Lower inductance is necessary to store an HFQ pulse, replacing the large storage inductors used in DSFQ circuits with 0-JJs [15]. This logic is named Dynamic Half Flux Quantum (DHFQ) logic. A DHFQ storage loop is shown in Fig. 2(b), containing an unshunted 2ϕ-junction J_D in series with a resistor R_D and an additional 2ϕ-JJ J_H shunted by resistor R_H.

The storage inductance is provided by the Josephson inductance of the 0-JJ J_L which operates in the nonswitching mode. This junction is shunted with R_L to reduce variations in the phase difference and improve the stability of the circuit parameters. When the current flowing through the junction is less than the critical current, J_L behaves as a nonlinear inductance [12]. The Josephson inductance of this junction is

$$L_{J_L}(\phi) = \frac{\Phi_0}{2\pi I_{c_L} cos\phi}. \tag{4}$$

Due to the nonswitching operation of this junction, the average phase difference is close to zero. To simplify the circuit design process, the inductance of the junction can be approximated as

$$L_{J_L}(0) = \frac{\Phi_0}{2\pi I_{c_L}}. \tag{5}$$

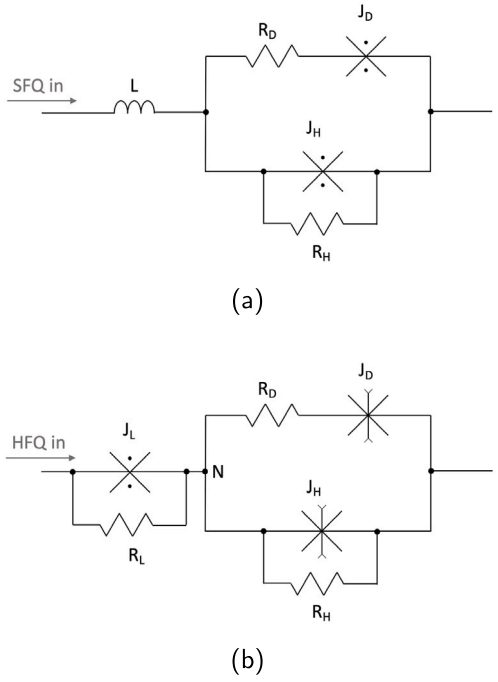

Fig. 2. Dynamic superconductive storage loops, (a) DSFQ storage loop introduced in [1], and (b) DHFQ storage loop.

The DHFQ storage loop operates as follows. Upon the arrival of an input HFQ pulse, voltage V_{LEAK} is produced at node N due to current flowing through resistor R_D. This voltage increases the phase of J_H. The current is redistributed between branches, switching the phase of J_H after a period of time, resetting the state of the storage loop. The hold time τ_H of the DHFQ logic gate depends upon the rate of the flux leakage, which is set by V_{LEAK}. The hold time therefore depends on R_D and the critical current of junction J_H. The reset time τ_R is independent of τ_H and is set by the shunt resistor R_H [1,27].

4. Dynamic inductorless logic gates

Two DHFQ circuits are introduced in this section, an AND gate and an OR gate. A fundamental limitation of pulse based logic is the inability to provide clockless inversion. Inversion operations can however be propagated to the clocked latches separating the combinational logic elements [1,19]. AND and OR gates comprise a functionally complete logic set. A dynamic HFQ AND gate is described in Section 4.1. A dynamic HFQ OR gate is presented in Section 4.2. The circuits are based on the 1 kA/cm^2 2ϕ-JJ model [14], with an I_cR_N product of 0.4 mV. The 0-JJ model used to analyze the circuits is the Whiteley Research Josephson junction model [28].

4.1. AND gate

The proposed DHFQ AND gate is shown in Fig. 3. Rather than the large storage inductors used in DSFQ gates, two 0-JJs, J_{L1} and J_{L2}, are used at the input ports of the two-input DHFQ AND gate. The output is determined by switching junction J_M. Transmitter (Tx) and receiver (Rx) cells are required for passive transmission line (PTL) routing in SFQ circuits. These cells are often incorporated within the standard logic cells. Inputs A and B are connected to the DHFQ AND gate by the receivers shown in Figs. 4(a) and 4(b). The transmitter is shown in Fig. 4(c).

A DHFQ AND gate operating at 10 GHz is shown in Fig. 5, depicting the phase dynamics of the JJs within the gate and the voltage at the

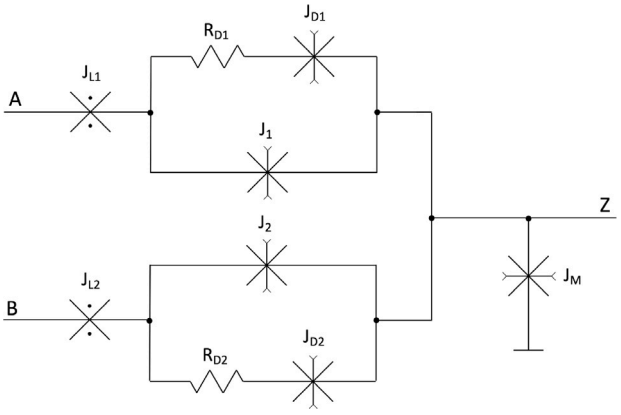

Fig. 3. Two-input DHFQ AND gate. The circuit parameters are listed in Table 1.

Table 1
Parameter values of the dynamic AND gate.

Junction	I_c (μA)	R_{shunt} (Ω)
J_{RA1}, J_{RA2}, J_{RB1}, J_{RB2}, J_{T1}, J_{T2}	70	3
J_{RA3}, J_{RA4}, J_{RB3}, J_{RB4}, J_{T3}, J_{T4}	250	1.6
J_{L1}, J_{L2}	100	4
J_{D1}, J_{D2}	50	–
J_1, J_2	80	2
J_M	100	5
Bias current source		**Current (μA)**
I_{RA1}, I_{RA2}, I_{RB1}, I_{RB2}, I_{T1}, I_{T2}		55
Resistor		**Resistance (Ω)**
R_{D1}, R_{D2}		0.5
R_{TX}		1

inputs and output of the gate. The hold time is set by the current in the output loop, as shown in Fig. 6. In this figure, the current through the "inductor" junctions I_{L1} and I_{L2} is shown as well as the current I_M at the output junction. The related input and output pulses are also shown for clarity. The first HFQ pulse arrives at the gate, in this case at input A, and propagates by switching the 2ϕ-junctions within the receiver. This pulse is stored within the storage loop. The arrival of another pulse at input B within the dynamic hold time τ_H increases the current in the output junction J_M, as shown in Fig. 6. This increase in current switches junction J_M, producing a pulse at output port Z. If the second pulse does not arrive within τ_H, junctions J_1 and J_{D1} within the storage loop switch, resetting the gate to the ground state (see Fig. 5(a)).

The value of the parameters of the AND gate is listed in Table 1. The resulting operation of the gate is depicted in Fig. 5 with τ_H = 36 ps. From (5), a critical current of the storage junction I_{c_L} of 100 μA results in a Josephson inductance of approximately 3.3 pH. The margins of the currents driving the transmitter and receiver of the DHFQ AND gate are −38%, +31%.

4.2. OR gate

The proposed DHFQ OR gate is shown in Fig. 7. The transmitter and receiver are the same as in the AND gate and are depicted in Fig. 4. The OR gate is characterized by the addition of a current source at output I_{OUT}. This increase in output current switches junction J_M in response to an input pulse [26]. The increase in current leads to erroneous switching of the input junctions in the case where only one pulse arrives at the input. This behavior is depicted in Fig. 8. Note the phase dynamics of the output junction J_M, receiver junctions J_{RA1} and J_{RB1}, as well as the related HFQ pulses. The arrival of the pulse

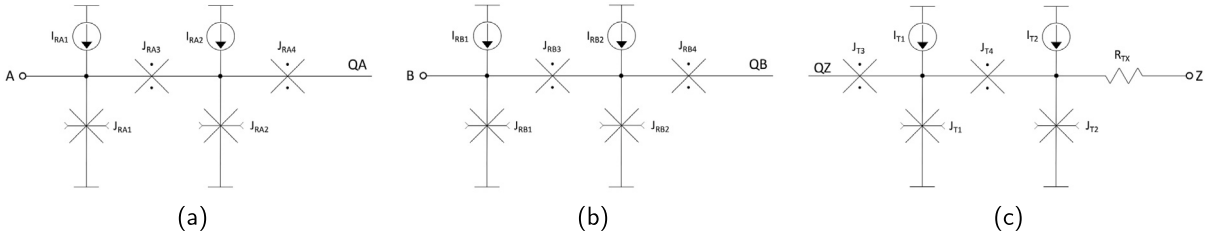

Fig. 4. Receiver and transmitter, (a) receiver for input A, (b) receiver for input B, and (c) transmitter.

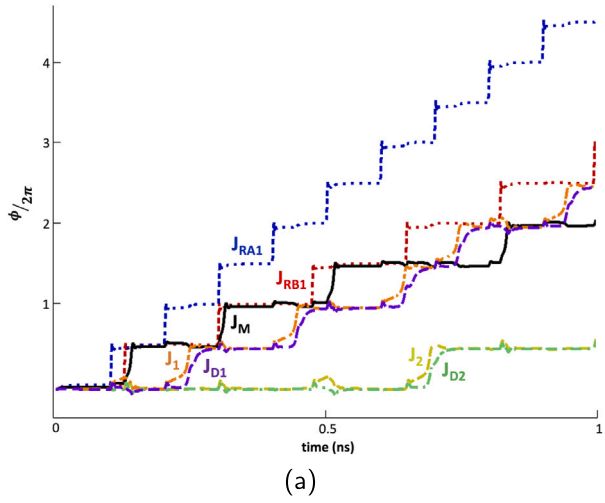

Fig. 5. Circuit behavior of the two-input DHFQ AND gate, (a) phases of the Josephson junctions within the gate, and (b) corresponding HFQ pulses at inputs A and B and output Z.

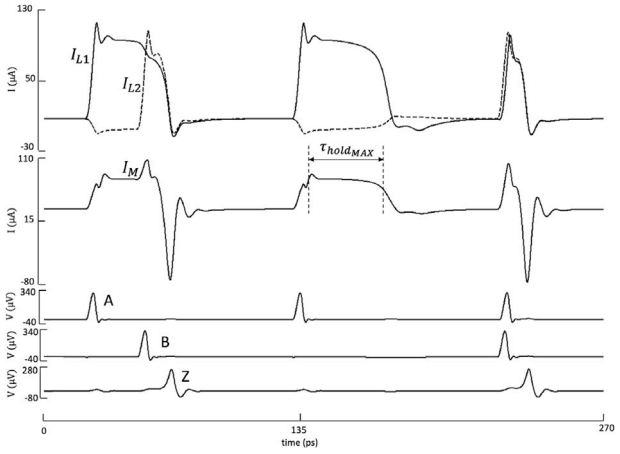

Fig. 6. AND gate waveform characteristics: loop currents I_{L1} and I_{L2}, output current I_M, and corresponding input (A and B) and output (Z) pulses.

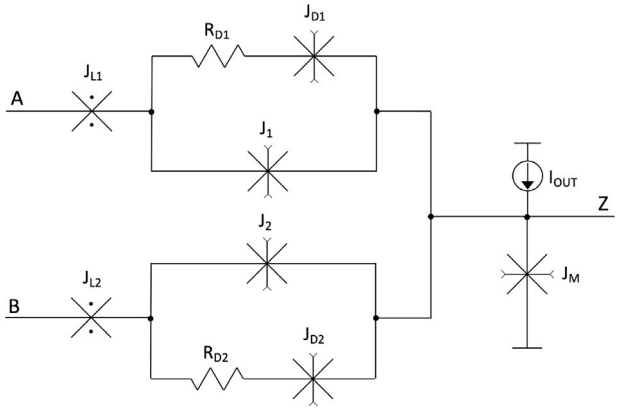

Fig. 7. Two-input DHFQ OR gate. The circuit parameters are listed in Table 2.

at input A, not followed by a pulse at input B, switches J_M, resulting in correct operation at the output of the gate. Switching J_M, however, switches junction J_{RB1}, propagating the pulse back to the input port of the gate [26]. To prevent this effect from occurring, the critical current of output junctions J_{RA2} and J_{RB2} of the receiver gate is higher. Correct operation of the DHFQ OR gate is shown in Fig. 9. When the second pulse does not arrive at the input of the gate, junctions J_D and J_H within the storage loop switch. This delayed switching of the storage loop junctions sets the hold time of the gate. If another pulse arrives before J_D and J_H completely switch, the gate resets to the ground state, and the second pulse is not produced at the output.

The value of the parameters of the OR gate is listed in Table 2. The resulting operation of the gate is depicted in Fig. 9 with $\tau_H = 78$ ps. The margins of the currents driving the transmitter and receiver for the DHFQ OR gate are −45%, +18%, while the margins of the output current I_{OUT} are −26%, +13%.

5. DHFQ half adder and comparison of logic families

To evaluate DHFQ logic, a DHFQ half adder utilizing a combination of DHFQ and HFQ gates is considered. The half adder is described in Section 5.1. DHFQ circuits operate without storage inductors. Parasitic inductances within the device as well as interconnect inductances however exist. The effects of the parasitic inductance on circuit operation are described in Section 5.2. To discuss tradeoffs in the design of DHFQ logic, a comparison among DHFQ, DSFQ, and synchronous RSFQ is provided in Section 5.3.

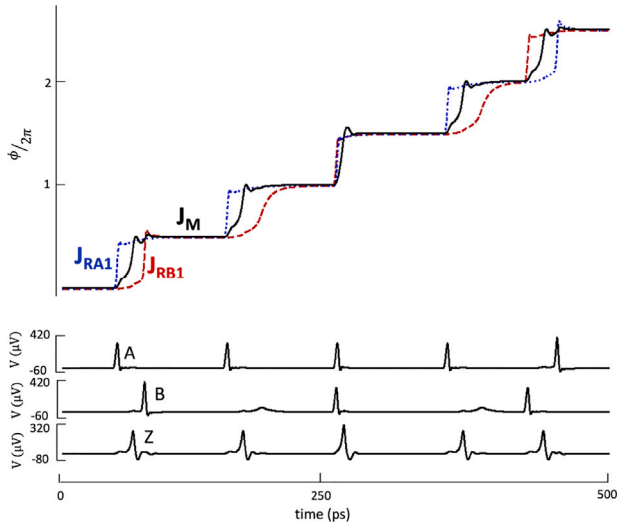

Fig. 8. Back propagation of flux in the DHFQ OR gate.

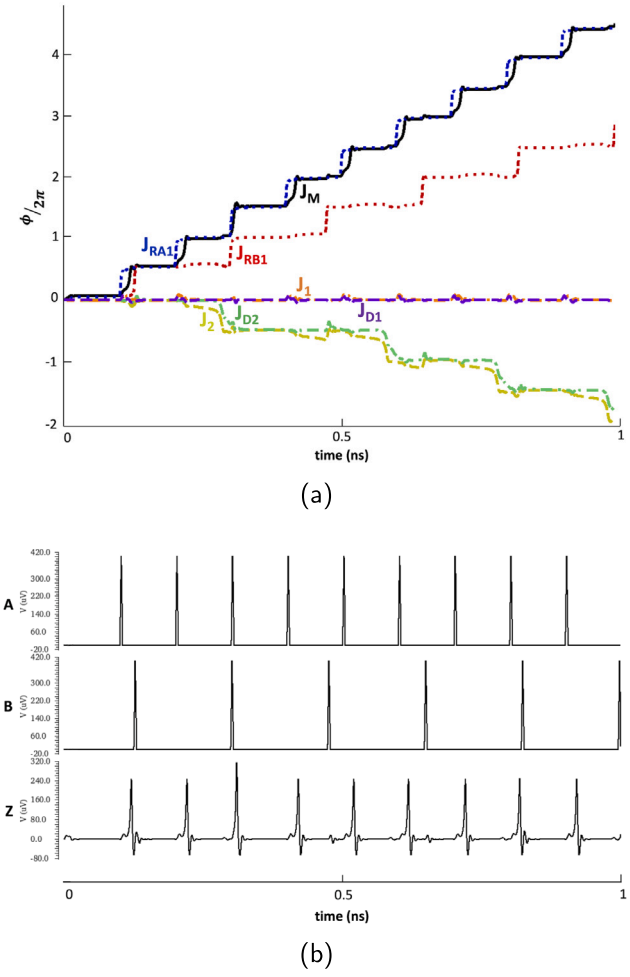

Fig. 9. Circuit behavior of the two-input DHFQ OR gate, (a) phases of the Josephson junctions within the gate, and (b) corresponding HFQ pulses at inputs A and B and output Z.

5.1. Half adder

A combination of DHFQ and HFQ gates is used within a DHFQ half adder, including a DHFQ AND and OR gate as well as an HFQ splitter [16] and HFQ NOT gate. The NOT gate, based on [15], is shown in Fig. 10. The input HFQ pulse switches junction J_{IA}, creating a circulating current within the J_{IA} - J_{I3} - J_{I4} - J_{ICLK} loop. The arrival of the clock pulse switches J_{ICLK}. If, however, the clock pulse arrives before the input pulse is stored, the current is higher at output junction J_{IM}. Switching this junction produces an HFQ pulse at the output. Two additional 2ϕ-JJs, J_{I1} and J_{I2}, isolate the inputs and prevent the flux from propagating backwards.

Table 2
Parameter values of the dynamic OR gate.

Junction	I_c (μA)	R_{shunt} (Ω)
J_{RA1}, J_{RB1}, J_{T1}, J_{T2}	70	3
J_{RA2}, J_{RB2}	140	3
J_{RA3}, J_{RA4}, J_{RB3}, J_{RB4}, J_{T3}, J_{T4}	250	1.6
J_{L1}, J_{L2}	100	4
J_{D1}, J_{D2}	50	–
J_1, J_2	90	2
J_M	100	5
Bias current source		**Current (μA)**
I_{RA1}, I_{RA2}, I_{RB1}, I_{RB2}, I_{T1}, I_{T2}		55
I_{OUT}		90
Resistor		**Resistance (Ω)**
R_{D1}, R_{D2}		0.5
R_{TX}		1

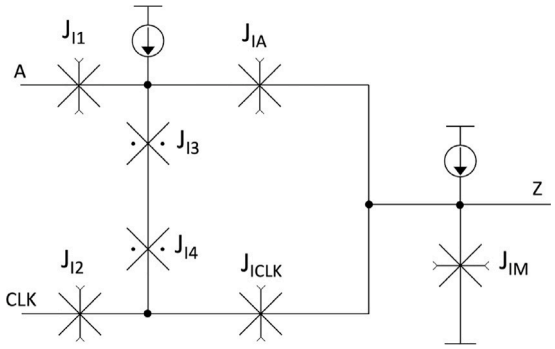

Fig. 10. HFQ NOT gate [15].

A DHFQ half adder is depicted in Fig. 11. Inputs A and B are each connected through an HFQ splitter to the DHFQ AND and OR gates described in Section 4. The output of the AND gate is inverted by an HFQ NOT gate. A self-timing technique is used for inversion, as described in [7]. Note that the output of the OR gate serves as a clock signal for the inverter. Chains of HFQ JTLs with 0-JJs serving as inductors introduce delay to adjust the skew between the clock signal and the input of the inverter. Alternatively, datapath balancing in circuits with tight skew margins can be achieved by inserting mirrored delay paths that replicate gate sequences from the critical paths [27]. The sum signal (S) is the output of the NOT gate, while the carry signal (C) is the non-inverted output of the AND gate with the output delayed. The operation of the half adder is illustrated in Fig. 12.

This circuit demonstrates the logical operation and integration of DHFQ and HFQ components. The performance of DHFQ logic strongly depends on the architectural topology. One possible direction is to utilize DHFQ logic between synchronous HFQ blocks, reducing path balancing requirements and improving throughput [27]. Alternatively, DHFQ-based majority logic can be used, offering narrower pipeline depth and increased performance [19].

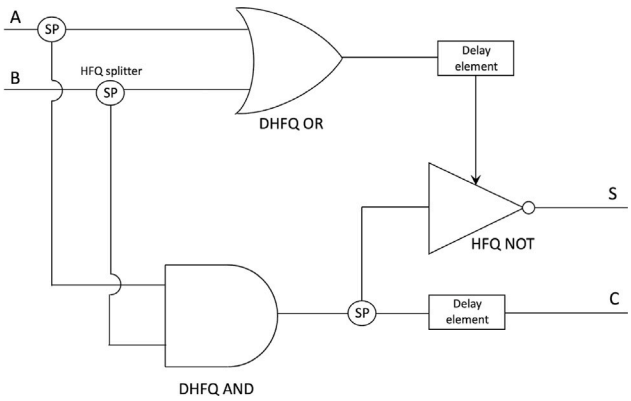

Fig. 11. DHFQ half adder.

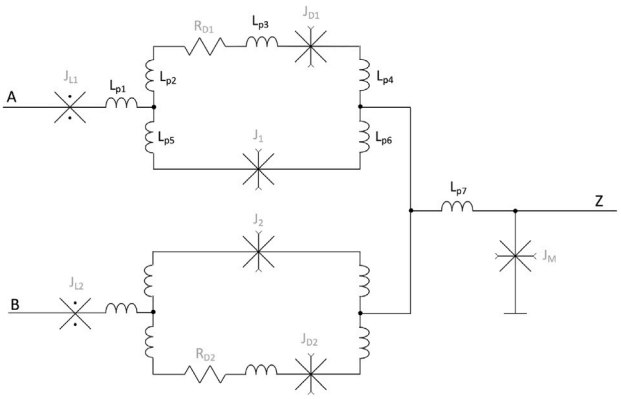

Fig. 13. DHFQ AND gate with parasitic inductances.

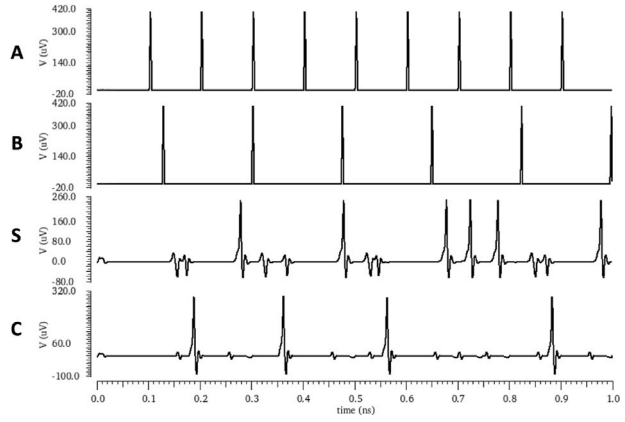

Fig. 12. Operation of the DHFQ half adder shown in Fig. 11. The output of the NOT gate produces the sum signal (S). The carry signal (C) is produced by the AND gate.

5.2. Parasitic inductance

Parasitic inductances in SFQ circuits typically arise from the connections between metal layers. An additional parasitic inductance is introduced by the connections between circuit elements [14]. These parasitic inductances affect the distribution of current and the operating margins of the superconductive circuits.

The parasitic inductances within a DHFQ AND gate are depicted in Fig. 13. These parasitic inductances can significantly degrade the dynamic hold time of the DHFQ circuits. Inductors L_{p1} and L_{p7} increase the hold time by contributing to the storage inductance of the dynamic storage loop. For L_{p1}, a small dependence between the inductance and τ_H is observed between 0 and 0.8 pH. Between 0.8 pH and 2.4 pH, τ_H increases exponentially. Above 2.4 pH, the operation of the AND gate is disturbed. Similar behavior is observed for L_{p7}; a small increase in τ_H between 0 and 1 pH, and an exponential increase between 1 pH and 3.8 pH.

L_{p2}, L_{p3}, and L_{p4} redistribute the current through the branches of the storage loop, increasing the current through J_1. This increase in current produces a smaller τ_H. The reduction in hold time is small between 0 and 1.5 pH. L_{p5} and L_{p6}, however, reduce the current through J_1, increasing τ_H. This strong dependence demonstrates the importance of accurately extracting the parasitic inductance within DHFQ circuits.

5.3. Comparison

A comparison of DHFQ logic gates to clockless DSFQ and standard synchronous RSFQ is listed in Table 3. The DSFQ and RSFQ circuits are based on the 10 kA/cm^2 MIT LL SFQ5ee fabrication technology, while DHFQ is based on the 1 kA/cm^2 technology. RSFQ is also described for comparative reasons based on a 1 kA/cm^2 technology.

The inductance area for DSFQ gates is extracted from the cell library described in [26] by measuring the primary storage inductors in each physical layout. The wiring between junctions, connections to the bias lines, and the Rx/Tx inductors are omitted. The same approach is applied to the 10 kA/cm^2 RSFQ standard cells developed within the SuperTools project [29]. For the 1 kA/cm^2 RSFQ technology, two processes are considered, HYPRES [30] and Fluxonics RSFQ1H based on the cell library developed by Bakolo [31]. The inductance area of the RSFQ1H OR gate layout is approximately 665 μm^2. Assuming a 4 μm inductor line width with the parameters reported in [14], the area of the inductance in the corresponding HYPRES technology is 480 μm^2. Data representative of the HYPRES process are listed in Table 3.

All-JJ DHFQ cells are smaller than 0-JJ gates. The reduction in area is due to the smaller inductance, as large storage inductors are no longer required. Up to 53 μm^2 in inductance area is saved per gate as compared to DSFQ. Considering the inductors within the DSFQ transmitter and receiver, 84 μm^2 and 116 μm^2 in inductance area is saved for, respectively, the AND and OR gate.

The delay of the DSFQ and DHFQ gates is dependent on the skew between the arrival of the input pulses to the gate and the switching of the output junction. For the OR gate, this skew is between the first input pulse and the output pulse. For the AND gate, this delay describes the skew between the second input pulse and the output pulse. The delay of standard clocked RSFQ gates is the CLK-to-Q delay. Note that the technology for the 2ϕ circuits is 1 kA/cm^2 [14]. A larger delay in DHFQ is therefore expected as compared to DSFQ and RSFQ logic based on a 10 kA/cm^2 technology. As listed in Table 3, the delay of a standard clocked RSFQ gate based on the 1 kA/cm^2 technology is significantly larger (22 ps vs. 9 ps for the 10 kA/cm^2 RSFQ OR gate [14]).

As discussed in Section 2, 2ϕ-JJs require less energy to transition between equilibrium states. This characteristic results in a smaller bias current to operate DHFQ circuits as compared to DSFQ and standard clocked RSFQ gates. DHFQ AND and OR gates exhibit, respectively, a decrease in bias current of 100% and 65% as compared to DSFQ gates. Considering the bias current used for the transmitter and receiver, the decrease in bias current is 42% and 59% for, respectively, the AND and OR gate.

The power dissipated by the bias network is the largest contributor to the overall power dissipation of SFQ and HFQ circuits [32]. In the case of RSFQ bias topologies, static power P_{bias} is dissipated, scaling with the bias current,

$$P_{bias} = V_{bias} I_{bias}, \tag{6}$$

where V_{bias} is the voltage on the bias bus. The same V_{bias} for DHFQ and DSFQ circuits dissipates 2.84 times less static power in a DHFQ

Table 3
Comparison between DHFQ, DSFQ, and RSFQ cells.

	AND gate			OR gate			
	RSFQ ($10\ kA/cm^2$)	DSFQ ($10\ kA/cm^2$)	DHFQ ($1\ kA/cm^2$)	RSFQ ($10\ kA/cm^2$)	DSFQ ($10\ kA/cm^2$)	RSFQ ($1\ kA/cm^2$)	DHFQ ($1\ kA/cm^2$)
Inductance area	80 μm^2	42 μm^2	–	80 μm^2	53 μm^2	480 μm^2	–
Gate delay	5 ps	4 ps	7 ps	5 ps	5 ps	22 ps	9 ps
Gate bias current	590 μA	130 μA	–	650 μA	256 μA	610 μA	90 μA
Tx/Rx bias current	836 μA	436 μA	330 μA	836 μA	772 μA	810 μA	330 μA

OR gate. Note that, while the power dissipation is reduced, the power delivery system consumes area similar to DSFQ circuits [26].

Another indicator of logic efficiency is dynamic power dissipation, resulting from switching the Josephson junctions. The average energy loss per switching event of a Josephson junction is [11]

$$\overline{E_{sw}} = \overline{I_b} \int V(t)dt, \tag{7}$$

where $\overline{I_b}$ is the average bias current. $\int V(t)dt$ is a single flux quantum for a 0-JJ and a half flux quantum for a 2ϕ-junction. For dynamic SFQ and HFQ gates, the greatest energy is dissipated within an OR gate when only one input receives a pulse. This operation switches three junctions during a logic cycle. The energy loss is 0.18 aJ and 1.2 aJ for, respectively, DHFQ and DSFQ logic. The dynamic operation of 2ϕ-junctions is 6.7 times more energy efficient.

The margins of the bias source I_{OUT} within the DHFQ OR gate are −26%, +13%, while the bias margins of the DSFQ gates are ±30% [26]. The larger margins of the DSFQ gates indicate that these circuits can be optimized to reduce energy dissipation by lowering I_c of the junctions [33]. Based on junction diameter constraints, the minimum I_c for the SFQ5ee fabrication technology is 38.5 μA [11]. Assuming a minimum I_c of 40 μA in a DSFQ OR gate, close to the technology constraint, $\overline{I_b}$ of the circuit can be scaled by ≈2.2. The energy dissipated during a logic cycle for the DSFQ OR gate with reduced critical current is 0.55 aJ. The energy loss of the DHFQ gate is three times less due to the inherently lower switching energy of 2ϕ-junctions stemming from HFQ operation. Note that scaling the critical current of the junctions affects the margins of the circuit, increasing the bit error rate [11].

Despite the promising advantages of 2ϕ-JJ circuits [9,14–16], fabrication of these junctions faces multiple challenges. Most of the experimental data is based on the dominant second harmonic within a small temperature range around the 0-π transition of the ferromagnetic junctions [18,21]. The robustness of the second harmonic in the CPR based on spin–triplet pairing has been predicted [23] and experimentally characterized [17,24]. The model described in [14] considers the basic parameters of the second harmonic. As research on 2ϕ-junctions advances, more accurate models may be developed, providing enhanced guidelines for HFQ circuit design.

The primary advantage of HFQ logic as compared to standard SFQ circuits is integration density. 2ϕ-JJ-based HFQ cells are approximately 50% smaller than SFQ cells utilizing the same technology [16]. Majority logic based on DHFQ gates can also be developed, reducing the logic depth and, consequently, the physical area [19]. Despite smaller bias currents, power delivery remains fundamental to SFQ circuits, hindering scalability. Significant further development of 2ϕ-JJ devices is necessary to exploit the full potential of DHFQ and related HFQ circuits.

6. Conclusions

Inductorless dynamic superconductive logic based on the DSFQ logic family is introduced in this paper. By leveraging the unique characteristics of 2ϕ-Josephson junctions, such as bistable behavior and half flux quantum pulse generation, the proposed circuit topology eliminates the need for large storage inductors. Clockless gates also enable the effective use of asynchronous design methodologies, alleviating area issues related to global clocking of SFQ circuits. The dynamic logic gates, including AND and OR gates, offer a power efficient and scalable solution for high speed superconductive digital circuits, enabling clockless operation while facilitating the integration of large scale digital systems. The Josephson inductance of a 0-JJ is utilized for storage rather than a lumped passive inductor. As compared to DSFQ, this approach saves up to 53 μm^2 of loop inductance area within a single dynamic logic gate. 59% less delay is achieved in DHFQ circuits than RSFQ gates in the same technology ($1\ kA/cm^2$). The low switching energy of 2ϕ-junctions also lowers the bias current requirements. The decrease in bias current as compared to DSFQ is 42% and 59% for, respectively, the AND gate and OR gate including the transmitter and receiver gates, resulting in a 6.7 times higher energy efficiency.

CRediT authorship contribution statement

Ana Mitrovic: Conceptualization, Methodology, Software, Validation, Investigation, Visualization, Writing – original draft. **Eby G. Friedman:** Resources, Writing – review & editing, Supervision, Project administration, Funding acquisition.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

References

[1] S.V. Rylov, Clockless dynamic SFQ AND gate with high input skew tolerance, IEEE Trans. Appl. Supercond. 29 (5) (2019) 1–5.
[2] I. Nagaoka, R. Kashima, M. Tanaka, S. Kawakami, T. Tanimoto, T. Yamashita, K. Inoue, A. Fujimaki, 50-GFLOPS floating-point adder and multiplier using gate-level-pipelined single-flux-quantum logic with frequency-increased clock distribution, IEEE Trans. Appl. Supercond. 33 (4) (2023) 1–11.
[3] A. Mitrovic, E.G. Friedman, Thermal exploration of RSFQ integrated circuits, IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 32 (4) (2024) 728–738.
[4] J.-H. Yang, G.-M. Tang, X.-Y. Zheng, X.-C. Ye, D.-R. Fan, Z.-M. Zhang, N.-H. Sun, Distributed self-clock: A suitable architecture for SFQ circuits, IEEE Trans. Appl. Supercond. 30 (7) (2020) 1–7.
[5] G. Krylov, E.G. Friedman, Globally asynchronous, locally synchronous clocking and shared interconnect for large-scale SFQ systems, IEEE Trans. Appl. Supercond. 29 (5) (2019) 1–5.
[6] J. Volk, P. Papanikolaou, G. Zervakis, G. Tzimpragos, Synthesis of resource-efficient superconducting circuits with clock-free alternating logic, in: ACM/IEEE Design Automation Conference, 2024, pp. 1–6.
[7] Y. Yamanashi, T. Fujisawa, Z. Li, N. Yoshikawa, Asynchronous single flux quantum logic gates using self-clocking, IEEE Trans. Appl. Supercond. 33 (5) (2023) 1–5.

[8] T. Kawaguchi, K. Takagi, N. Takagi, Rapid single-flux-quantum logic circuits using clockless gates, IEEE Trans. Appl. Supercond. 31 (4) (2021) 1–7.
[9] I.I. Soloviev, V.I. Ruzhickiy, S.V. Bakurskiy, N.V. Klenov, M.Y. Kupriyanov, A.A. Golubov, O.V. Skryabina, V.S. Stolyarov, Superconducting circuits without inductors based on bistable Josephson junctions, Phys. Rev. Appl. 16 (2021) 014052.
[10] T. Jabbari, E.G. Friedman, Flux mitigation in wide superconductive striplines, IEEE Trans. Appl. Supercond. 32 (5) (2022) 1–6.
[11] S.K. Tolpygo, Superconductor digital electronics: Scalability and energy efficiency issues, Low Temp. Phys. 42 (5) (2016) 361–379.
[12] B. Dimov, T. Ortlepp, F.H. Uhlmann, Phase-drop realization within RSFQ digital circuits with reduced Josephson current density, IEEE Trans. Appl. Supercond. 17 (2) (2007) 613–616.
[13] F. Li, Y. Takeshita, M. Tanaka, A. Fujimaki, Superconductor digital circuits with π junctions alone, Appl. Phys. Lett. 122 (16) (2023).
[14] T. Jabbari, M. Bocko, E.G. Friedman, All-JJ logic based on bistable JJs, IEEE Trans. Appl. Supercond. 33 (5) (2023) 1–7.
[15] I. Salameh, E.G. Friedman, S. Kvatinsky, Superconductive logic using 2ϕ—Josephson junctions with half flux quantum pulses, IEEE Trans. Circuits Syst. II 69 (5) (2022) 2533–2537.
[16] H. Cong, S. Razmkhah, M.A. Karamuftuoglu, M. Pedram, Superconductor logic implementation with all-JJ inductor-free cell library, IEEE Trans. Appl. Supercond. 34 (9) (2024) 1–10.
[17] A. Pal, Z. Barber, J. Robinson, M. Blamire, Pure second harmonic current-phase relation in spin-filter Josephson junctions, Nat. Commun. 5 (1) (2014) 3340.
[18] M. Stoutimore, A. Rossolenko, V. Bolginov, V. Oboznov, A. Rusanov, D. Baranov, N. Pugach, S. Frolov, V. Ryazanov, D. Van Harlingen, Second-harmonic current-phase relation in Josephson junctions with ferromagnetic barriers, Phys. Rev. Lett. 121 (17) (2018) 177702.
[19] G. Krylov, E.G. Friedman, Asynchronous dynamic single-flux quantum majority gates, IEEE Trans. Appl. Supercond. 30 (5) (2020) 1–7.
[20] S.K. Tolpygo, V. Bolkhovsky, T.J. Weir, A. Wynn, D.E. Oates, L.M. Johnson, M.A. Gouker, Advanced fabrication processes for superconducting very large-scale integrated circuits, IEEE Trans. Appl. Supercond. 26 (3) (2016) 1–10.
[21] F. Li, L. Wu, L. Chen, S. Zhang, W. Peng, Z. Wang, Measurement of the intrinsic higher harmonic current-phase relation in NbN/NiCu/NbN Josephson junctions, Phys. Rev. B 99 (10) (2019) 100506.
[22] V. Oboznov, V. Bol'ginov, A. Feofanov, V. Ryazanov, A.I. Buzdin, Thickness dependence of the Josephson ground states of superconductor-ferromagnet-superconductor junctions, Phys. Rev. Lett. 96 (19) (2006) 197003.
[23] D. Nikolić, M. Vanević, A.I. Buzdin, Z. Radović, Interference phenomena in Josephson junctions with ferromagnetic bilayers: Spin-triplet correlations and resonances, Phys. Rev. B 106 (2022) 054513.
[24] G.A. Ovsyannikov, A. Sheyerman, A.V. Shadrin, Y.V. Kislinskii, K. Constantinian, A. Kalabukhov, Triplet superconducting correlations in oxide heterostructures with a composite ferromagnetic interlayer, Jetp Lett. 97 (2013) 145–148.
[25] P.K. Sharma, A. Pal, Shunt-free cryogenic memory using ferromagnetic insulator-based Josephson junctions, Appl. Phys. Lett. 125 (5) (2024).
[26] S. Rylov, M. Beck, K. Tien, J. Bulzacchelli, M. Wong, J. Timmerwilke, D. Friedman, Superconducting VLSI logic cell library using DC-powered clockless dynamic SFQ gates and ASIC-style layout template, IEEE Trans. Appl. Supercond. 33 (5) (2023) 1–7.
[27] A. Van Wijk, Development of a DSFQ Cell Library for Superconducting Circuits (Master's thesis), Stellenbosch University, 2023.
[28] Whiteley Research Inc., WRSPICE, [Online]. Available: http://www.wrcad.com/wrspice.html.
[29] R. Freeman, J. Kawa, K. Singhal, Synopsys' journey to enable TCAD and EDA tools for superconducting electronics, in: Government Microcircuit Applications & Critical Technology Conference, 2020.
[30] D. Yohannes, A. Kirichenko, S. Sarwana, S.K. Tolpygo, Parametric testing of HYPRES superconducting integrated circuit fabrication processes, IEEE Trans. Appl. Supercond. 17 (2) (2007) 181–186.
[31] R.S. Bakolo, Design and Implementation of a RSFQ Superconductive Digital Electronics Cell Library (Master's thesis), Stellenbosch University, 2011.
[32] A. Mitrovic, E.G. Friedman, Thermal modeling of rapid single flux quantum circuit structures, IEEE Trans. Electron Devices 69 (5) (2022) 2718–2724.
[33] M. Tanaka, A. Kitayama, T. Takinami, Y. Komura, A. Fujimaki, Bit error rate in low-voltage RSFQ circuits with small critical currents/lowered bias voltages, in: IEEE International Superconductive Electronics Conference, 2013, pp. 1–3.