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ON THE EXTRACTION OF ON-CHIP INDUCTANCE

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Inductance extraction has become an important issue in the design of high speed CMOS circuits. Two characteristics of on-chip inductance are discussed in this paper that can significantly simplify the extraction of on-chip inductance. The first characteristic is that the sensitivity of a signal waveform to errors in the inductance values is low, particularly the propagation delay and the rise time. It is quantitatively shown in this paper that the error in the propagation delay and rise time is below 9.4% and 5.9%, respectively, assuming a 30% relative error in the extracted inductance values. If an *RC* model is used for the same example, the corresponding errors are 51% and 71%, respectively. The second characteristic is that the magnitude of the on-chip inductance is a slow varying function of the width of a wire and the geometry of the surrounding wires. These two characteristics can be exploited by using simplified techniques that permit approximate and sufficiently accurate values of the on-chip inductance to be determined with high computational efficiency.

Keywords: Inductance; *RC*; *RLC*; extraction.

1. Introduction

The importance of on-chip inductance is increasing with faster on-chip rise times and longer wire lengths.[1–15] Wide wires are frequently encountered in clock distribution networks, data buses, and upper metal layers. These wires are low resistance lines that can exhibit significant inductance effects. Furthermore, performance requirements are pushing the introduction of new materials for low resistance interconnect[16–18] and new dielectrics to reduce the interconnect capacitance. These technological advances increase the importance of inductance, as has been described in Refs. 6–8 and 13.

The efficient and accurate extraction of inductance is one of the primary bottlenecks that hinder incorporating on-chip inductance within integrated circuit design tools. To extract on-chip inductance, the return path of the current flowing in an

interconnect line must be determined. Initial work has assumed the return path of the current to be within the substrate.[1–5] However, further investigation has provided evidence that the return path of the current is primarily within the power distribution network and other interconnect lines.[6–12] This characteristic of the return path severely complicates the process of accurately extracting the on-chip inductance since the value of the inductance of a wire not only depends on the wire characteristics but also on the characteristics of the other wires surrounding the line. This problem is further aggravated by the fact that the current return path can be distributed among many power and signal wires, some of which may be hundreds of micrometers away from the wire for which the inductance is being extracted.[1,6–12] Some research on on-chip inductance extraction has been described which places an emphasis on accuracy and the use of expensive 3D numerical algorithms.[1–9] Fortunately, as is shown in this paper, on-chip inductance has two useful characteristics which enable simple methods to be used to extract the inductance. These two characteristics are described and analyzed in Sec. 2. A summary is provided in Sec. 3.

2. Characteristics of On-Chip Inductance which Simplify the Extraction Process

Two characteristics of on-chip inductance can be exploited to simplify the extraction process of on-chip inductance. These two characteristics are discussed in this section.

First characteristic: The sensitivity of a signal waveform to errors in the inductance values is low, particularly the propagation delay and rise time.

Inductance only appears under a square root function in a waveform or timing expression characterizing a signal. The reason for this square root dependence is physical since an LC constant has the dimensions of time squared, where L and C are any inductance and capacitance values in the circuit, respectively. The square root dependence can be compared to the linear dependence of the delay expressions on the resistance since any RC constant has the dimensions of time, where R is any resistance of the circuit. For example, according to the equivalent Elmore delay for RLC trees that was introduced in Ref. 19, the 50% delay of the signal at node i of an RLC tree is

$$t_{pdi} = 1.047 \cdot \sqrt{\sum_k C_k L_{ik}} \cdot e^{-\frac{\zeta_i}{0.85}} + 0.695 \cdot \sum_k C_k R_{ik}\,, \tag{1}$$

where ζ_i is the damping factor at node i and is

$$\zeta_i = \frac{1}{2} \frac{\sum_k C_k R_{ik}}{\sqrt{\sum_k C_k L_{ik}}}\,. \tag{2}$$

The summation variable k operates over all of the capacitors in the circuit. R_{ik} (L_{ik}) is the common resistance (inductance) from the input to nodes i and k. For example,

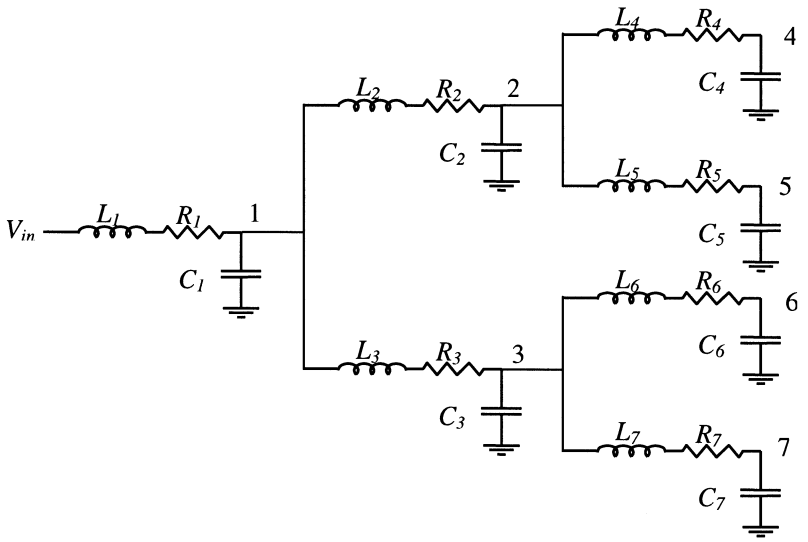

Fig. 1. General RLC tree.

as shown in Fig. 1, $R_{77} = R_1 + R_3 + R_7$, $R_{67} = R_1 + R_3$, and $R_{27} = R_1$. The square root dependence of the propagation delay on the inductance values in an RLC tree is evident in Eqs. (1) and (2).

To quantify the error in the propagation delay due to errors in the extracted inductance, consider an extraction tool that generates a value of the extracted inductance with a maximum error E relative to the actual inductance value. Alternatively, the extracted inductance based on this extraction tool is in the range between $L\,(1-E)$ and $L\,(1+E)$ where L is the actual inductance value. The worst case error in the propagation delay occurs when all of the inductance values are overestimated by a maximum factor of $(1+E)$ [or underestimated by the minimum factor of $(1-E)$]. In that case, the propagation delay in Eq. (1) becomes

$$t_{pdi\_E} = 1.047 \cdot \sqrt{1+E} \cdot \sqrt{\sum_k C_k L_{ik}} \cdot e^{-\frac{\zeta_i}{0.85 \cdot \sqrt{1+E}}} + 0.695 \cdot \sum_k C_k R_{ik}\,, \qquad (3)$$

where L_{ik} represent the actual inductance values and Eq. (1) represents the actual propagation delay. Errors in the extracted inductance values result in a worst case relative error of the propagation delay as given by

$$Et_{pdi\_E} = \left| \frac{t_{pdi} - t_{pdi\_E}}{t_{pdi}} \right| = \left| \frac{1.047 \cdot [e^{-\frac{\zeta_i}{0.85}} - \sqrt{1+E} \cdot e^{-\frac{\zeta_i}{0.85 \cdot \sqrt{1+E}}}]}{1.047 \cdot e^{-\frac{\zeta_i}{0.85}} + 1.39 \cdot \zeta_i} \right|. \qquad (4)$$

The worst case error in the propagation delay only depends upon the damping factor and the worst case error in the extracted inductance. Another interesting metric is the error in the propagation delay due to neglecting inductance altogether

and using an RC interconnect model. The propagation delay in this case can be calculated by letting $L_{ik} \to 0$ in Eq. (1) and is

$$t_{pdi\_RC} = 0.695 \cdot \sum_k C_k R_{ik} \,, \tag{5}$$

which is simply the Elmore (Wyatt) approximation of the propagation delay.[20,21] Thus, the relative error in the propagation delay when inductance is not extracted and an RC model is used is

$$Et_{pdi\_RC} = \left| \frac{t_{pdi} - t_{pdi\_RC}}{t_{pdi}} \right| = \left| \frac{1.047 \cdot e^{-\frac{\zeta_i}{0.85}}}{1.047 \cdot e^{-\frac{\zeta_i}{0.85}} + 1.39 \cdot \zeta_i} \right| . \tag{6}$$

The relative error in the propagation delay due to using an RC model is only a function of the damping factor.

The worst case error in the propagation delay due to errors in the extracted inductance values as given by Eq. (4) is plotted in Fig. 2 versus ζ_i for several values of E. Equation (6) is also plotted in Fig. 2. Note in Fig. 2 that including the extracted inductance when evaluating the propagation delay significantly improves the accuracy as compared to an RC model even with a 30% error in the extracted inductance. The error in the propagation delay decreases with increasing ζ_i since a higher damping factor means the inductance has less effect and most of the delay is due to the RC time constants in the circuit, thereby diminishing the relevance of the error caused by inexact inductance values. Note also that the improvement in accuracy by extracting approximate values of the inductance as compared to

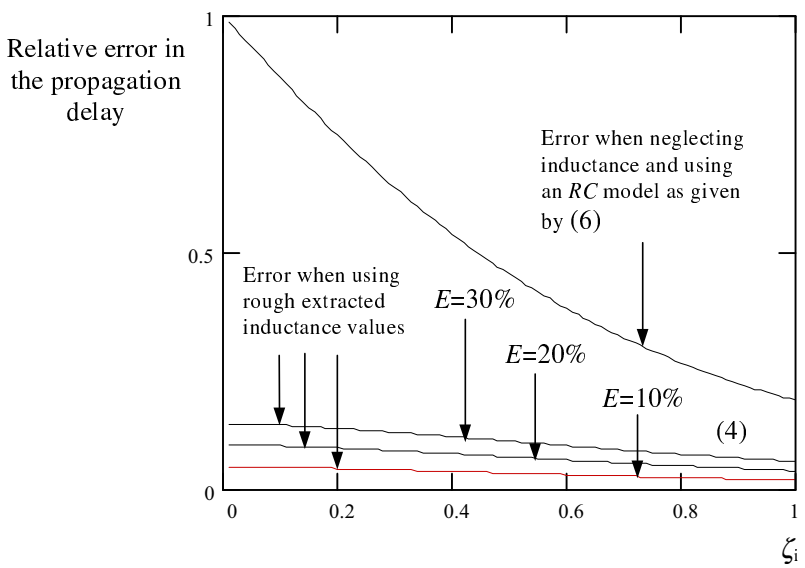

Fig. 2. The relative error in Eqs. (4) and (6) is plotted versus ζ_i. Several values of E in Eq. (4) are used as labeled in the figure.

using an *RC* model increases as the importance of the inductance increases (for small ζ_i, which is the range of primary interest). Numerical values of the error in the propagation delay are listed in Table 1 with different accuracy levels of the extracted inductance values and with no inductance. At $\zeta_i = 0.4$ and with a relative error in the inductance values of 30%, the relative error in the propagation delay improves by a factor of five as compared to using an *RC* model.

As an example, consider the *RLC* tree shown in Fig. 3. AS/X[22] simulations are performed for the *RLC* tree shown in Fig. 3 with the inductance values shown in the figure, with no inductance (an *RC* model), and with all of the inductance values increased by 10%, 20%, and 30%. These simulations are depicted in Fig. 4. Note in the simulations that using an approximate inductance estimation greatly improves the accuracy of the waveform as compared to using an *RC* model. The 50% delay

Table 1. Relative error of the propagation delay when inductance is extracted and when an *RC* model is used. The relative errors for the extracted inductance values are 10%, 20%, and 30%.

	Relative error of the propagation delay			
ζ_i	Extraction error $E = 10\%$	Extraction error $E = 20\%$	Extraction error $E = 30\%$	*RC* model (no inductance)
0.0	4.9%	9.5%	14%	100%
0.2	4.5%	8.8%	13%	75%
0.4	3.9%	7.6%	11%	54%
0.6	3.2%	6.3%	9.3%	39%
0.8	2.6%	5.1%	7.5%	27%
1.0	2%	4%	6%	19%

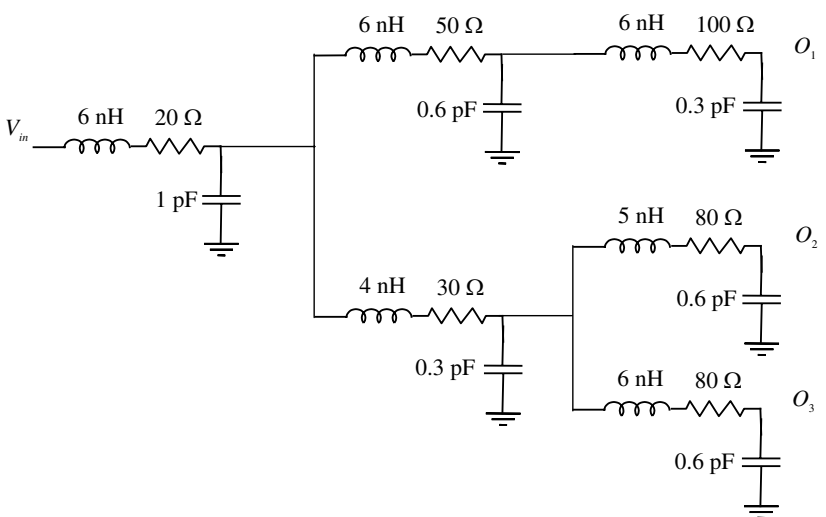

Fig. 3. An example of an *RLC* tree.

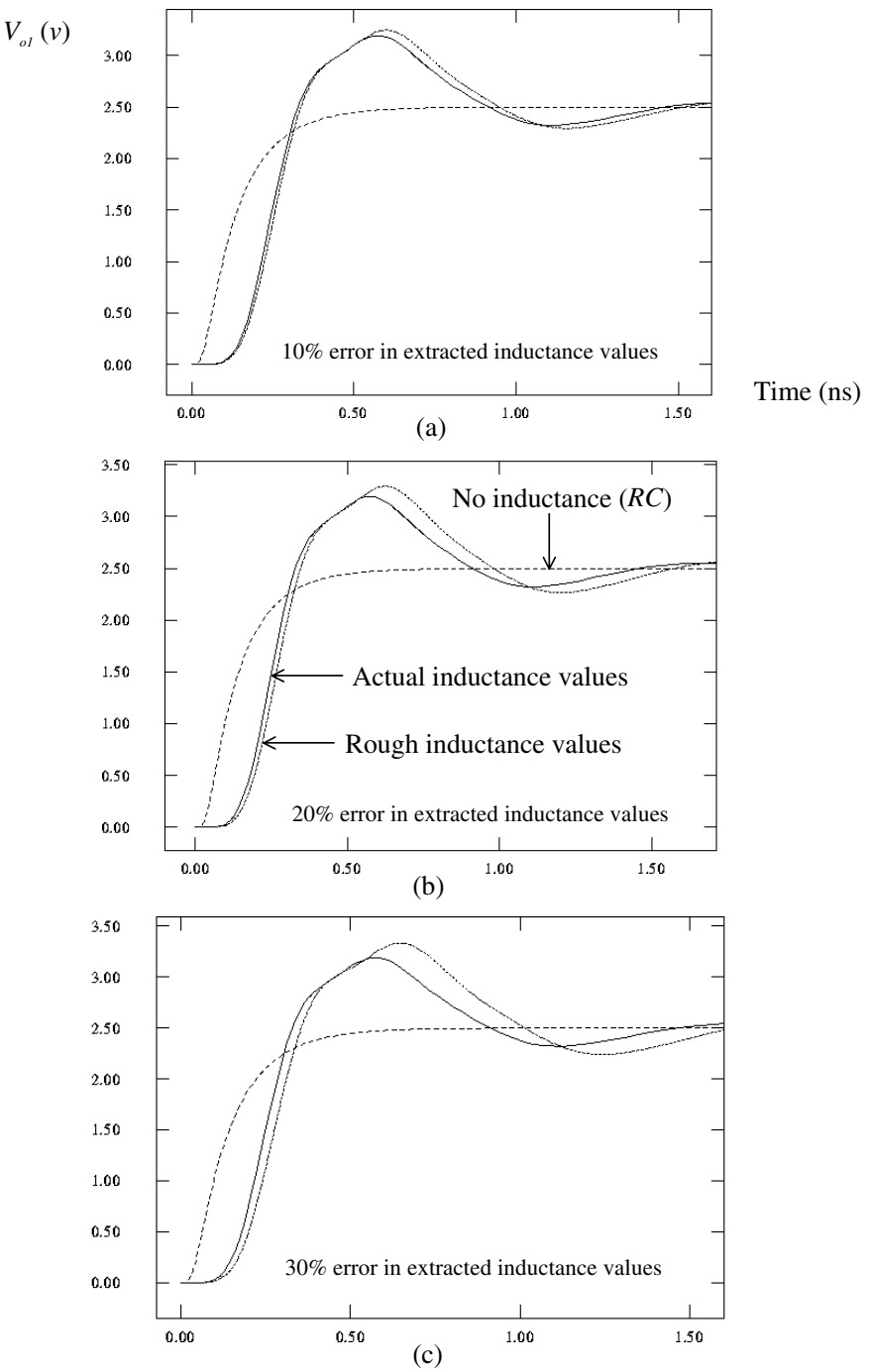

Fig. 4. AS/X[22] simulations of the *RLC* tree shown in Fig. 3 at output node O_1 with the actual inductance values, with no inductance (an *RC* model), and with all of the inductance values increased by (a) 10%, (b) 20%, and (c) 30%.

Table 2. The 50% delay and the 10% to 90% rise time from AS/X[22] simulations for the *RLC* tree shown in Fig. 3 with the actual inductance values, with all of the inductance values increased by 10%, 20%, and 30%, and with no inductance (an *RC* model).

Relative error in inductance values		*RC* (no inductance)	Relative error ⟷	Actual inductance values	Relative error ⟷	Rough inductance values
10%	t_{pd} (ps)	116	51%	233	3.4%	241
	t_r (ps)	260	71%	152	2.0%	155
20%	t_{pd} (ps)	116	51%	233	6.9%	249
	t_r (ps)	260	71%	152	3.9%	158
30%	t_{pd} (ps)	116	51%	233	9.4%	255
	t_r (ps)	260	71%	152	5.9%	161

and the 10% to 90% rise time are listed in Table 2 for the circuit simulations shown in Fig. 4. With a 30% error in the inductance values, the propagation delay differs by 9.4% from the actual value as compared to 51% if an *RC* model is used. The improvement in the rise time is even greater. The rise time differs from the actual value by 5.9% with a 30% error in the inductance values as compared to a 71% error when an *RC* model is used. Note that these errors are worst case errors since the circuits are simulated after overestimating all of the inductance values in the circuit by 30%. Practically, some of the inductance values are overestimated while others are underestimated. The error in the different directions partially cancels, thereby reducing the error in the total delay. The maximum error in the waveform shape occurs around the overshoots (see Fig. 4). However, estimating the overshoot requires less accuracy since the overshoot is usually evaluated to decide if the overshoot is within an acceptable limit. This high tolerance of the delay expressions to errors in the extracted inductance encourages the use of simplified techniques with higher computational efficiency to extract the on-chip inductance.

Second characteristic: The value of the on-chip inductance is a slow varying function of the width of the wire and the geometry of the surrounding wires.

Most of the analytical formulae approximating the on-chip inductance has a logarithmic dependence on the width of the interconnect,[4,5,11] which is a slow varying function. Also, numerical three-dimensional extraction methods based on solving Maxwell's differential equations and experimental measurements have demonstrated this slow varying dependence of the on-chip inductance on the wire width and the surrounding wire geometries.[6–9] The on-chip inductance values for a high performance VLSI circuit are typically between 4 nH/cm and 6 nH/cm for the range of wire widths used in Refs. 6–9.

This characteristic together with the low sensitivity of the delay expressions to errors in the extracted inductance permit extraction techniques as simple as using a constant inductance value per unit length of interconnect of 5 nH/cm. Using

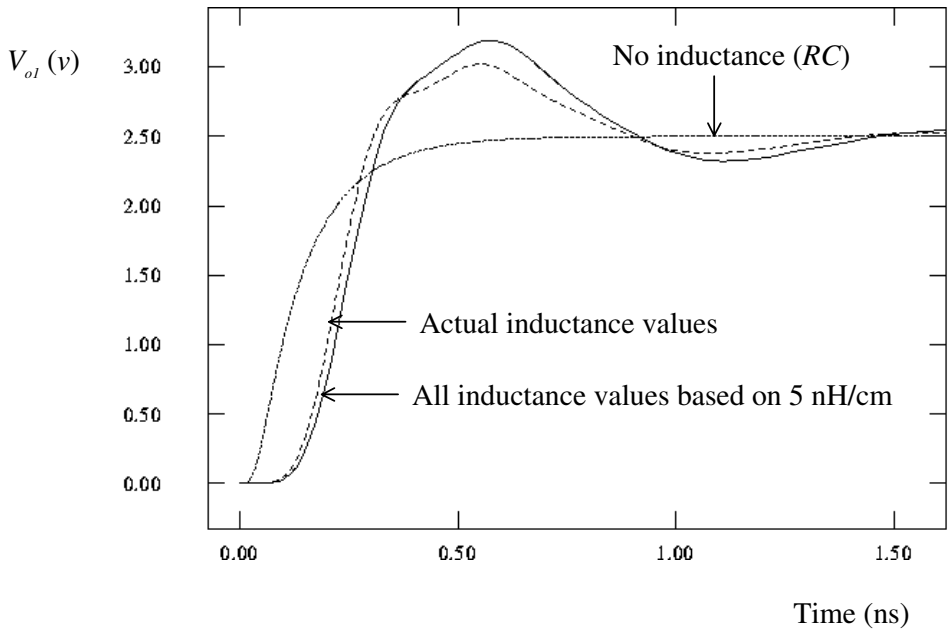

Fig. 5. AS/X^{22} simulations of the *RLC* tree shown in Fig. 3 at output node O_1 with the actual inductance values, with no inductance (an *RC* model), and with all of the inductance values recalculated based on a value of 5 nH/cm inductance per unit length.

this constant average value technique results in a maximum overestimation of 25% and a maximum underestimation of 16.6% for the inductance values. According to this sensitivity analysis, these errors in the inductance values result in errors of less than 9% in the propagation delay and below 5% in the rise time for typical damping factors commonly seen in VLSI circuits (i.e., $\zeta_i > 0.4$).[6–9] As an example, all of the inductance values in the tree shown in Fig. 3 are recalculated assuming a value of 5 nH/cm. AS/X^{22} simulations are performed for the resulting tree and for the tree with actual inductance values. These simulations are shown in Fig. 5. The actual values of the propagation delay and rise time are 233 ps and 152 ps, respectively. The estimated propagation delay improves from 116 ps when using an *RC* model to 215 ps when using a constant inductance value of 5 nH/cm, which is equivalent to an improvement in the relative error from 51% to 7.7%. The estimated rise time improves from 260 ps to 146 ps, which is equivalent to an improvement in the relative error from 71% to 3.9%. Using this method there is an insignificant overhead in including inductance. However, a significant amount of information characterizing the signal waveform shape which is lost when using an *RC* model can be retrieved by using this simple technique. If a more accurate inductance estimation is required, other methods can be used such as simple curve fitting or look-up table methods to quickly estimate the inductance based on the wire width and certain characteristics of the power distribution network such as the metal

pitch. Other techniques can be considered which utilize simple analytical formulae to provide an approximate estimate of the inductance based on the wire width and certain characteristics of the power distribution network.[11]

3. Summary

Two characteristics of on-chip inductances have been discussed in this paper that can be exploited to significantly simplify the extraction of on-chip inductance. The first characteristic is that the sensitivity of a signal waveform to errors in the inductance values is low, particularly the propagation delay and the rise time. It is quantitatively shown in this paper that the error in the propagation delay and rise time is below 9.4% and 5.9%, respectively, assuming a 30% relative error in the extracted inductance. If an *RC* model is used for the same example, the corresponding errors are 51% and 71%, respectively. The second characteristic is that the value of the on-chip inductance is a slow varying function of the width of the wire and the geometry of the surrounding wires. These two characteristics can be exploited by using simplified techniques to generate approximate inductance values with high computational efficiency. A trivial method such as using a constant value of average inductance per unit length has also been shown to significantly improve the accuracy of the propagation delay and the rise time as compared to using an *RC* model. Thus, one solution when extracting on-chip inductance is to trade off accuracy for computational efficiency and use a simple estimation of the on-chip inductance.

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