On-Chip Test Circuit for Measuring Substrate and Line-to-Line Coupling Noise

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***Abstract*—An on-chip test circuit has been developed to directly measure substrate and line-to-line coupling noise. This test circuit has been manufactured in a 0.35 μm double-well double polysilicon CMOS process and consists of noise generators and switched-capacitor signal processing circuitry. On-chip analog-to-digital conversion and calibration are used to eliminate off-chip noise and to extend the measurement accuracy by removing system noise. A scan circuit is described that enables the noise waveform to be reconstructed. On-chip generators ranging in area from 0.25 μm^2 to 1.5 μm^2 produce noise at the receiver decreasing from 3.14 mV/μm to 0.73 mV/μm. Open and closed guard rings reduce the noise by 20% and 85%, respectively. Measurement of test circuits manufactured with an epitaxial process—5.5-μm-thick epitaxy with 20 Ω·cm resistivity on top of a 120 μm bulk with 0.03 Ω·cm—exhibits a frequency limit of 50 MHz below which coupling is insensitive to substrate noise. The difference between experimental results and an analytic model of the line-to-line coupling capacitance ranges from 8.5% to 17.7% for different metal layers.**

***Index Terms*—CMOS switched-capacitor circuit, coupling, noise, on-chip measurement.**

I. INTRODUCTION

COMPLEX high-speed digital circuits together with high performance analog circuits are commonly integrated onto the same substrate. In such mixed-signal systems, fast switching transients produced by digital circuits can couple into sensitive analog components through both the substrate and line-to-line capacitances, thereby limiting the achievable analog precision. Furthermore, performance degradation caused by substrate and capacitive coupling noise is difficult to control and even more difficult to predict. The requirement for highly accurate noise measurement to identify and manage noise has therefore become increasingly evident.

In order to evaluate substrate noise, on-chip test circuits are required to accurately and efficiently measure substrate current [1]–[10]. These measurements, however, are based on simple single MOS transistor test structures [5], [7], voltage comparator structures [3], [4], or single-stage MOS differential amplifier structures [6]. Due to the analog output signals, a common problem in these measurements is the difficulty of acquiring output signals without other noise signals becoming mixed in the measured signal. The external circuitry and parasitic impedances affect the analog output signal, severely decreasing the measurement accuracy. The accuracy of these test structures is therefore usually quite poor.

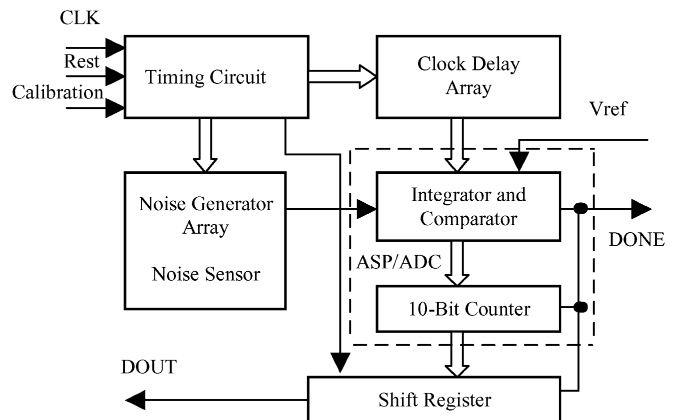

Fig. 1. Block diagram of the noise coupling test circuit.

Four different test circuits have been fabricated: two substrate coupling noise test circuits and two capacitive interconnect coupling noise test circuits. The substrate coupling noise test circuit is used to measure the substrate coupling noise generated from a substrate noise generator array where each individual substrate noise generator is of different size and distance to the noise receiver. The second substrate noise test circuit is used to evaluate the reduction in substrate coupling noise due to guard rings. Noise generators are placed outside each guard ring so that the effect of the reduction in substrate noise due to each guard ring can be measured and evaluated. The capacitive coupling test circuits measure line-to-line capacitive coupling noise and capacitance.

This paper is organized as follows. The substrate noise measurement technique is described in Section II. In Section III, experimental data from the substrate coupling noise test circuitry is presented and discussed. The test results describing the reduction in substrate noise due to the guard lines and rings are evaluated in Section IV. The on-chip line-to-line capacitive coupling test technique and related test results are presented and compared to an analytic model of the line-to-line coupling capacitance in Section V. Finally, some conclusions are provided in Section VI.

II. ON-CHIP SUBSTRATE COUPLING NOISE TEST TECHNIQUE

A specialized on-chip test circuit has been developed to directly measure substrate coupling noise. The test circuit utilizes differential switched-capacitor circuits with digital outputs. The test circuit has an input pin to enable on-chip system calibration to remove existing system noise. The circuit

Manuscript received November 3, 2004; revised June 4, 2005.
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Digital Object Identifier 10.1109/JSSC.2005.862349

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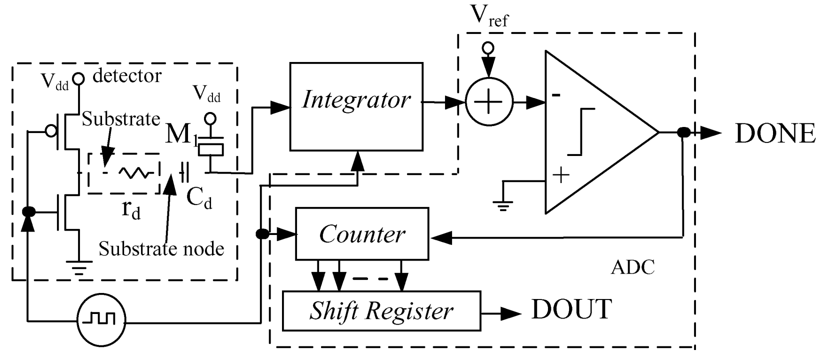

Fig. 2. Principle of the on-chip noise generating/sensing and analog-to-digital conversion.

consists of a noise generator array, an analog signal processing (ASP)/analog-to-digital converter (ADC) block, a clock delay array, and a timing circuit, as shown in Fig. 1. The clock delay array generates 32 different delayed clocks to operate the ASP/ADC block such that the noise waveform can be reconstructed from 32 points that make up a substrate noise waveform. The delay time is set from 0 to 31 ns with a 1-ns step size. Details of the test circuit are presented in the following subsections.

The substrate noise is generated by an array of noise generators, each of different size and placed at different distances from each noise receiver. A decoder is used to control the noise generator array such that only one noise generator switches at any one time. The substrate coupling noise is sensed by the receiver and passed to the input of the integrator where the sensed noise voltage is amplified and integrated. The integrated coupling noise is converted to a digital signal by an on-chip ADC consisting of a 1-bit differential comparator and a 10-bit counter. The integrated coupling noise is applied to the inputs of the comparator and compared to the reference voltages at each clock cycle as shown in Fig. 2.

A. Sampling the Substrate Noise

The circuit described in this paper samples the substrate noise voltage at the rising edge of clock ϕ_1, which operates the ASP/ADC blocks. Individual points on the substrate noise voltage waveform are individually tested by changing the rising edge of the ASP/ADC clock ϕ_1 relative to the noise generating clock CLK. The clock delay circuit is composed of a series of small inverters controlled by a multiplexer. Depending upon the input code, different delay times between clocks CLK and ϕ_1 are generated by the clock delay array. As shown in Fig. 3, the clock delay circuit is composed of 32 delay cells with each cell composed of two small inverters and a decoder. Each delay cell generates a 1-ns delay from the input clock to the ASP/ADC.

The clock waveforms are schematically shown in Fig. 4. At the falling edge of the clock CLK, substrate voltage spikes are generated by the noise generator. Negative voltage spikes are also generated at the rising edges of CLK. This proposed substrate voltage waveform test circuit only samples and integrates the positive spikes. Integrating both spikes would yield a zero voltage due to cancellation of the positive and negative spikes.

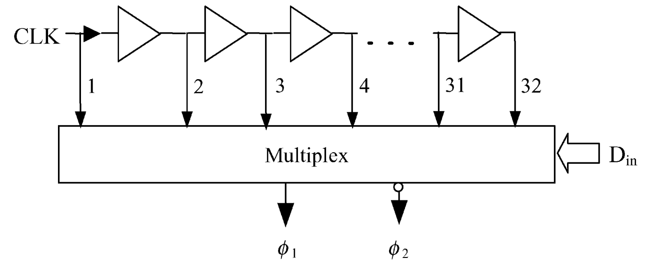

Fig. 3. Circuit diagram of the clock delay array block.

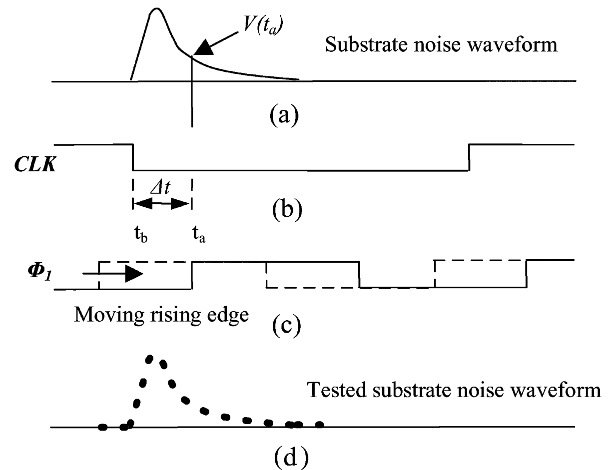

Fig. 4. Waveforms of proposed substrate noise test circuit: (a) the substrate noise voltage; (b) the clock applied to the noise generator; (c) the sampling clock; and (d) the substrate noise waveform.

By delaying clocks ϕ_1 and ϕ_2 by a time Δt from the noise generating clock CLK (see Fig. 4), the substrate noise voltage $V(t_a)$ at time t_a is sampled and integrated.

When CLK is applied to the substrate noise generator/sensor block, a current is injected into the substrate, producing a fluctuation in the substrate voltage during the falling and rising edges of CLK. This substrate voltage is passed to the substrate noise signal processing/analog-to-digital conversion circuit where the raw substrate noise voltage digital codes are generated. Scanning the sampling clock ring edge from left to right across the falling edge of the clock permits the measurement of a number of points representing the substrate voltage waveform.

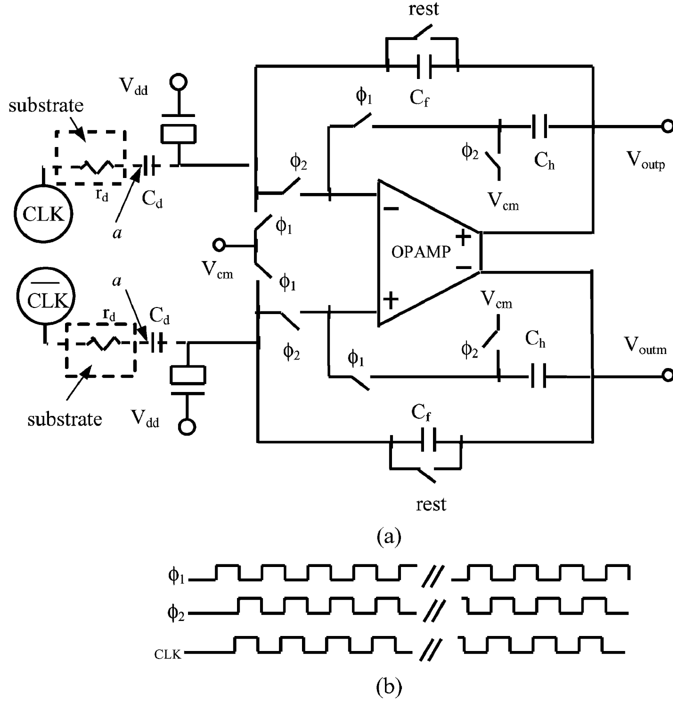

Fig. 5. Substrate coupling voltage integrator circuit. (a) Schematic. (b) Clock waveforms.

B. Integration of the Substrate Noise

A schematic of the substrate coupling noise integrator circuit is shown in Fig. 5. The integrator is a fully symmetric differential switched capacitor circuit. The common-mode noise (such as noise from the power supply, ground, and the reference voltage $V_{\rm cm}$) is removed or reduced by the differential circuit architecture. There is noise, however, caused by clock feedthrough from the switches, OPAMP offset, mismatch of the two differential paths, and other forms of random noise. Other noise sources such as $1/f$ noise, thermal noise, and *kT/C* noise may also exist in the integrator output analog voltage signal. In order to achieve accurate results, these noise sources must be removed from the integrator output. An on-chip calibration process is used in this test circuit to remove the integrator offset voltage and other noise voltages.

When clock ϕ_1 is "high," capacitor C_f is charged to $V_o[n-1]+\Delta V_{\rm cm}$ and the two capacitors C_h hold the previous output voltages $V_{\rm outm}[n-1]$ and $V_{\rm outp}[n-1]$. Capacitor C_d is charged to $V_{\rm in}[n]-V_{\rm cm}$. When clock ϕ_2 is high and ϕ_1 low, charge stored on capacitors C_d and C_f are re-distributed to C_f and C_d. To ensure the integrator operates properly, the substrate noise voltage needs to be settled before ϕ_2 goes "high." The clock frequency of ϕ_1 and ϕ_2 is required to be low. Applying the law of conservation of charge to the OPAMP inputs, the output differential voltage is

$$\Delta V_o[n]=\frac{C_d}{C_f}\Delta V_{\rm in}[n]+\Delta V_o[n-1]-\frac{C_d}{C_f}\Delta_{\rm sys}+\delta[n] \quad (1)$$

where $\Delta V_{\rm in}[n]$ is the differential voltage at the sensor input nodes a during ϕ_1, $\Delta V_o[n]$ is the differential voltage at the integrator outputs during ϕ_2, C_d is the sensing capacitance, C_f is the feedback capacitance in the integrator, and $\Delta_{\rm sys}$ is the differential system offset voltage. δ is the lumped noise voltage during each integration cycle.

After N clock cycles, the differential voltage at the integrator output is

$$\Delta V_o[N]=\frac{C_d}{C_f}\sum_{k=1}^{N}\Delta V_{\rm in}[k]-\frac{NC_d}{C_f}\Delta_{\rm sys}+\sum_{k=1}^{N}\delta[k] \quad (2)$$

where N is the total number of clock cycles during the integration or the raw test data.

The first term in (2) is the substrate noise component after N clock pulses. The remaining terms are noise components unrelated to substrate coupling. For every clock cycle, the voltage $V_{\rm in}[k]$ is the same and equal to $V_{\rm noise}$. At the end of the integration, the integrator output is equal to the reference voltage $V_{\rm ref}$. The comparator output changes and both the counter and the integrator are terminated. The measured substrate coupling noise raw code is generated at the counter output. The substrate coupling noise per switching event can be obtained from the raw code by

$$V_{\rm noise}=\frac{C_f}{C_d}\cdot\frac{V_{\rm ref}}{N}-\left(\Delta_{\rm sys}+\frac{C_f}{C_d}\cdot\frac{\Delta_{\rm comp}}{N}\right)-\frac{C_f}{C_d}\cdot\frac{\sum_{k=1}^{N}\delta[k]}{N} \quad (3)$$

where $\Delta_{\rm comp}$ is the comparator offset voltage and $V_{\rm noise}$ is the raw data of the measured substrate noise. The error of the measured data is

$$\text{error}=-\left(\Delta_{\rm sys}+\frac{C_f}{C_d}\cdot\frac{\Delta_{\rm comp}}{N}\right)-\frac{C_f}{C_d}\cdot\frac{\sum_{k=1}^{N}\delta[k]}{N} \quad (4)$$

where this error needs to be removed (or minimized).

C. Circuit Calibration

The operation of the calibration process proceeds as follow: a power supply voltage is applied at the input of the noise generator inverter during the calibration period and the circuit is operated as shown in Fig. 2. The input voltage $V_{\rm in}[k]$ at the sensor input node a is zero. Another digital code N_c is generated at the end of the calibration process. The new digital code is called the error (including the amplifier offset voltage error) calibration code. From (2), the total noise voltage after N_c clock cycles is

$$\Delta V_o[N_c]=\Delta V_{\rm ref}=-\frac{N_cC_d}{C_f}\cdot\Delta_{\rm sys}-\Delta_{\rm comp}+\sum_{k=1}^{N_c}\delta[k] \quad (5)$$

where N_c is the decimal value of the calibration code, and $\Delta V_{\rm ref}$ is the reference differential DC voltage.

From (3) and (5), the calibrated substrate coupling noise per switching event is

$$\begin{aligned}\Delta V_{\rm noise}=&\frac{C_f}{C_d}\cdot\left(\frac{1}{N}-\frac{1}{N_c}\right)\cdot\Delta V_{\rm ref}\\&+\frac{C_f}{C_d}\cdot\left(\frac{1}{N}-\frac{1}{N_c}\right)\cdot\Delta_{\rm comp}\\&+\frac{C_f}{C_d}\cdot\left(\frac{\sum_{k=1}^{N}\delta[k]}{N}-\frac{\sum_{k=1}^{N_c}\delta[k]}{N_c}\right)\end{aligned} \quad (6)$$

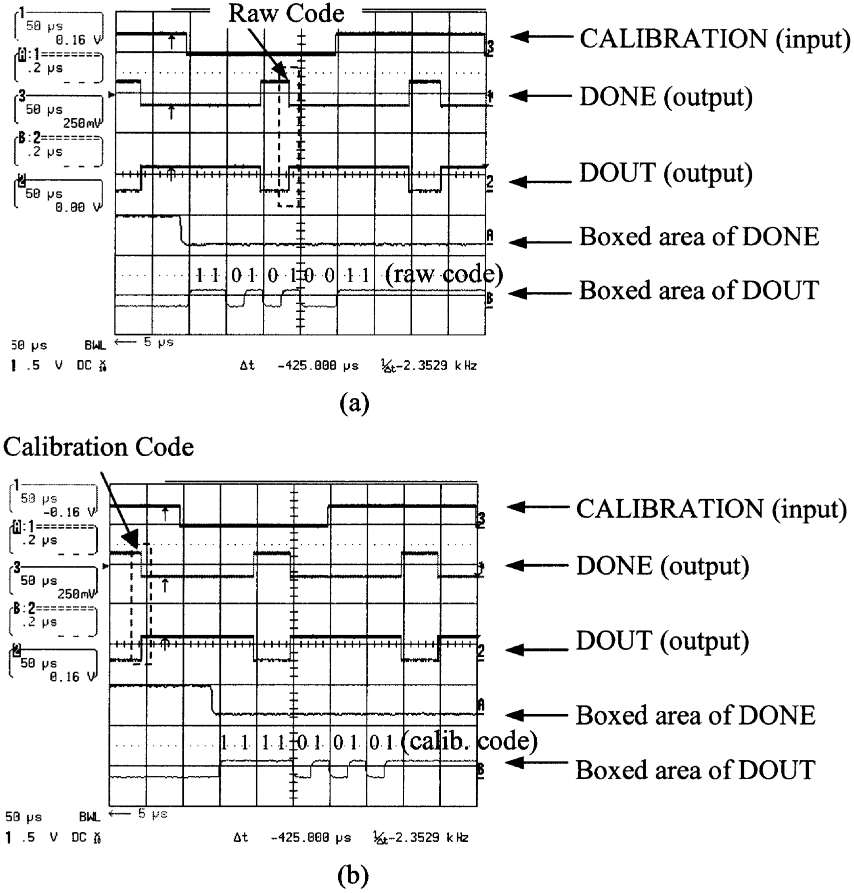

Fig. 6. Measured output waveforms of the substrate coupling noise test circuit. (a) Raw data measurement when input CALIBRATION is "low." (b) Calibration data measurement when input CALIBRATION is "high."

where $\Delta V_{\rm noise}$ is the calibrated substrate noise voltage. The measurement error after calibration is

$$V_{\rm error} = \frac{C_f}{C_d} \cdot \left(\frac{1}{N} - \frac{1}{N_c}\right) \cdot \Delta_{\rm comp} + \frac{C_f}{C_d} \cdot \left(\frac{\sum_{k=1}^{N} \delta[k]}{N} - \frac{\sum_{k=1}^{N_c} \delta[k]}{N_c}\right) \qquad (7)$$

where $V_{\rm error}$ is the measurement error, C_d is the sensing capacitance, C_f is the feedback capacitance in the integrator, $\Delta_{\rm comp}$ is the comparator offset voltage, δ is the lumped noise voltage during each integration cycle, N is the decimal value of the raw test code, N_c is the decimal value of the calibration code, and $\Delta V_{\rm ref}$ is the reference differential DC voltage. The noise in the reference voltage is the only source of error in the measured result.

Once the integrated coupling noise reaches the reference voltage, the comparator output flags the output pin (DONE, shown in Figs. 1 and 6) to indicate the completion of the measurement process, terminating the counter and integrator. The counter numerates the number of clock cycles during the integration period and the system uses the counted value as raw test data. At the end of each measurement, the value stored in the 10-bit counter is moved in parallel to a shift register from where the test data is shifted out (through the DOUT pin shown in Fig. 6).

The system noise in the measured data is removed by an on-chip calibration process. During the calibration process, the noise generators are maintained inactive such that only the system noise is integrated and compared to the reference voltages. A digital code is generated at the end of the calibration process and used to calibrate the raw test data. Each measurement generates two 10-bit digital codes, the raw data code and the calibration code. The peak-to-peak substrate noise voltage is determined from the integrator gain, reference voltages, and the decimal value of the two digital codes. One pair of the measured substrate raw and calibration codes is imported from the digital oscilloscope and is shown in Fig. 6.

The waveforms shown in Fig. 6(a) depict the raw data measurement and the waveforms illustrated in Fig. 6(b) display the calibration test data. Five waveforms are shown in each imported screen. The upper waveform depicts the input calibration waveform, indicating whether the calibration test is "High." Below the calibration waveform is the single bit output indicating the completion of the measurement when the signal changes from "High" to "Low." Below the DONE waveform is the digital output signal DOUT. Greater resolution of the test results, the zoomed areas of waveform DOUT, is shown at the bottom of Fig. 6.

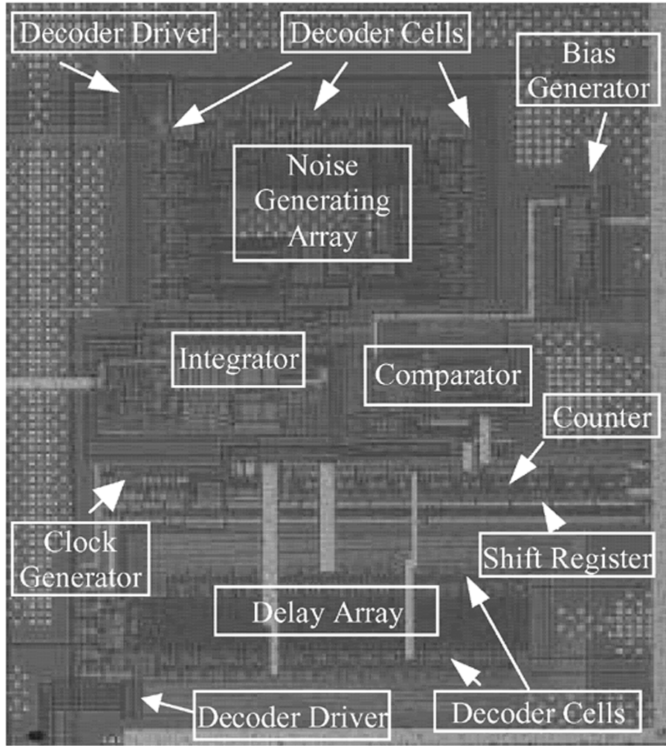

Fig. 7. Microphotograph of the substrate coupling test circuit.

D. Accuracy and Error Analysis

The system offset voltage is completely removed after the calibration process [see (7)]. The test error due to the comparator offset voltages is reduced by $C_f N_c N / C_d (N_c - N)$ and is negligible. However, due to the randomness of the many noise sources such as power/ground noise, $1/f$ noise, and thermal noise at the integrator output, the noise can only be completely removed if N and $N_c \to \infty$. The remaining error in the measured substrate noise voltage after the calibration process is

$$\Delta V_n = \frac{C_f}{C_d} \cdot \left(\frac{\sum_{k=1}^{N} \delta[k]}{N} - \sum_{k=1}^{N_c} \zeta[k] N_c \right) \qquad (8)$$

where δ_k is the noise voltage per clock cycle during sampling and ς_k is the noise voltage per clock cycle generated during the calibration process.

Based on this analysis, a smaller measurement error is achieved if the reference voltage is large (large N). Since the substrate coupling noise voltage is usually small, in order to efficiently sense the substrate voltage (providing good sensitivity), the sensing capacitance cannot be excessively small. Increasing the size of the sensing transistor M_1 also reduces the error in C_d due to process variations which improves the linearity of C_d. An effective strategy to increase the measurement accuracy is to maintain a large reference voltage V_{ref} and feedback capacitor C_f.

A microphotograph of the substrate coupling noise test circuit is shown in Fig. 7, where the primary blocks in the test circuit are individually labeled. A 5-bit decoder is placed around the noise generators in the noise generator array block, as shown in Fig. 7. Two identical mirrored noise generator arrays, with an opposite clock phase, are placed next to each other to support the differential operation. A 6-bit decoder is laid out around the delay array. Drivers are placed in front of the decoder inputs to drive the long buses. The power supply and ground buses of the analog and digital circuit are physically separate.

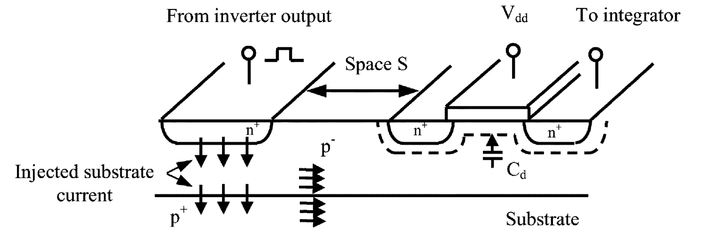

Fig. 8. Operation of the substrate coupling noise generator/receiver pair.

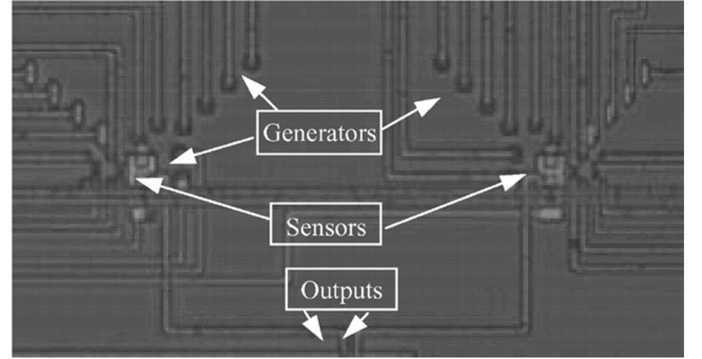

Fig. 9. A closer look at the noise generator array.

The noise receiver is an MOS gate capacitor formed by applying the power supply voltage V_{dd} on the gate of an NMOS transistor and connecting the source/drain (S/D) of the transistor as the input to the integrator circuit. The noise generator is an N^+ region, similar to the S/D of an NMOS transistor, with a specific size and distance from the receiver. A current is injected into the substrate from this N^+ region when a clock signal is applied. The principle of the substrate coupling noise generator/receiver pair is illustrated in Fig. 8. A microphotograph of the noise generator/sensor is shown in Fig. 9. The noise generator size ranges from 0.25 to 2 $\mu\mathrm{m}^2$ and the distance to the noise receiver ranges from 1 to 20 μm.

III. Experimental Data From the Substrate Coupling Noise Test Circuit

The measured test circuits have been packaged in an 84 pin ceramic pin grid array (CPGA) package. The circuit uses 36 of the 84 total pins. Improved ground connection has been achieved by using Ni/Au backside plating on both the package and wafer. A test printed circuit board was used during the test. Reference voltages, scanning codes, and noise generator selection codes are generated on the test printed circuit board. Each of the 21 noise generators on the substrate noise test circuit have been evaluated, producing 32 different points on the substrate coupling noise waveforms for each noise generator. The substrate coupling noise voltage waveforms are reconstructed from these test data points. The test results of each of the 21 noise generators in the substrate noise generator array are summarized in Figs. 11 and 12. The results show that

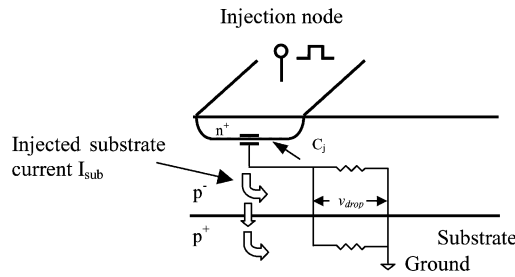

Fig. 10. The effect of feedback on the PN junction capacitance due to the voltage drop caused by the substrate resistance.

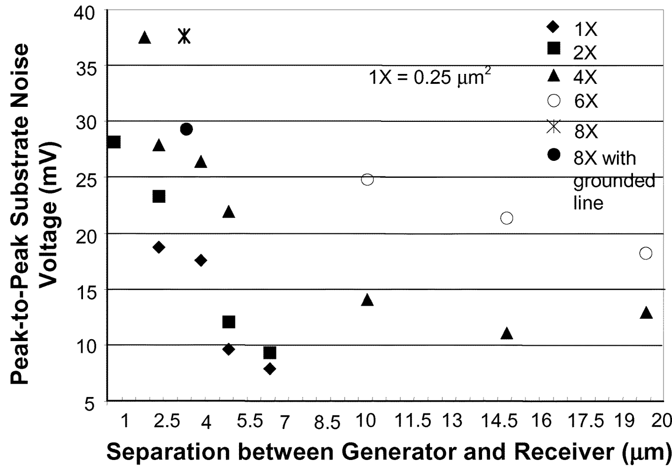

Fig. 11. Measured substrate coupling noise voltage as a function of the noise generator size and distance from the noise receiver.

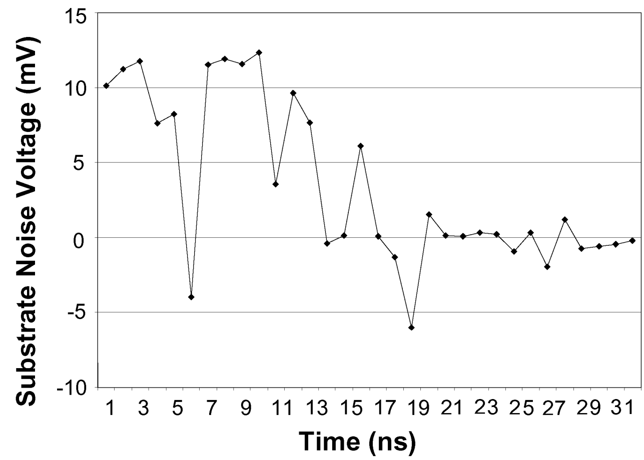

Fig. 12. Reconstructed substrate noise waveform determined from 32 test points.

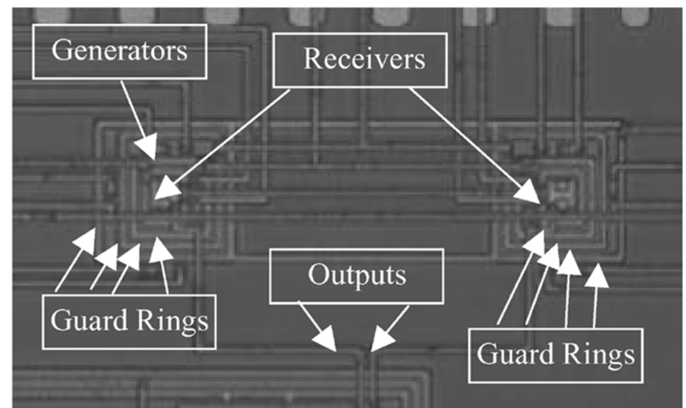

Fig. 13. Microphotograph of the circuit structures for evaluating the reduction in noise caused by the guard rings.

the substrate coupling voltage is proportional (but not linear) to the size of the noise generator. At 2.5 μm from the noise generators, the measured substrate coupling noise voltages are 18.2, 23.45, and 27.89 mV for noise generators of size 0.25, 0.5, and 1 μm^2, respectively. Due to the effect of feedback on the substrate current, the injected substrate current from a larger noise generator can travel farther within the substrate. The feedback effect is strongly dependent upon the density of the injected substrate current. The substrate current is injected through two different regions of the PN junction capacitor in the edge and flat part areas. The current injected through the PN junction edge capacitance has a larger density and therefore produces a stronger feedback effect on the substrate voltage. The larger noise generator has a relatively smaller portion of the edge capacitance, producing a weaker feedback effect such that the substrate noise can travel farther in the space domain.

The measurement data also show that the substrate coupling noise voltages decrease exponentially with time as the signal propagates within the substrate. The noise signal, however, attenuates at a different rate for different noise generator sizes in the time domain. The substrate coupling noise generated from large noise generators attenuates slowly as compared to smaller size noise generators, partially due to the effect of feedback on the voltage of the substrate current injecting PN junction [12]. The injected current produces a voltage drop between the injection node and ground due to the substrate resistance. This voltage drop due to the substrate resistance reduces the voltage across the PN junction, causing an increase in the PN junction capacitance as shown in Fig. 10. Additional current is therefore injected into the substrate due to this feedback effect, causing the noise signal to attenuate more slowly.

For noise generators of size 0.25, 0.5, 1, and 1.5 μm^2, the peak-to-peak substrate noise voltage decreases as a function of distance and, for this substrate, is 3.14, 3.08, 1.98, and 0.73 mV/μm, respectively (see Fig. 11). A substrate coupling noise waveform reconstructed from the 32-point measurement is shown in Fig. 12. The substrate noise generator requires an area of 1×1 μm^2 and is placed 5 μm from the receiver. The test results illustrate the peak-to-peak substrate coupling noise voltage produced by the noise generator, approximately 15 mV for this 0.35 μm CMOS p^-/p^+ substrate process. The epi-layer is 5.5 μm thick and has a resistivity ρ of 20 Ω·cm. The heavily doped p^+ substrate has a thickness of 120 μm and a resistivity of 0.03 Ω·cm. Note that the substrate coupling noise waveform attenuates quickly and diminishes in about 20 ns. This result indicates that the substrate noise voltage reduces to zero (or close to zero) in about 20 ns (equal to 50 MHz) for the specific substrate of the test circuit. For sampled-data systems, the substrate noise will not affect analog circuits operating at frequencies lower than 50 MHz (for this particular substrate). In general, for a certain type of substrate, a frequency boundary

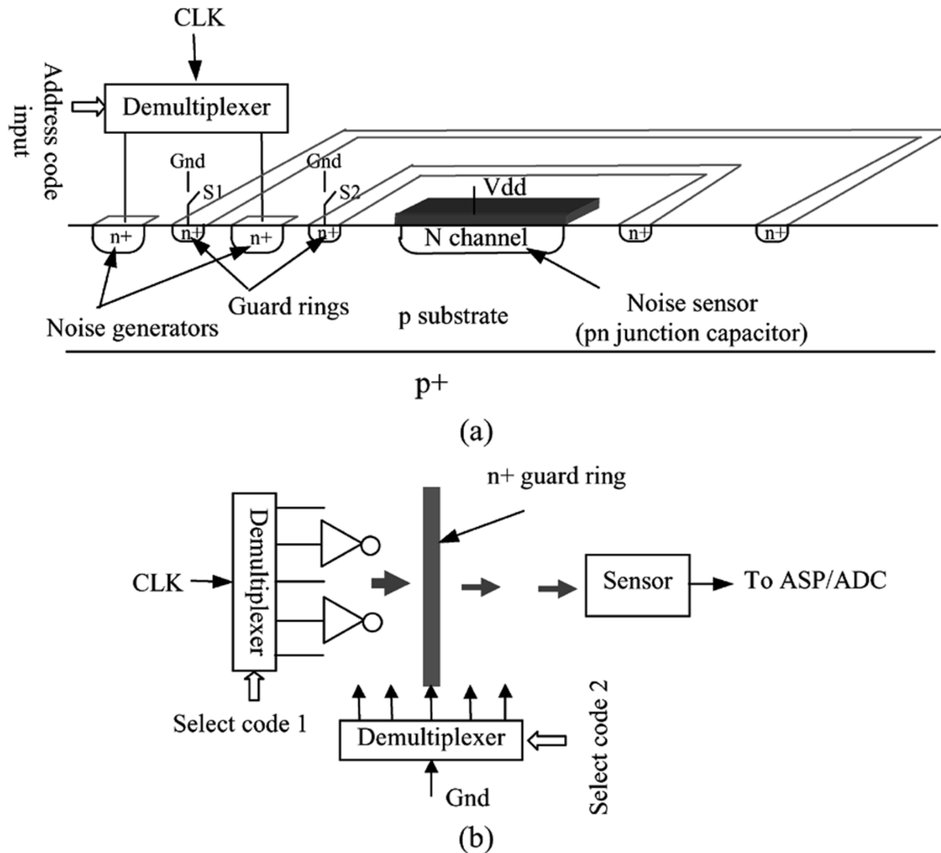

Fig. 14. Test structures for measuring substrate guard rings. (a) Cross sectional view of the guard rings. (b) Schematic representation.

exists that makes on-chip circuits operating within this frequency limit insensitive to substrate coupling noise.

IV. Substrate Coupling Noise Reduction Due to Guard Lines and Rings

The noise generator array also includes a noise generator with an N^+ grounded line (also called a guard band) to separate the noise source from the noise receiver. The test results demonstrate that the guard line has only a limited effect on reducing the substrate noise. As compared to the noise generator without a guard line, less than a 20% reduction in noise is measured for this N^+ grounded line test structure.

Four guard rings have been included on the test circuit. Two noise generators are placed outside each guard ring. Eight structures have been developed for evaluating the reduction in substrate noise due to these guard rings. The guard rings are single 1.8-μm-wide closed grounded N^+ rings as shown in Fig. 13, and a cross-sectional view is shown in Fig. 14. During each measurement, only one guard ring is connected to the analog ground (which is shared with other on-chip analog circuits) to avoid noise coupling caused by the digital circuitry, while the other guard rings are maintained floating. The substrate noise voltages induced by the noise generators placed at different distances to the noise sensors are measured with one substrate guard ring between the noise generator and receiver (which is connected to ground).

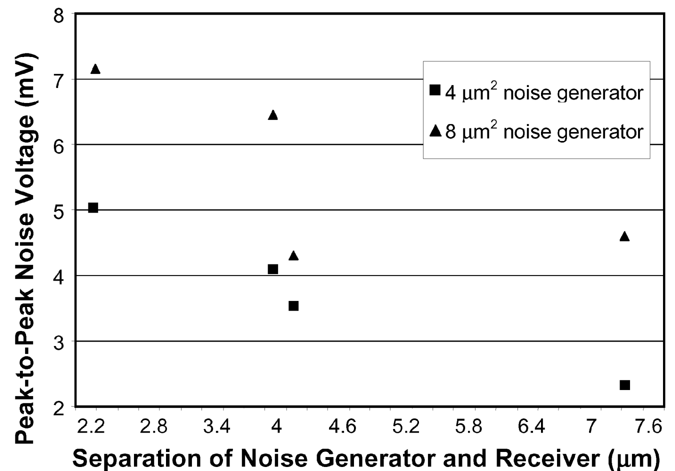

Fig. 15. Measured reduction in substrate noise with guard rings.

The measured results are displayed in Fig. 15. As compared with the measured results shown in Fig. 11, the substrate noise voltage coupled to the receiver is about six to eight times smaller than the noise voltage coupled to those receivers not surrounded by guard rings. Significant substrate coupling noise (as large as 7 mV as shown in Fig. 15), however, is measured for a receiver with a single closed grounded N^+ guard ring. The reduction in noise for a single guard ring is approximately 85% (by comparing test data in Figs. 11 and 15). This measurement demonstrates that double or triple guard ring structures are required to efficiently reduce substrate coupling noise. In the measurement,

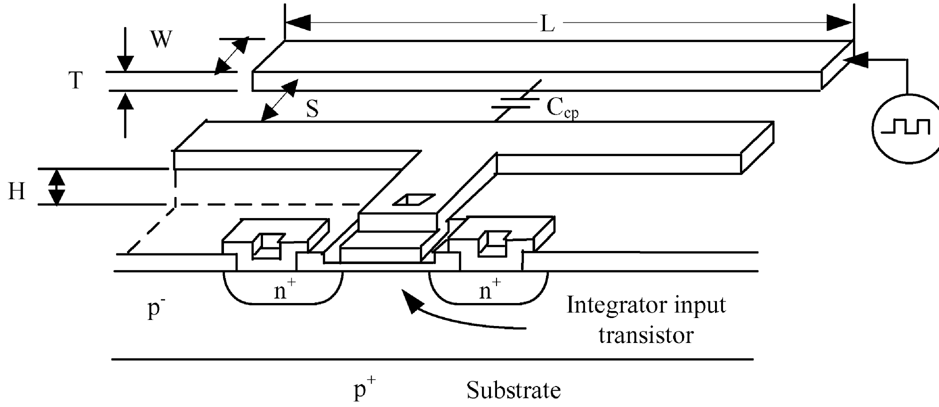

Fig. 16. Test structure for sensing line-to-line capacitive coupling noise voltage.

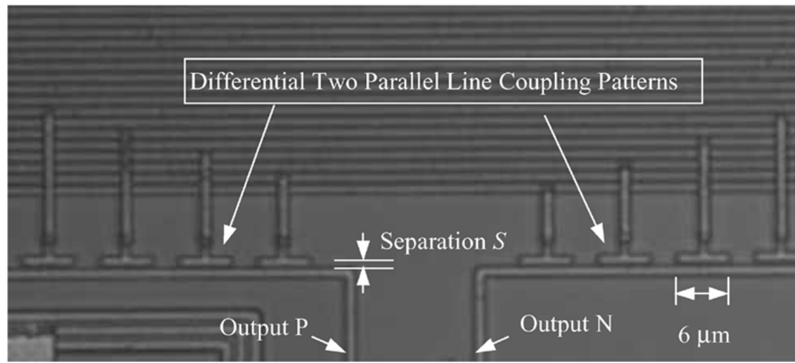

Fig. 17. Microphotograph of capacitive coupling circuit structures.

the distance between the noise generator and noise receiver is shown to not influence the efficiency of the guard rings.

V. Line-to-Line Capacitive Coupling Measurement Results

Line-to-line capacitive coupling has also been evaluated based on the same signal processing circuitry but with different coupling structures as illustrated in Figs. 16 and 17. In these test structures, all of the lines are 6 μm long and 0.7 μm in width. The coupling voltage between two lines on the same layer is measured from the digital output code pair (raw and calibration codes). An estimate of the coupling capacitance can also be obtained from

$$C_{\text{coupling}} = \left(\frac{1}{N} - \frac{1}{N_C}\right) \cdot \frac{V_{\text{ref}}}{V_{\text{dd}}} \cdot C_f \tag{9}$$

where N is the decimal value of the raw substrate coupling noise code, N_c is the decimal value of the calibration code, C_f is the feedback capacitance in the integrator circuit, V_{ref} is a DC reference voltage, and V_{dd} is the power supply voltage.

The line-to-line coupling capacitance for three different metal layers is measured and compared to those values determined from the Sakurai and Tamaru model [11] and shown in Fig. 18. The difference between the experimental and analytic capacitances is 8.5%, 12.6%, and 17.7% for metal 1, metal 2, and metal 3, respectively. The error is due to the assumption that the length of a line in the Sakurai and Tamaru model is considered to be infinite. In deep-submicrometer ICs, however, coupling between short lines can no longer be ignored. The unit capacitance for short lines can also not be considered as constant due to edge effects [13]. Note that in other line-to-line capacitive coupling models, Chang [14], Elmasry [15], Mejis and Fokkema [16], and Yuan and Trick [17], the edge effect is also not considered. The line-to-line capacitive coupling test technique presented in this paper can be useful for measuring and modeling the coupling capacitance between short lines in deep-submicrometer ICs.

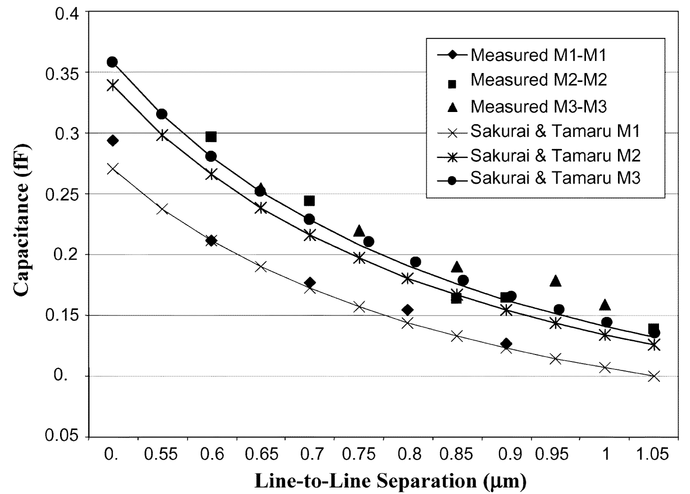

Fig. 18. Comparison of measured and analytic line-to-line coupling capacitance.

VI. Conclusions

A specialized test circuit has been developed to directly measure substrate and line coupling noise, which consists of noise generators and signal processing circuitry. On-chip ADC and calibration are used to eliminate off-chip noise and to extend the measurement accuracy. A scan circuit is described that enables reconstruction of the noise waveform. Based on test data, noise generators of size 0.25, 0.5, 1, and 1.5 μm^2 produce peak-to-peak substrate noise voltages that decrease as a function of distance and are 3.14, 3.08, 1.98, and 0.73 mV/μm, respectively, for a standard CMOS substrate. Open and closed guard rings are shown to reduce substrate noise by 20% and 85%, respectively. For a certain type of substrate, a frequency boundary exists that makes on-chip circuits operating within this frequency limit insensitive to substrate coupling noise. The difference between experimental and analytic models of the line-to-line coupling capacitance ranges from 8.5% to 17.7% for different metal layers.

References

[1] R. B. Merrill, W. M. Young, and K. Brehmer, "Effect of substrate material on crosstalk in mixed analog/digital integrated circuits," in *Int. Electron Devices Meeting (IEDM) Tech. Dig.*, Dec. 1994, pp. 433–437.

[2] R. M. Secareanu, S. Warner, S. Seabridge, C. Burke, T. Watrobski, C. Morton, W. Staub, T. Tellier, and E. G. Friedman, "Placement of substrate contacts to minimize substrate noise in mixed-signal integrated circuits," *Analog Integrat. Circuits Signal Process.*, vol. 28, no. 3, pp. 253–264, Sep. 2001.

[3] K. Makie-Fukuda, T. Ando, T. Tsukada, T. Matsura, and M. Hotta, "Voltage comparator based measurements of equivalently sampled substrate noise waveforms in mixed-signal integrated circuits," *IEEE J. Solid-State Circuits*, vol. 31, no. 5, pp. 726–731, May 1996.

[4] M. Nagata, Y. Kashima, D. Tamura, T. Morie, and A. Iwata, "Measurements and analysis of substrate noise waveform in mixed-signal IC environment," in *Proc. IEEE Custom Integrated Circuits Conf.*, May 1999, pp. 575–578.

[5] D. K. Su, M. J. Loinaz, S. Masui, and B. A. Wooly, "Experimental results and modeling techniques for substrate noise in mixed-signal integrated circuits," *IEEE J. Solid-State Circuits*, vol. 28, no. 4, pp. 420–430, Apr. 1993.

[6] M. Van Heilningen, J. Copiet, P. Wambacq, S. Donnay, M. Gngels, and I. Bolsens, "Analysis and experimental verification of digital substrate noise generation for epi-type substrates," *IEEE J. Solid-State Circuits*, vol. 35, no. 7, pp. 1002–1008, Jul. 2000.

[7] S. Masui, "Simulation of substrate coupling in mixed-signal MOS circuits," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 1992, pp. 42–43.

[8] T. Blalack, J. Lau, F. J. R. Clément, and B. A. Wooley, "Experimental results and modeling of noise coupling in a lightly doped substrate," in *Int. Electron Devices Meeting (IEDM) Tech. Dig.*, Dec. 1996, pp. 23.3.1–23.3.4.

[9] T. Blalack, "Design techniques to reduce substrate noise," in *Analog Circuit Design: Volt Electronics; Mixed-Mode Systems; Low-Noise and RF Amplifiers for Telecommunication*, J. Huijsing, R. v. d. Plassche, and W. Sansen, Eds. Boston, MA: Kluwer Academic, 1999, pp. 193–218.

[10] T. Schmerbeck, "Noise coupling in mixed-signal ASICs," in *Low-Power HF Microelectronics: A Unified Approach*, G. Machado, Ed. London, U.K.: IEE, 1996, vol. 8, pp. 373–430. Circuits and Systems Series.

[11] T. Sakurai and K. Tamaru, "Simple formula for two- and three-dimensional capacitance," *IEEE Trans. Electron Devices*, vol. ED-30, no. 2, pp. 183–185, Feb. 1983.

[12] R. M. Secareanu, S. Warner, S. Seabridge, C. Burke, J. Becerra, T. E. Watrobski, C. Morton, W. Staub, T. Tellier, I. S. Kourtev, and E. G. Friedman, "Substrate coupling in digital circuits in mixed-signal smart-power systems," *IEEE Trans. Very Large Scale Integrat. (VLSI) Syst.*, vol. 12, no. 1, pp. 67–78, Jan. 2004.

[13] C. T. A. Johnk, *Engineering Electromagnetic Fields and Waves*. New York: Wiley, 1988.

[14] W. H. Chang, "Analytic IC-metal-line capacitance formulas," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-24, no. 9, pp. 608–611, Sep. 1976.

[15] M. I. Elmasry, "Capacitance calculation in MOSFET VLSI," *Electron Device Lett.*, vol. EDL-3, no. 1, pp. 6–7, Jan. 1981.

[16] N. V. D. Meijs and J. T. Fokkema, "VLSI circuit reconstruction from mask topology," *Integration*, vol. 2, no. 2, pp. 85–119, 1984.

[17] C. P. Yuan and T. N. Trick, "A simple formula for the estimation of the capacitance of two dimension interconnects in VLSI circuits," *Electron Device Lett.*, vol. EDL-3, no. 1, pp. 391–393, Dec. 1982.

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