# Power Noise in TSV-Based 3-D Integrated Circuits

Ioannis Savidis, *Student Member, IEEE*, Selcuk Kose, *Member, IEEE*, and Eby G. Friedman, *Fellow, IEEE*

***Abstract*—A three-dimensional (3-D) test circuit examining power grid noise in a 3-D integrated stack has been designed, fabricated, and tested. Fabrication and vertical bonding were performed by MIT Lincoln Laboratory for a 150 nm, three metal layer SOI process. Three wafers are vertically bonded to form a 3-D stack. Noise analysis of three power delivery topologies is described. Calibration circuits for a source follower sense circuit compare the different power delivery topologies as well as the separate 3-D stacked circuits. The effect of the through silicon via (TSV) density on the noise profile of a 3-D power delivery network is experimentally described. A comparison of the peak noise for each topology with and without board level decoupling capacitors, and resonant behavior is provided, and suggestions for enhancing the design of a 3-D power delivery network are offered.**

***Index Terms*—Noise propagation, 3-D power distribution, 3-D power network, topology specific noise.**

## I. Introduction

A TECHNOLOGICAL push, due to the proliferation of wireless devices, has accelerated the need to find alternative technologies that increase device density, merge disparate technologies, while reducing the power budget. 3-D integration has emerged as a potential solution that supports mixed-signal systems without the need for greater process complexity. A critical component of 3-D systems, which is experimentally explored in this paper, is delivering power to multiple device planes [1].

An important issue for 3-D integrated circuits (ICs) is the design of a robust power distribution network that can provide sufficient current to every load within a system. In planar ICs where flip-chip packaging is adopted as the packaging technique, an array of power and ground pads is allocated throughout the integrated circuit. Increasing current densities and faster current transients, however, complicate the power distribution design process. Three-dimensional integration provides additional metal layers for the power distribution networks through topologies unavailable in two-dimensional circuits. With 3-D technologies, individual planes can potentially be dedicated to delivering power.

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I. Savidis and E. G. Friedman are with the Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY 14627 USA (e-mail: ioannis.savidis@rochester.edu; friedman@ece.rochester.edu).

S. Kose is with the University of South Florida, Tampa, FL 33620 USA (e-mail: kose@usf.edu).

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The challenges of efficiently delivering power across a 2-D circuit while satisfying local current requirements have been explored for decades [2], [3]. Two-dimensional power distribution networks are designed to achieve specific noise requirements. A variety of techniques have been developed to minimize both *IR* drops and $L \cdot di/dt$ noise [4], [5], such as multi-tiered decoupling placement schemes [6]–[8] and power gating [9]. These techniques have been effective with increasing current demands of each progressive technology node. 3-D integrated systems however are in its infancy, and much work is required to design efficient power distribution topologies for these vertically integrated systems.

Power delivery in 3-D integrated systems presents difficult new challenges for delivering sufficient current to each device plane. Stacking device planes in the vertical direction leads to higher power densities [10]. Specialized techniques are required to ensure that each device plane is operational, while not exceeding the target output impedance [3]. The focus of this paper is on a primary issue in 3-D power delivery, the power distribution network, and provides a quantitative experimental analysis of the noise measured on each plane within a three plane 3-D integrated stack.

The effects of the through silicon vias (TSVs) on the *IR* voltage drops and $L \cdot di/dt$ noise are significant, as the impedance of a 3-D power distribution network is greatly affected by the TSV density. In addition, the electrical characteristics of a TSV vary based on the 3-D via diameter, length, and dielectric thickness [11], [12]. A comparison of two different via densities for identical power distribution networks is also provided in this paper, and implications of the 3-D via density on the power network design process are discussed.

The proper placement of decoupling capacitors can potentially reduce noise within the power network, while enhancing performance. The effect of board level decoupling capacitors on *IR* and $L \cdot di/dt$ noise in 3-D circuits is also described here. Methods for placing decoupling capacitors at the interface between planes to minimize the effects of inter-plane noise coupling are also suggested.

The 3-D test circuit is described in the following section. A brief summary of the MITLL 3-D process is provided in Section III. Experimental results of the noise characteristics of the power distribution networks are presented in Section IV. A discussion of the experimental results and the effect of the choice of power distribution topology on the noise characteristics of the power network is provided in Section V. Some conclusions are offered in Section VI.

## II. Design of 3-D Power Distribution Network Test Circuit

The fabricated test circuit is 2 mm × 2 mm, and composed of four equal area quadrants. Three quadrants are used to evaluate the effects of the topology of the power distribution network on

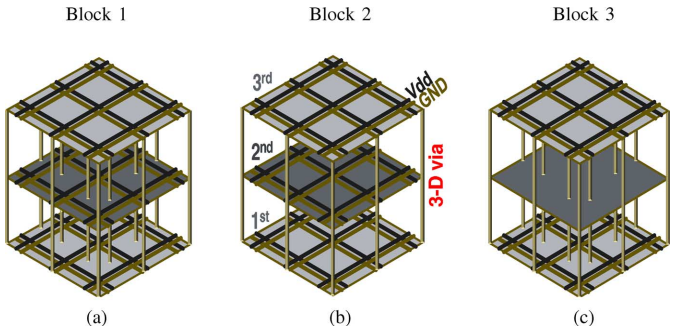


Fig. 1. Power distribution network topologies. (a) interdigitated power network on all planes with the 3-D vias distributing current on the periphery and through the middle of the circuit, (b) interdigitated power network on all planes with the 3-D vias distributing current on the periphery, and (c) interdigitated power network on planes 1 and 3 and power/ground planes on plane 2 with the 3-D vias distributing current on the periphery and through the middle of the circuit.

the noise propagation characteristics, and one quadrant is dedicated to DC-to-DC conversion. Each stacked power network is 530 μm × 500 μm, and includes three discrete two-dimensional power networks, one network within each of the three device planes. The total area occupied by each block is less than 0.3 $mm^2$, representing a portion of a power delivery network. Each block includes the same logic circuit but utilizes a different power distribution architecture. The power supply voltage is 1.5 volts for all of the blocks. The different power distribution architectures are reviewed in Section II.A, and the logic circuitry common to each power module is described in Section II.B.

### A. 3-D Power Topologies

Interdigitated power/ground lines are used in each of the power network topologies. There are five main objectives for the test circuit: i) determine the peak and average noise within the power and ground distribution networks, ii) determine the effect of the board level decoupling capacitors on reducing power noise, iii) explore the effects of a dedicated power/ground plane on the power noise, iv) investigate the effects of the TSV density on the noise characteristics of the power network, and v) evaluate the resonant characteristic frequency of each power network topology.

The three topologies are illustrated in Fig. 1. The difference between the left (Block 1) and central (Block 2) topologies is the number of TSVs, where the latter topology contains two-thirds the number of TSVs. The third topology (Block 3) replaces the interdigitated power and ground lines on the second device plane with two metal planes to assess the benefit of allocating dedicated power and ground planes to deliver current to the loads within a 3-D system. The interdigitated power and ground lines are both 15 μm wide and separated by a 1 μm space for all three power distribution networks. The power and ground planes of Block 3 are separated by a 1 μm space of inter-layer dielectric composed of plasma etched, chemical vapor deposited tetra-ethyl-ortho-silicate (TEOS). Based on the experimental results, enhanced understanding of the noise propagation properties of these 3-D power network topologies has been achieved.

### B. 3-D Circuit Architecture

The three power networks utilize identical on-chip circuitry, with two of the topologies only differing by the total number of TSVs required to distribute power to the lower two device planes. With one network, 1,728 TSVs are placed along both the inner and outer interdigitated power/ground lines, as shown in Fig. 1(a), while the second network includes 1,152 TSVs located along the outer peripheral interdigitated power/ground lines, as depicted in Fig. 1(b). The third power network topology also includes 1,728 TSVs, but the interdigitated power network on the second stacked die is replaced with two metal planes, one for ground and one for power.

The basic logic blocks are illustrated in Fig. 2. The power supply noise generators deliver different current to the power lines. These noise generators are placed on each plane of each power network topology. Voltage sense circuitry is included on each of the planes of each test block to measure the noise on both the power and ground lines. The second plane of the power delivery network, illustrated in Fig. 1(c), does not include noise sense circuitry or noise generation circuitry as this plane is dedicated to power and ground. The voltage range and average voltage of the sense circuitry on each plane for each test block are compared for the three topologies illustrated in Fig. 1.

A schematic of the on-chip circuitry on each plane of each power network is shown in Fig. 2. The circuit is designed to emulate a power load drawing current, generating noise within the power and ground networks. Two sets of circuits are present, noise generating circuits and noise detection circuits. The noise generating circuits include ten current mirrors per device plane (fifteen for the second device plane), 250 MHz, 500 MHz, and 1 GHz ring oscillators, and five, eight, nine, and ten bit pseudorandom number generators (PRNG). The clock pulses generated by the ring oscillators are buffered and fed into the PRNGs, which are again buffered before randomly driving the current mirrors as enable bits. Each current mirror requires eight enable bits, with each enable bit turning on one branch of the current mirror which draws a maximum 4 mA current at increments of 0.5 mA (0.5 mA per branch). With ten current mirrors on each of the first and third device planes and fifteen current mirrors on the second plane, the maximum current drawn by each power network is 140 mA at 1.5 volts, producing a maximum power density of 79 W/$cm^2$ in each 530 μm × 500 μm topology.

The noise detection circuits include separate circuits for evaluating power and ground noise. A schematic of the power and ground detection circuits is shown in Fig. 3. These single stage amplifier circuits utilize an array structured noise detection circuit, as suggested in [13]. Each device plane contains both power and ground noise detection circuits. An off-chip resistor, labeled $R_{bias}$ in Fig. 3, biases the output node of the PMOS current mirror (with a PMOS threshold voltage of $-0.56$ V), and ensures that the current mirror operates in the saturation region. The resistor is chosen to ensure that the maximum voltage at the output node of the current mirror does not exceed 400 mV, the voltage at which the current mirror enters the triode region. The measured current at the output of the current mirror ranges between 200 milliamperes and 300 milliamperes. Since $R_{bias}$ is chosen as 100 Ω, the maximum voltage at the

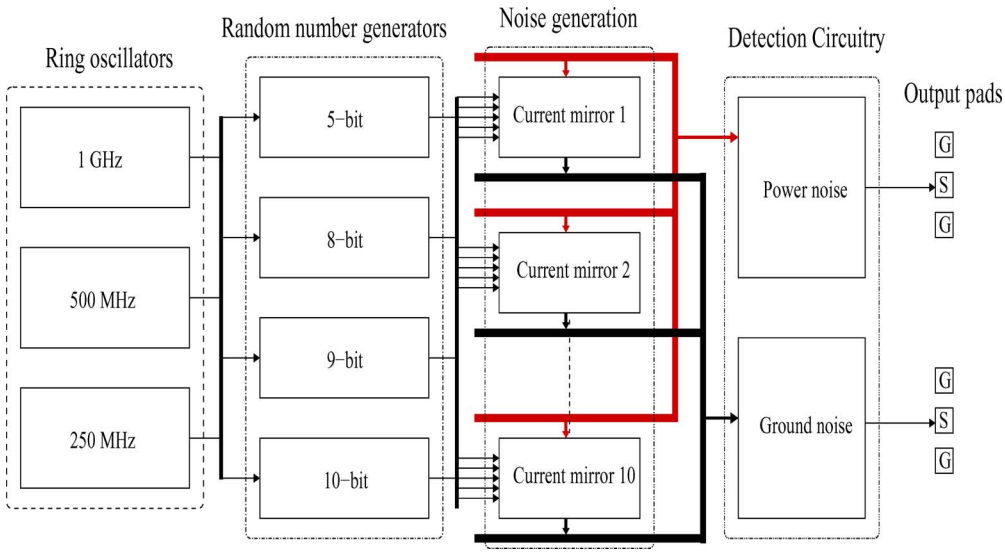


Fig. 2. Block level schematic of noise generation and detection circuits.

output node is 300 mV. In addition, the intrinsic impedance $Z_o$, shown in Fig. 3, is 50 Ω.

Two sets of ground-signal-ground (GSG) output pads source current from the final stage of the noise detection circuits of all three planes, as shown in Fig. 2. One set of GSG output pads is dedicated to the three noise detection circuits that monitor the power network, while the other set of GSG pads supports the three noise detection circuits that monitor the ground network. Counter logic rotates the control of the output pads among the three device planes every $2^{18}$ cycles (at a 250 MHz clock) for both the power and ground noise detection circuits. A second isolated power and ground network with a 2 μF board level decoupling capacitor ensures that the generated noise is not injected into the detection circuits.

## III. 3-D IC Fabrication Technology

The manufacturing process developed by MITLL for fully depleted silicon-on-insulator (FDSOI) 3-D circuits is described in [14] and [15]. The MITLL process is a wafer level 3-D 150 nm integration technology with up to three FDSOI 150 mm wafers vertically bonded with TSVs to form a 3-D circuit. The operating voltage of the SOI transistors is 1.5 volts. The technology includes one polysilicon layer and three metal layers interconnecting the devices on each wafer. A backside metal layer also exists on the upper two planes, providing the starting and landing pads for the TSVs, and the I/O, power supply, and ground pads for the overall 3-D circuit. An attractive feature of this process is the high density TSVs. The dimensions of the TSVs are 1.25 μm × 1.25 μm, and 10 μm deep, much smaller than many existing 3-D technologies [16], [17]. Two of the SOI wafers are thinned to less than 15 μm, while the third layer is used as a handle wafer with a substrate thickness of around 675 μm [14]. An intermediate step of the fabrication process is illustrated in Fig. 4. As depicted in this figure, this process includes both face-to-face and face-to-back plane bonding. The SOI device layers are used for both monolithic [18] and wafer level 3-D integrated systems. SOI is an effective technology for 3-D circuits since the wafers can be aggressively thinned as compared to standard bulk CMOS technologies [19]. This capability results in significantly shorter TSVs, a critical issue in 3-D systems. The primary obstacle for 3-D SOI technologies is the high thermal resistance of the oxide which impedes the heat removal process [20]. A microphotograph of the fabricated die is shown in Fig. 5.

## IV. Experimental Results

The noise generated within the power distribution network is detected by a source follower amplifier circuit. A schematic of the amplifier circuit is depicted in Fig. 3. The sense circuits can detect a minimum voltage of 165 μV (from simulation). Noise from the digital circuit blocks is coupled into the sense circuit through the node labeled $DV_{dd}$. The gain of the circuit is controlled by adjusting the analog voltage, labeled $AV_{dd}$ in Fig. 3.

The gain and bandwidth of both the power and ground network noise detection circuits are calibrated by S-parameter extraction. The measured results are shown in Fig. 6. The simulated DC gain and 3 dB bandwidth of the power network detection circuit are, respectively, −3.8 dB and 1.4 GHz. The measured DC gain and 3 dB bandwidth are, respectively, −4.1 dB and 1.3 GHz. Similarly, the simulated DC gain and 3 dB bandwidth of the ground network detection circuit are, respectively, −4.0 dB and 1.35 GHz, and the measured DC gain and 3 dB bandwidth are, respectively, −4.25 dB and 1.15 GHz. For both the power and ground detection circuits, the measured gain is within 3.4% of simulations. The models include the on-chip interconnect (15 Ω), the bias-T inductance (340 μH) and capacitance (3 μF), the resistance to bias the output node, and the 50 Ω intrinsic impedance $Z_o$ of the network analyzer, as shown in Fig. 3.

The power spectral density of the generated noise within the power network with the voltage bias on the current mirrors set to 0.75 volts is shown in Fig. 7. The noise data shown on the top half of Fig. 7 include the effect of a 4 μF board level decoupling capacitance, whereas the noise data on the bottom half of Fig. 7 are without any decoupling capacitance between the

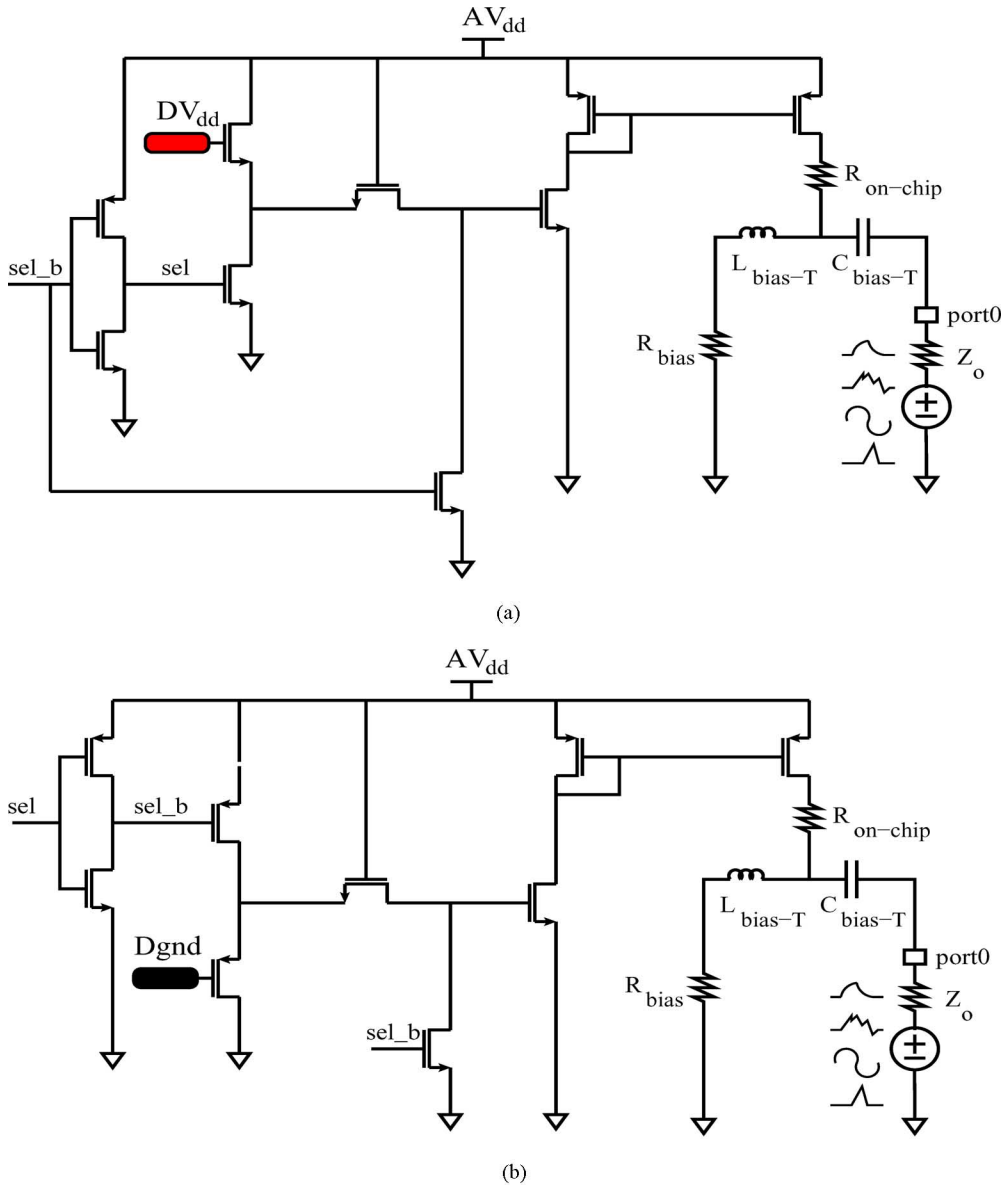


Fig. 3. Source-follower noise detection circuits that detect noise on both the digital (a) power lines, and (b) ground lines.

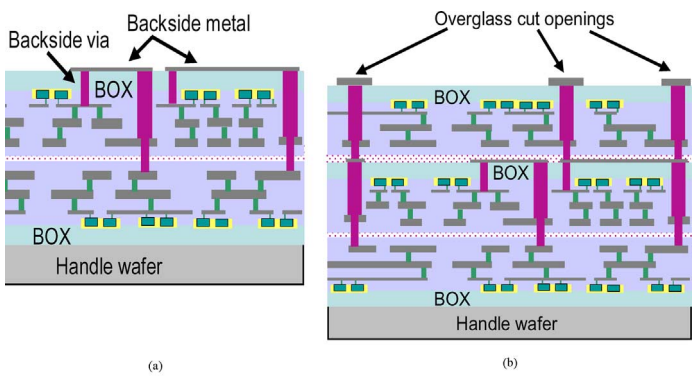


Fig. 4. Cross-sectional view of a 3-D circuit based on the MITTLL process, (a) intermediate step, and (b) fully fabricated 3-D stack [14]. The second plane is flipped and bonded with the first plane, while the third plane is bonded face-to-back with the second plane. The backside metal layer, vias, and through silicon vias are also shown [14].

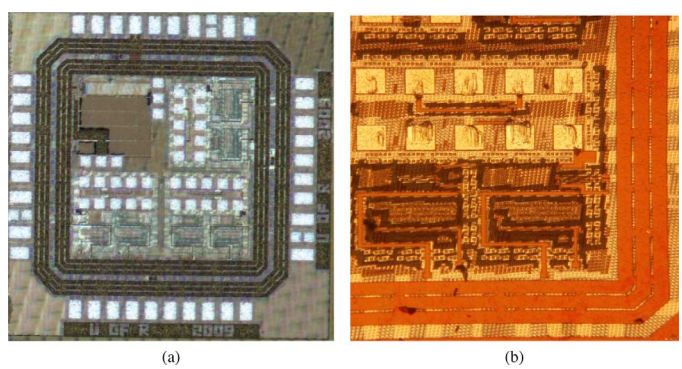


Fig. 5. Fabricated test circuit examining noise propagation for three different power distribution networks and a distributed DC-to-DC rectifier, (a) die microphotograph of the 3-D test circuit, and (b) an enlarged image of Block 1.

power and ground networks. Both plots illustrate the three noise components produced by the 250 MHz, 500 MHz, and 1 GHz ring oscillators. No on-chip decoupling capacitance is added to the three power distribution topologies other than the intrinsic capacitance of the power and ground networks. The peak

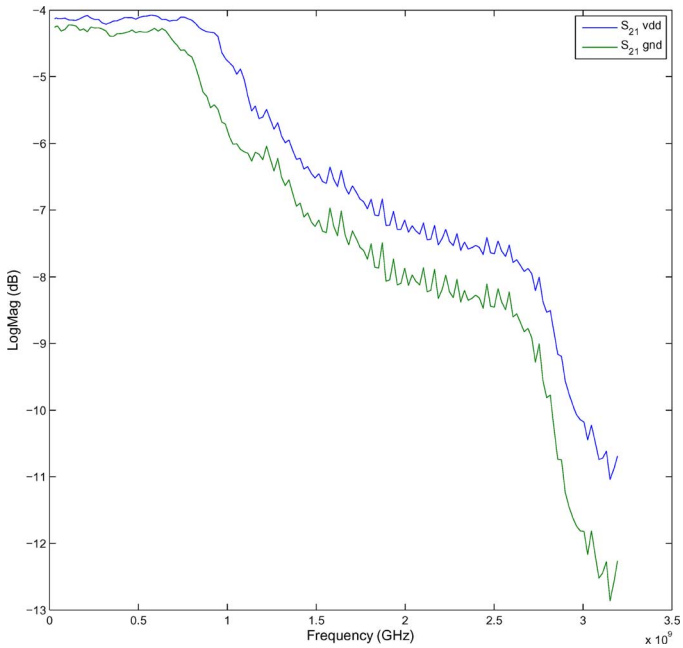


Fig. 6. S-parameter characterization of the power and ground noise detection circuits.

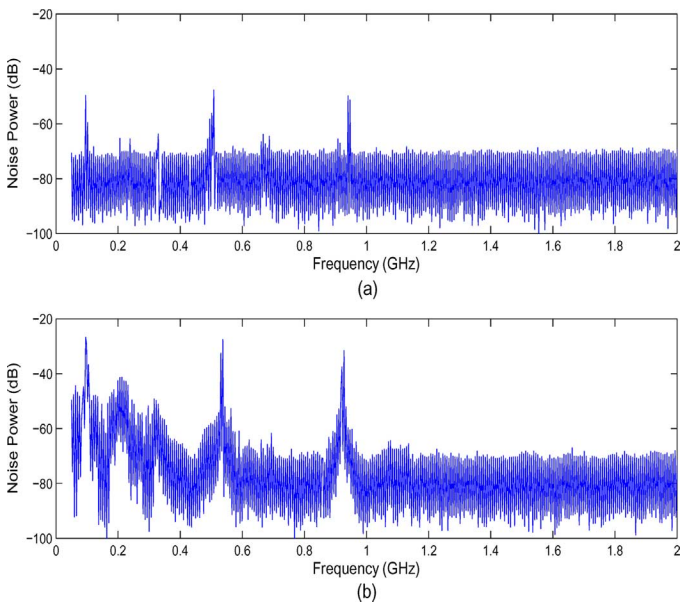


Fig. 7. Spectral analysis of the noise generated on the power line of Block 2 with (a) board level decoupling capacitance, and (b) without board level decoupling capacitance.

noise power does not precisely match the ring oscillator frequencies as the ring oscillators are not tuned to the targeted 250, 500, and 1000 MHz frequencies. The peak noise therefore occurs at 97 MHz (−49 dB), 480 MHz (−47 dB), and 960 MHz (−50 dB) with a board level decoupling capacitor, and at 96 MHz (−27 dB), 520 MHz (−29 dB), and 955 MHz (−33 dB) without a decoupling capacitor. The inclusion of a board level decoupling capacitor reduces the peak noise within the power networks by approximately 20 dB.

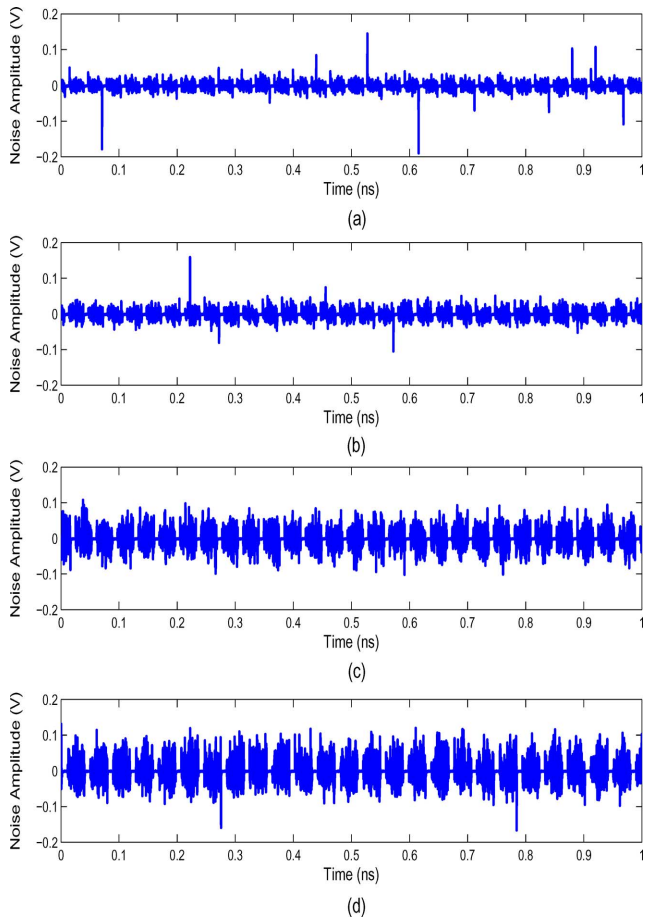


Fig. 8. Time domain measurement of the generated noise on the power line of Block 2 without board level decoupling capacitance for (a) 0 volt, (b) 0.5 volt, (c) 0.75 volt, and (d) 1 volt voltage bias on the current mirrors.

A time domain analysis of the generated noise is used to compare the three different power networks. The detected noise voltage is measured after the intrinsic capacitance of the bias T junction that couples the noise into the oscilloscope and spectrum analyzer (see node labeled port0 in Fig. 3). The noise amplitude with increasing current mirror bias voltage (from 0 to 1 volt) is depicted in Fig. 8. These results indicate that the current mirrors function properly. The 4,096 data points used to generate each subfigure shown in Fig. 8 are centered around 0 volts for both the power and ground network, as only the RF component is passed to the oscilloscope. The average noise for each topology, with or without a board level decoupling capacitance, and for both the power and ground networks as a function of the applied bias voltage to the current mirrors, is shown in Fig. 9. In all cases, with or without decoupling capacitors, the network topology that includes the metal planes reduces the average noise as compared to the other two topologies, as the metal planes behave as an additional decoupling capacitor. The number of TSVs also affects the magnitude of the noise, as shown in Fig. 9. Reducing the number of TSVs by half increases the average amplitude of the noise by 2% to 14.2%, as the parasitic impedance of the three-dimensional power network is larger. The amplitude of the noise is less than twice as great since the portion of the impedance contributed by the TSVs

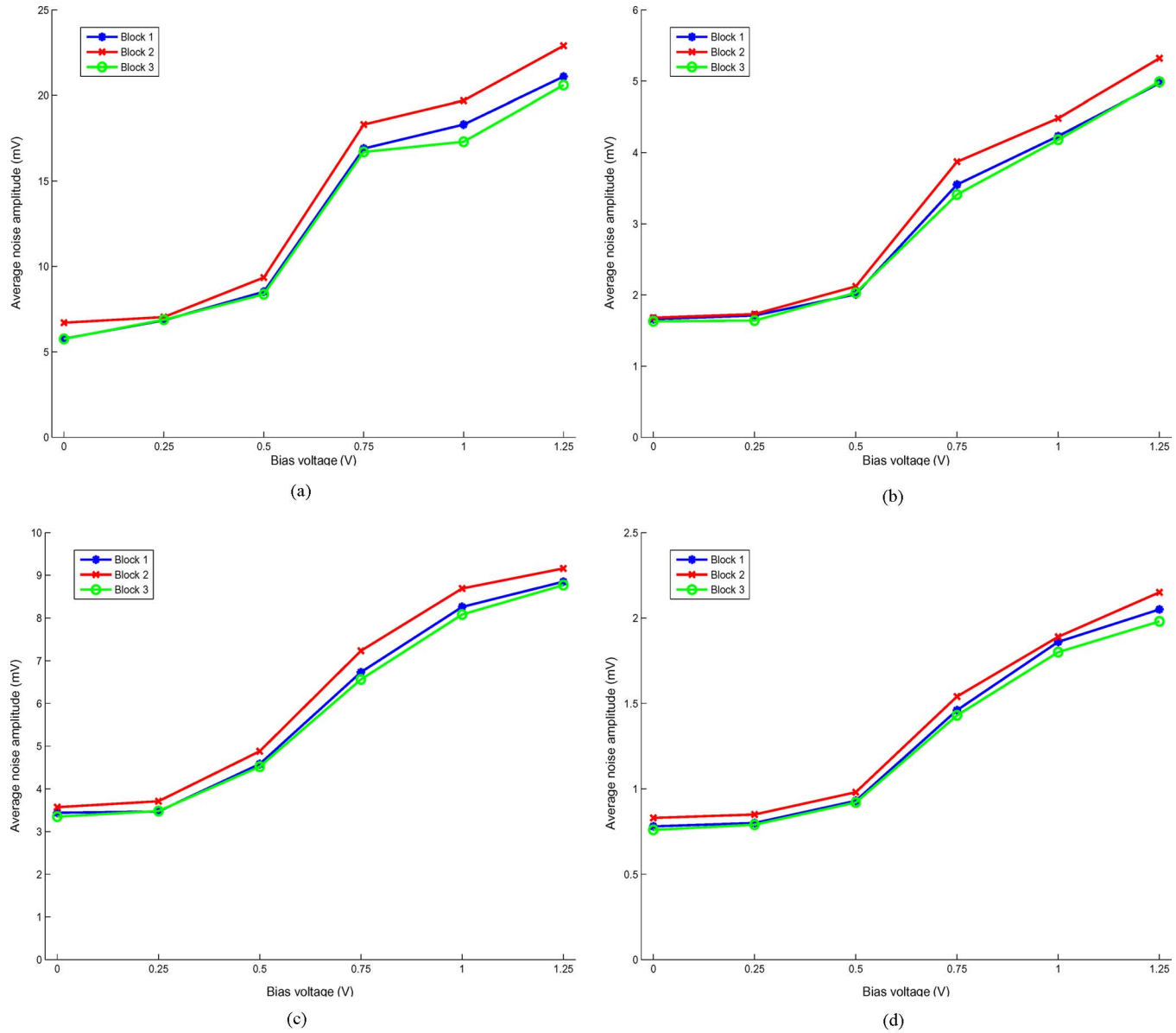


Fig. 9. Average noise voltage on the power and ground distribution networks with and without board level decoupling capacitance. (a) Average noise of power network without decoupling capacitance, (b) average noise of power network with decoupling capacitance, (c) average noise of ground network without decoupling capacitance, and (d) average noise of ground network with decoupling capacitance.

along the path from the power supply through the cables and wirebonds into the 3-D power network and back is a small fraction of the total impedance.

The peak noise for each topology, with or without a board level decoupling capacitance and for both the power and ground networks as a function of the applied bias voltage to the current mirrors, is shown in Fig. 10. Unlike the average noise shown in Fig. 9, the peak voltage detected from each topology does not follow a distinct pattern. No single topology produces the largest noise voltage at any specific current mirror bias voltage. These voltages represent single data points indicative of the maximum peak-to-peak noise voltage for each topology at each bias voltage. For the average noise voltage, Block 3 produces a lower average noise than Block 1, which produces a lower average noise than Block 2. Interestingly, the average noise for each topology is approximately 75% to 90% lower than the peak-to-peak noise voltage, indicating that a majority of the noise data are located within close proximity of the nominal power and ground voltages. In addition, the saturation voltage of the detection circuitry at the output node (port0) is approximately 230 mV when the gain is $-4.2$ dB. The noise detection range is approximately 600 mV centered around 1.5 volts and 0 volts, respectively, for the power and ground lines. The detection circuits for the power network, therefore, detect noise that ranges from 1.2 volts to 1.8 volts, and for the ground networks, from $-0.3$ volts to 0.3 volts.

In addition to the peak and average noise voltage measurements for each power network topology, an analysis of the current drawn by the digital power network is presented. The measured current for each block within the test circuit as a function of the bias voltage applied to the current mirrors is listed in Table I. Each topology draws a similar amount of current as the

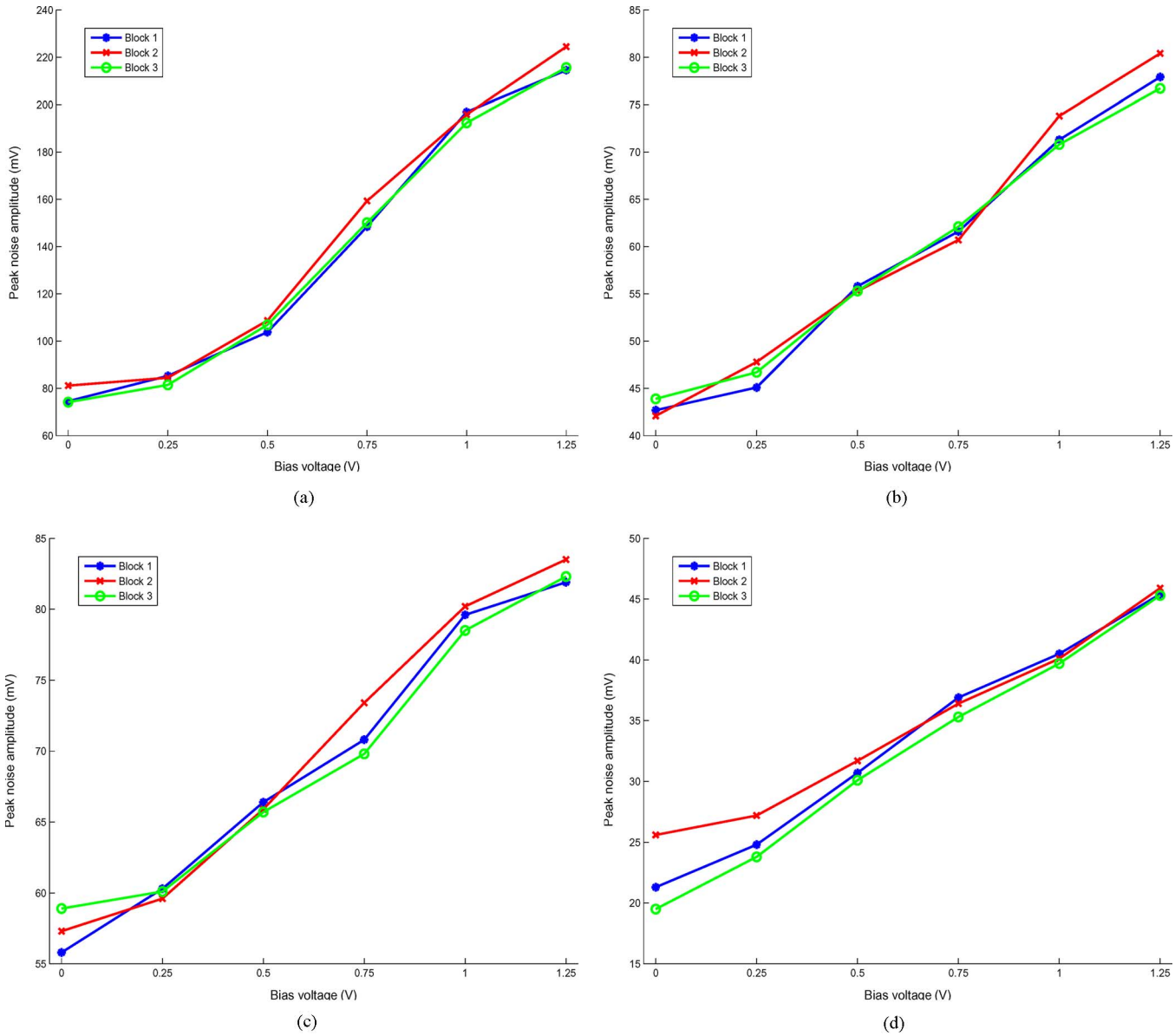


Fig. 10. Peak noise voltage on the power and ground distribution networks with and without board level decoupling capacitance. (a) Peak noise of power network without decoupling capacitance, (b) peak noise of power network with decoupling capacitance, (c) peak noise of ground network without decoupling capacitance, and (d) peak noise of ground network with decoupling capacitance.

TABLE I
POWER SUPPLY CURRENT WITHIN THE DIFFERENT POWER DISTRIBUTION TOPOLOGIES AS A FUNCTION OF BIAS VOLTAGE ON THE CURRENT MIRRORS

| Power network block | Current as function of bias voltage (mA) | | | | | |
|---|---|---|---|---|---|---|
| | 0 volts | 0.25 volts | 0.5 volts | 0.75 volts | 1 volts | 1.25 volts |
| Block 1 | 29.2 to 34.6 | 31.4 to 38.7 | 40.1 to 45.3 | 56.2 to 59.8 | 73.6 to 79.5 | 86.4 to 91.3 |
| Block 2 | 32.6 to 38.5 | 33.6 to 40.1 | 43.7 to 47.8 | 59.2 to 66.3 | 75.5 to 82.5 | 88.6 to 93.8 |
| Block 3 | 43.6 to 55.3 | 44.1 to 56.3 | 52.9 to 65.1 | 68.7 to 78.7 | 83.4 to 91.9 | 97.5 to 105.7 |

total number of current mirrors for each power network is identical. The data listed in Table I reveal that Blocks 1 and 2 sink similar currents. Block 3 draws about 30% to 45% more current as compared to the other two topologies. The Block 3 topology includes power and ground planes on the second device plane; therefore, in this topology, both leakage between these two large planes as well as leakage from the TSVs distributing power to the bottom plane contribute additional current. Based on the currents listed in Table I and a 1.5 volt power supply, a peak power density of 59.8 W/cm$^2$ is achieved for Block 3 when the current mirrors are biased with a voltage of 1.25 volts.

## V. EFFECT ON 3-D POWER DISTRIBUTION TOPOLOGIES

The choice of power distribution topology affects the noise propagation characteristics of the power network, as indicated by the results described in Section IV. Additional insight into

the design of the power networks (see Section V.A), and a discussion on the effect of the design of the 3-D power distribution network based on the experimental results (see Section V.B) is provided in this section.

### A. Pre-Layout Design Considerations

Several considerations are accounted for in the design of the power distribution topologies. One issue is the placement of a sufficient number of TSVs to ensure the mitigation of electromigration between planes. The total number of TSVs required to satisfy a target current density of $1 \times 10^6$ A/cm$^2$, a current load of 0.14 amperes, a TSV diameter of 1.25 µm, and a footprint of 530 µm by 500 µm (the footprint area of each power distribution network) verifies that the 576 and 864 TSVs per plane, respectively, for Block 2 and Blocks 1 and 3, far exceed the necessary twelve TSVs to mitigate electromigration. The number of TSVs to satisfy electromigration constraints is determined as follows,

$$\text{Area}_{\text{target current density}} = \frac{I_{\text{load}}}{J_{\text{electromigration}}}, \quad (1)$$

$$\text{Number of TSVs} = \frac{\text{Area}_{\text{target current density}}}{\text{Area}_{\text{TSV}}}. \quad (2)$$

The diameter of the TSV determines the "keep out zone" surrounding the TSV, an area where no devices can be fabricated. For the MIT Lincoln Laboratories 3-D technology, the keep out zone is approximately two times the diameter $D$. A square area with a width of $2\times D$ and depth of $2\times D$ is therefore used to determine the area penalty per TSV. An area of 1.36% and 2.04% of the 530 µm by 500 µm area is occupied by each power distribution topology on each device plane for, respectively, 576 and 864 TSVs. The area is the same for planes 2 and 3, where all I/Os originate from plane 3. No area penalty on device plane 1 exists as no TSVs are necessary in this front-to-back bonded plane (the TSVs land on metal 3 on plane 1). For a keep out zone equivalent to $3 \times D$, the area penalty is 3.06% and 4.58%, respectively, for 576 and 864 TSVs.

To determine the resonant frequency of each topology, a model of the 3-D power distribution networks includes the impedance of the cables, board, wirebonds, on-chip DC pads, TSVs, and the power distribution network on each device plane. The equivalent electrical parameters are listed in Table II, and the capacitance of the 3-D power distribution topologies is listed in Table III. The impedances listed in Table II for the cables, board, and wirebonds are divided into three equivalent $\pi$-models to characterize the distributed nature of the lines, as shown in Fig. 11.

The interdigitated power and ground lines in metal 3 are 530 µm long, 15 µm wide, and exhibit a sheet resistance of 0.08 Ω per sheet, producing a 2.83 Ω resistance. Similarly, the metal 2 lines are 500 µm long, 15 µm wide, with a sheet resistance of 0.12 Ω per sheet, producing a 4 Ω resistance. Each power and ground line is divided into eight equal *RLC* $\pi$-model segments to represent the distributed nature of the on-chip metal lines. An inductance of 1 pH is added to each $\pi$-model segment. There are three horizontal pairs (metal 3) of power and ground lines as well as three vertical pairs (metal 2) of power and ground lines for each interdigitated power distribution network on each device plane. The *RLC* parameters for a single $\pi$-segment of the interdigitated topology models the plane topology, but the connections between segments is modified to better characterize the power and ground planes, as shown in Fig. 11.

The resonant frequency for the three different power distribution networks is determined with and without board level decoupling capacitors, and with and without an on-chip load capacitance (in addition to the intrinsic capacitance of the power distribution network). The resulting resonant frequency for the three power distribution topologies for the different capacitive configurations is listed in Table IV. The resonant frequencies reported in Table IV account for the distributed inductance of the cables, board, wirebonds, and on-chip power distribution network. The on-chip inductance produces the highest resonant frequency reported in Table IV for any given block. The other three resonant frequencies, from the smallest to the largest, are dependent, respectively, on the cable, board, and wirebond inductances. The presence of a board-level decoupling capacitor eliminates all but the the highest resonant frequency, the resonance caused by the on-chip inductance.

### B. Design Considerations Based on Experimental Results

Based on the experimental results, both doubling the number of TSVs and utilizing a dedicated power and ground plane lowers the power noise. Although the noise is lower with both a greater number of TSVs and dedicated power network planes (2% to 14.2% lower noise, as listed in Table V), the power noise is limited by the small series resistance of the 3-D power network as compared to the larger series resistance of the cables and wirebonds, as described in Section V.A.

Two issues in 3-D power distribution networks are considered based on the experimental results: 1) the benefit of the power and ground planes to justify the use of two metallization levels, and 2) the benefits and drawbacks of increased TSV density on area and reducing noise. Addressing 1), the power planes provide an additional reduction of 0.2% to 5.5% in average noise as compared to the fully interdigitated topology. The reduction in average noise is primarily due to the increased capacitance of the power and ground networks, as indicated in Table III. The average noise characteristics of the planes topology can be further improved by increasing the size of the power/ground planes or using multiple metal layers for both power and ground. The use of full planes to deliver current to the load does require significant metal resources, and therefore this cost must be considered. In addition, the power planes complicate the design of the signal interconnects, where holes are required in the power/ground planes to pass signals between device planes. For those applications where additional noise reduction is required, extra metallization and design complexity may be justified.

The TSV density provides the greatest reduction in average noise, ranging from 2.7% to 14.0%, as listed in Table V. The additional area penalty when increasing the number of TSVs by 50% from 576 to 864 is 0.68% (1.36% as compared to 2.04%), noting that the area penalty is also dependent on the keep out region, as described in Section V.A. The increased area due to the higher TSV density is small as compared to the large reduction in average noise.

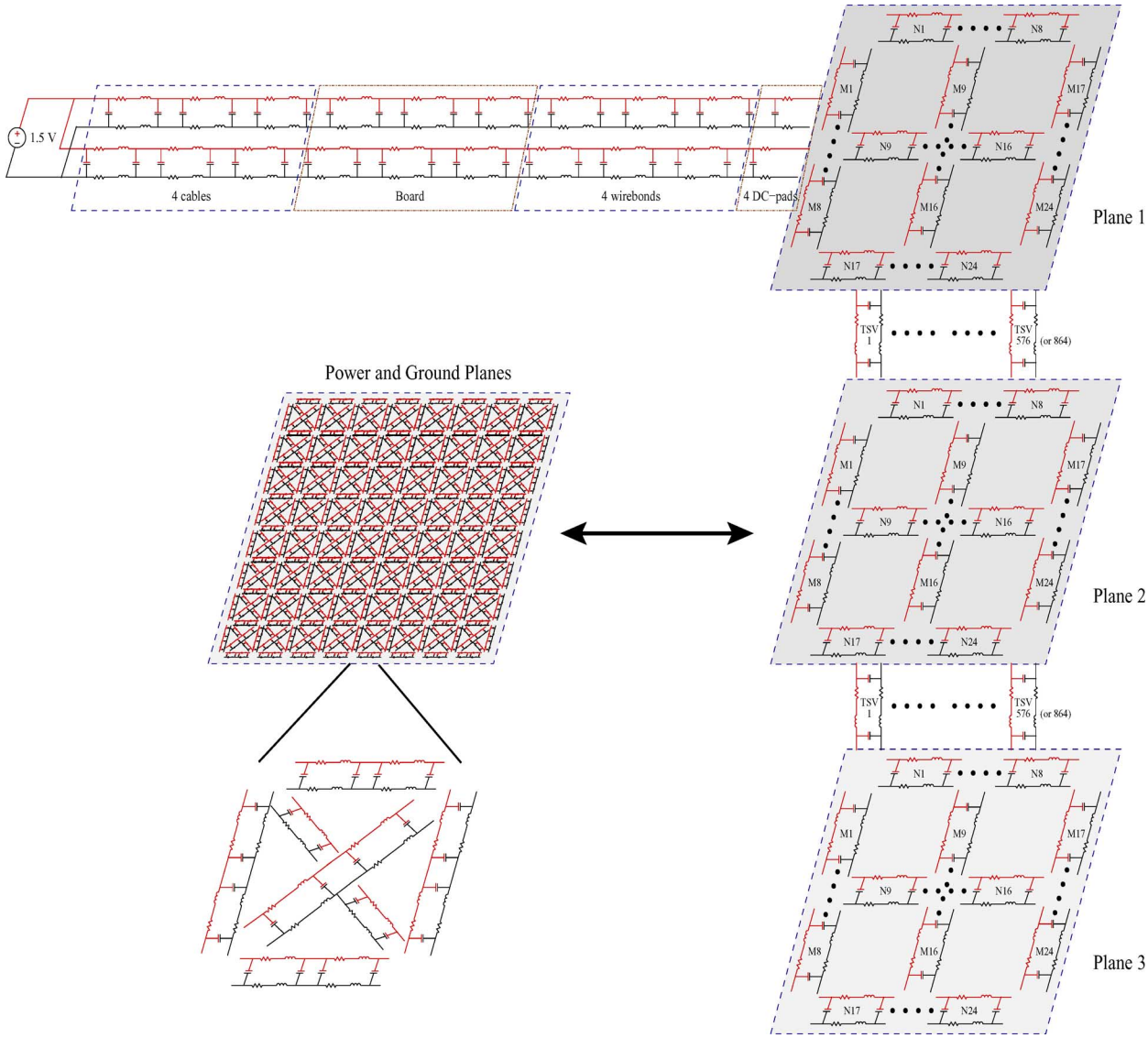


Fig. 11. Equivalent electrical model of the cables, board, wirebonds, on-chip DC pads, power distribution networks, and TSVs.

TABLE II
PHYSICAL AND ELECTRICAL PARAMETERS OF THE CABLES, BOARD, WIREBONDS, ON-CHIP DC PADS, POWER DISTRIBUTION NETWORKS, AND TSVS

| Component | Width (μm) | Diameter (μm) | Length (mm) | Thickness (μm) | Resistance (Ω) | Capacitance (pF) | Inductance (nH) |
|---|---|---|---|---|---|---|---|
| Cables | — | 1020 | 965.2 | — | 0.072 | 10.59 | 1445.75 |
| Board | 760 | — | 40 | 43.2 | 0.021 | 1.88 * | 26.48 |
| Wirebonds | — | 25.4 | 4 to 5 | — | 0.278 | 0.0233 | 5.92 |
| DC pads | 80 | — | 0.12 | 2 | — | 0.0717 | — |
| Pad to power grid | 60 | — | 0.260 | 0.63 | 0.52 | — | — |
| TSV | — | 1.25 | 0.009 | — | 0.4 | $0.124 \times 10^{-3}$ ** | $5.55 \times 10^{-3}$ |

* An additional 4 μF when board level decoupling capacitors are added. ** Coupling capacitance between two TSVs [11].

## VI. CONCLUSIONS

The design of a power distribution network for application to 3-D circuits is considerably more complex than the design of a two-dimensional power network. The preferable topology of a power distribution network is not dictated by a single design objective but rather by the overall 3-D system level requirements including the availability of I/O pins, and number of bonded planes.

A three-dimensional (3-D) test circuit examining power grid noise in a 3-D integrated stack has been designed, fabricated, and tested. Three topologies to distribute power within a 3-D circuit have been evaluated, and an analysis of the peak noise voltage, voltage range, average noise voltage, and resonant frequency characteristics for both power and ground is described. Fabrication and vertical bonding were performed by MIT Lincoln Laboratory for a 150 nm, three metal layer SOI process. Three wafers are vertically bonded to form a 3-D stack. A noise analysis of three power delivery topologies is described. Calibration circuits for a source follower sense circuit compare the different power delivery topologies as well as the individual 3-D

TABLE III
CAPACITANCE OF THE THREE DIFFERENT POWER DISTRIBUTION BLOCKS, AND INTERDIGITATED AND POWER/GROUND PLANES

| Block or topology | Power or ground | Capacitance (fF) | Capacitance with load (fF) |
|---|---|---|---|
| Interdigitated | $V_{dd}$ | 330.09 | — |
| | $V_{gnd}$ | 330.08 | — |
| Planes | $V_{dd}$ | 1000.35 | — |
| | $V_{gnd}$ | 1158.24 | — |
| Block 1 | $V_{dd}$ | 993.38 | 1631.68 |
| | $V_{gnd}$ | 993.39 | 1596.38 |
| Block 2 | $V_{dd}$ | 964.37 | 1610.37 |
| | $V_{gnd}$ | 964.38 | 1574.18 |
| Block 3 | $V_{dd}$ | 1862.74 | 2487.10 |
| | $V_{gnd}$ | 1949.60 | 2590.36 |

TABLE IV
RESONANT FREQUENCY OF THE THREE DIFFERENT POWER DISTRIBUTION NETWORKS WITH AND WITHOUT BOARD LEVEL DECOUPLING CAPACITORS, AND WITH AND WITHOUT AN ON-CHIP LOAD CAPACITANCE

| Block | Decap ($\mu$F) | Extracted load (fF) | Resonant frequencies (GHz) |
|---|---|---|---|
| Block 1 | none | none | 0.224, 0.447, 0.794, 1.25 |
| | 4 | none | 1.25 |
| | none | 638 | 0.199, 0.447, 0.708, 1.25 |
| | 4 | 638 | 1.25 |
| Block 2 | none | none | 0.223, 0.447, 0.794, 1.78 |
| | 4 | none | 1.78 |
| | none | 646 | 0.199, 0.447, 0.708, 1.78 |
| | 4 | 646 | 1.78 |
| Block 3 | none | none | 0.224, 0.447, 0.794, 1.67 |
| | 4 | none | 1.67 |
| | none | 624 | 0.199, 0.447, 0.708, 1.67 |
| | 4 | 624 | 1.67 |

TABLE V
PER CENT REDUCTION IN AVERAGE NOISE FROM THE NOISIEST TOPOLOGY (BLOCK 2) TO THE LEAST NOISY TOPOLOGY (BLOCK 3) AS A FUNCTION OF BIAS VOLTAGE ON THE CURRENT MIRRORS

| Power or ground | Decap present | Noisier Block | Quieter Block | Per cent noise reduction as function of bias voltage 0 V | 0.25 V | 0.5 V | 0.75 V | 1 V | 1.25 V |
|---|---|---|---|---|---|---|---|---|---|
| Power | No | 2 | 1 | 14.0 | 2.7 | 8.9 | 7.7 | 7.1 | 7.9 |
| | | 2 | 3 | 14.2 | 2.3 | 10.5 | 8.7 | 12.2 | 10.0 |
| | | 1 | 3 | 0.2 | -0.4 | 1.8 | 1.2 | 5.5 | 2.4 |
| Power | Yes | 2 | 1 | 1.2 | 1.2 | 5.2 | 8.3 | 5.6 | 6.6 |
| | | 2 | 3 | 3.0 | 5.2 | 4.2 | 11.9 | 6.7 | 6.2 |
| | | 1 | 3 | 1.8 | 4.1 | -1.0 | 3.9 | 1.2 | -0.4 |
| Ground | No | 2 | 1 | 3.6 | 6.5 | 6.1 | 6.9 | 4.9 | 3.4 |
| | | 2 | 3 | 6.2 | 6.2 | 7.4 | 9.3 | 7.0 | 4.3 |
| | | 1 | 3 | 2.6 | -0.3 | 1.3 | 2.5 | 2.2 | 0.9 |
| Ground | Yes | 2 | 1 | 6.0 | 5.9 | 5.1 | 5.2 | 1.6 | 4.7 |
| | | 2 | 3 | 8.4 | 7.1 | 6.1 | 7.1 | 4.8 | 7.9 |
| | | 1 | 3 | 2.6 | 1.3 | 1.1 | 2.1 | 3.3 | 3.4 |

circuits. The effect of the TSV density on the noise profile of a 3-D power delivery network is experimentally described. A comparison of the peak noise and resonant behavior for each topology with and without board level decoupling capacitors is provided and suggestions for enhancing the design of the power delivery network are offered. This test circuit provides greater understanding of topology dependent noise generation and propagation in 3-D power delivery systems.

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**Ioannis Savidis** (S'04) received the B.S.E. degree in electrical and computer engineering and biomedical engineering from Duke University, Durham, NC, in 2005. He received the M.Sc. degree in electrical and computer engineering from the University of Rochester, Rochester, NY, in 2007, and is currently completing the Ph.D. degree in electrical and computer engineering under the guidance of Prof. Eby G. Friedman.

He interned at Freescale Semiconductor Corporation, Austin, TX, during the summers of 2006 and 2007, where he worked on the electrical characterization and modeling of interplane 3-D vias. During the summers of 2008, 2009, and 2010 he interned at the IBM T. J. Watson Research Center, Yorktown Heights, NY, where he worked on electrical characterization and modeling, reticle design, and DC and high frequency electrical measurements of test vehicles implementing various interplane 3-D via topologies. His research interests include analysis, modeling, and design methodologies for high performance digital and mixed-signal integrated circuits, emerging integrated circuit technologies, and interconnect related issues, with an emphasis on electrical and thermal modeling and characterization, signal and power integrity, and power and clock delivery for 3-D IC technologies.

**Selcuk Kose** (S'10–M'12) received the B.S. degree in electrical and electronics engineering from Bilkent University, Ankara, Turkey, in 2006, and the M.S. and Ph.D. degrees in electrical engineering from the University of Rochester, Rochester, NY, in 2008 and 2012, respectively.

He is currently an Assistant Professor with the Deparment of Electrical Engineering, University of South Florida, Tampa, Florida. He was a part-time Engineer with the VLSI Design Center, Scientific and Technological Research Council (TUBITAK), Ankara, Turkey, where he worked on low power ICs in 2006. During the Summers of 2007 and 2008, he was with the Central Technology and Special Circuits Team in the enterprise microprocessor division of Intel Corporation, Santa Clara, CA, where he was responsible for the functional verification of a number of blocks in the clock network including the de-skew machine and optimization of the reference clock distribution network. In Summer 2010, he interned in the RF, Analog, and Sensor Group, Freescale Semiconductor, Tempe, AZ, where he developed design techniques and methodologies to reduce electromagnetic emissions. His current research interests include the analysis and design of high performance integrated circuits, monolithic DC-DC converters, and interconnect related issues with specific emphasis on the design and analysis of power and clock distribution networks, 3-D integration, and emerging integrated circuit technologies.

Prof. Kose is an Associate Editor of the *Journal of Circuits, Systems, and Computers*.

**Eby G. Friedman** (M'79–SM'90–F'00) received the B.S. degree from Lafayette College in 1979, and the M.S. and Ph.D. degrees from the University of California, Irvine, in 1981 and 1989, respectively, all in electrical engineering.

From 1979 to 1991, he was with Hughes Aircraft Company, rising to the position of manager of the Signal Processing Design and Test Department, responsible for the design and test of high performance digital and analog ICs. He has been with the Department of Electrical and Computer Engineering at the University of Rochester since 1991, where he is a Distinguished Professor, and the Director of the High Performance VLSI/IC Design and Analysis Laboratory. He is also a Visiting Professor at the Technion–Israel Institute of Technology. His current research and teaching interests are in high performance synchronous digital and mixed-signal microelectronic design and analysis with application to high speed portable processors and low power wireless communications.

Dr. Friedman is the author of over 400 papers and book chapters, a dozen patents, and the author or editor of 15 books in the fields of high speed and low power CMOS design techniques, 3-D design methodologies, high speed interconnect, and the theory and application of synchronous clock and power distribution networks. He is the Regional Editor of the *Journal of Circuits, Systems and Computers*, a Member of the editorial boards of the *Analog Integrated Circuits and Signal Processing*, *Microelectronics Journal*, *Journal of Low Power Electronics*, *Journal of Low Power Electronics and Applications*, and *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, Chair of the *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* steering committee, and a Member of the technical program committee of a number of conferences. He previously was the Editor-in-Chief of the *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, a Member of the editorial board of the *Proc. IEEE*, *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, and *Journal of Signal Processing Systems*, a Member of the Circuits and Systems (CAS) Society Board of Governors, Program and Technical chair of several IEEE conferences, and a recipient of the University of Rochester Graduate Teaching Award and a College of Engineering Teaching Excellence Award. Dr. Friedman is a Senior Fulbright Fellow and an IEEE Fellow.