Exploiting Hysteresis in a CMOS Buffer

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Abstract— **A high drive CMOS buffer circuit characterized by a voltage transfer characteristic (VTC) with low threshold voltages and hysteresis is proposed. The proposed circuit is capable of restoring slow transition times and distorted input signals with a minimum delay penalty. Due to the hysteresis characteristic of this buffer, a comparison with a Schmitt-trigger is provided. An important application of this circuit is the restoration of slow transitioning signals propagated along an *RC* interconnect. The circuit can be used in conjunction with existing repeater insertion methodologies to decrease the delay of an *RC* line.**

I. Introduction

In modern high performance digital circuits, high interconnect resistance and capacitance have become an important factor in limiting performance. Multiple solutions for driving highly capacitive loads such as a High Drive (HD) buffer [1] or cascaded tapered buffers [2–6] have been proposed. Approaches for driving highly resistive RC lines, such as repeaters, have also been described in [7–10].

Existing solutions for driving RC interconnect utilize primarily one approach: inverter-like repeater circuit optimization with an insertion methodology for optimal placement, sizing, and power dissipation. A CMOS inverter driving a distributed RC line is shown in Fig. 1.

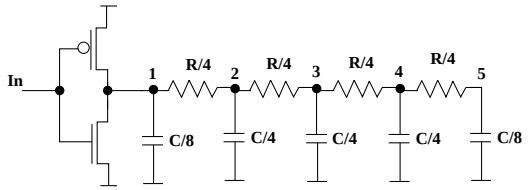

Fig. 1. An inverting repeater driving a distributed RC line.

The signal waveforms at different points of the distributed RC line are shown in Fig. 2 where R = 2 KΩ and C = 3 pF for an input transition time of 0.1 ns. Note that the signal transitions deteriorate as the signal propagates towards nodes 2, 3, 4, and 5.

Two major limiting factors for inserting inverting repeaters along an RC line are noted. The first factor is that a typical $V_{IH} = 3$ V and $V_{IL} = 2$ V (for a $V_{DD} = 5$ V power supply) of a CMOS inverter will drastically limit the speed since these thresholds must be reached in order to switch the state of the inverter. The second factor is the short-circuit power dissipated by the inverter during slow transition time input signals. These two limiting factors require the line be partitioned into multiple smaller segments by inserting repeaters, thereby not permitting the signal to degrade and create long transition times. However, multiple repeaters, combined with typical V_{IH} and V_{IL} values of a CMOS inverter, result in long delays and increased power dissipation [7–10].

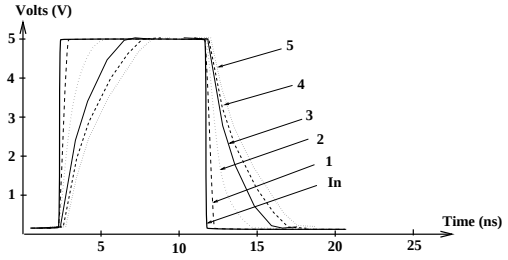

Fig. 2. The signal waveforms at nodes 1, 2, 3, 4, and 5 along the distributed RC line shown in Fig. 1. Note the points of interest, 1 V and 3 V for the low-to-high transition, and 4 V and 2 V for the high-to-low transition.

In this paper, a solution to these problems is provided by a circuit that detects a transitioning input signal early in the transition process. The circuit achieves this early detection of the transitioning input signal by employing a VTC featuring low threshold voltages and hysteresis. Slow and distorted input signals for the proposed circuit are tolerated. By employing an HD buffer-like structure [1], the circuit also provides a high output drive capability (significant output current) and at the same time introduces minimal delay to propagate the signal along the signal path. All of these properties permit the circuit to be used as a repeater to drive highly resistive RC lines. By using this circuit together with a modified repeater insertion methodology [9], the delay of an RC line can be substantially improved, since the RC line is partition into less segments than in a classical repeater insertion process [9].

A detailed description of the operation of the proposed buffer circuit [called the High Drive Repeater (HDR)] is presented in Section II. Some sizing considerations for an HDR circuit are summarized in Section III. Different circuit and performance trade-offs are also discussed in this section. Simulation results characterizing the performances of the proposed circuit are described in Section IV. Finally, some conclusions are presented in Section V.

II. Operation of HDR Circuit

The VTC with hysteresis of the proposed HDR circuit is shown in Fig. 3. For comparison, the VTC with hysteresis of a Schmitt trigger is also shown. The proposed circuit offers thresholds of V_{M+} (V_{IH}) up to 1 V and V_{M-} (V_{IL}) up to 4 V for a process in which $V_T = 0.8$ V. Note that a Schmitt trigger has $V_{M+} = 4$ V and $V_{M-} = 1$ V. Accordingly, the HDR circuit switches when the low-to-high input transition reaches 1 V, while a Schmitt trigger switches at 4 V. Similar behavior occurs for the high-to-low transition (4 V as compared to 1 V). For restoring slow transition input signals, this behavior provides an important gain in speed.

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A three stage transistor level schematic of the proposed HDR circuit is shown in Fig. 4. The first stage consists of two input gates. At least one additional stage, an output stage, is also required. An intermediate (amplifier) stage is also included in Fig. 4. The Q transistors are the driving transistors, while the M transistors are the nulling transistors [1]. Note the symmetric, complementary configuration of the HDR circuit, and the structural similarity to a complementary analog amplifier [11].

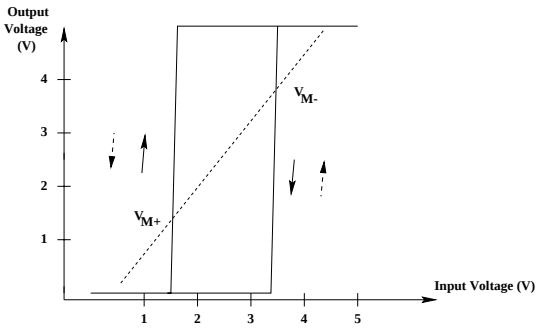

Fig. 3. The VTC of the proposed HDR circuit (the solid arrow). For comparison, the VTC of a Schmitt trigger is also shown (the dotted arrow).

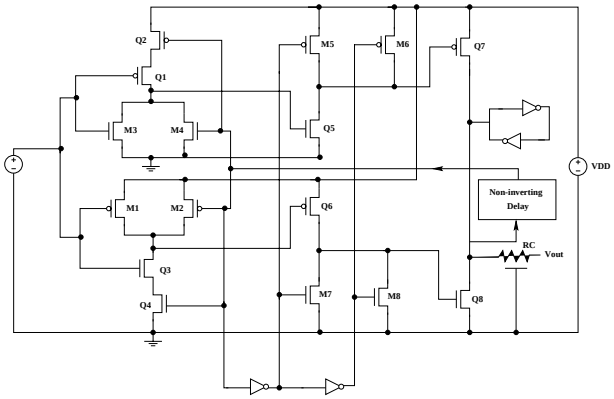

Fig. 4. The transistor level schematic of a three stage HDR circuit

The principal observation to note is that the HDR circuit can operate with slow transition input signals. Consider $T_{rise} = T_{fall} = T_t$, the transition time of the input signal. Several circuit details important in implementing the desired function of the HDR circuit are described below:

1. The input gates are sized to obtain the desired V_{M+} and V_{M-} threshold voltages. The V_{M+} threshold is provided by the NAND gate, while the V_{M-} threshold is provided by the NOR gate. The use of two separate gates together with an HD buffer-like structure provide a single output, with two independent, well controlled V_{M+} and V_{M-} threshold voltages in one circuit with a minimum delay penalty.
2. The HD buffer-like structure reduces the HDR circuit delay and produces a high drive capability. Reducing the delay to a minimum is important since the HDR circuit restores slow transition signals. Any additional delay introduced in the signal path reduces the efficiency of the system. A high drive capability provides a fast response when driving a significant load impedance.
3. The delay element placed in the feedback loop plays a major functional role in this structure. Consider an input signal with T_t = 2 ns and a buffer delay of D = 0.5 ns. Consider a low-to-high input transition that generates a high-to-low output transition through the lower branch of the circuit shown in Fig. 4. If the delay element is not used, after 0.5 ns, the output reaches the low state, finds the input in transition from low-to-high, and activates the upper branch through the NOR gate. The cycle repeats after another 0.5 ns, the buffer output oscillating between states for approximately 1.5 ns until the input reaches the high state. At that point, the output of the buffer settles into an unknown state. By introducing a delay element with a minimum delay of T_t - D (1.5 ns in this example) into the feedback path, this malfunction is prevented.

As mentioned in Section I, the HDR circuit can be used as a repeater to drive highly resistive RC lines. Furthermore, applications that must recover a slow transitioning signal with a minimum delay penalty are appropriate for the HDR circuit. For example, a specific HD buffer driving a capacitive load is described in [1], where up to a 30% savings in power and up to a 500% savings in area as compared to a same speed tapered buffer is demonstrated, the trade-off being up to four times slower output transitions as compared to a tapered buffer system. Using the HDR circuit to restore the slow output transition signals of this HD buffer provides a valuable savings in power and area as compared to a tapered buffer, as well as fast output signal transitions. The trade-off in using an HDR circuit is a decreased noise margin.

III. HDR circuit optimization and related trade-offs

Several simple sizing strategies can be applied for different trade-offs. The sizing rules for an HD buffer [1] are also applicable to an HDR circuit.

- The desired V_{M+} and V_{M-} threshold voltages are obtained from the size of the input gates. M1 and M3 are minimum size. Q1, Q2, Q3, and Q4 are sized to obtain the desired threshold voltages, and are much larger than M1 and M3, permitting a negligible short-circuit power for a slow transitioning input signal. Due to the large size, the Q transistors provide a fast response to the input signal. The same transconductance for the Q1, Q2 and Q3, Q4 pairs is desired to ensure similar amplification for the two signal transitions.
- Q5 and Q6 and similarly all HDR stages are sized to represent a standard load equivalent to a tapering factor of $e = 2.7$ [2, 3] for the transistors of the previous stage. Note that the size of Q5 and Q6 is already considerable, due to the size of the Q1, Q2 and Q3, Q4 pairs. Thus, a two stage HDR may be sufficient for many applications.
- The delay element could be composed of several cascaded inverters or clock controlled latches to introduce the required delay. The actual implementation depends upon the delay value and the circuit characteristics. If a large delay is necessary, the latch-based implementation is more power efficient.
- The remaining portion of the circuit is sized according to an HD buffer [1].

One aspect that should be noted is that an excessive size for Q1, Q2, Q3, and Q4 would adversely increase the load at the insertion points, slowing down the line. However, due to the low threshold voltages of the HDR circuit, the size of Q1, Q2, Q3, and Q4 do not greatly increase the time required to reach these threshold voltages, but rather the time required for the input signal to resolve to the final state is increased.

Several solutions exist to reduce the load at the insertion points without modifying the V_{M+} and V_{M-} threshold voltages:

- The first solution is a tradeoff between the size of Q1, Q2, Q3, and Q4 and the total buffer delay. The threshold voltages of the input gates (V_{M+}, V_{M-}) depend upon the size of the Q1, Q2, Q3, and Q4 transistors and the input gate loads (related to the size of Q5 and Q6). Choosing Q5 and Q6 as minimum size, V_{M+} and V_{M-} are greatly decreased. Accordingly, smaller sizes for the Q1, Q2, Q3, and Q4 transistors can be used. The drawback is a reduced drive capability (the final transistors are accordingly smaller), possibly one or two extra stages being necessary to drive a given load. These stages introduce additional delay.
- The second solution partially modifies the HDR circuit structure, and is shown in Fig. 5. Each gate is driven by an inverter, where MU and MD (see Fig. 5) are minimum size, and QU and QD are sized to obtain the desired threshold voltages, V_{M+} and V_{M-}. The role of the Q1, Q2, Q3, and Q4 transistors is assumed by QU and QD. The advantage is that QU and QD are only half the size of Q1, Q2, Q3, and Q4 to maintain the same threshold voltages, since Q1, Q2 and Q3, Q4 are serially connected transistors. If a minimum load at the insertion points is desired, then Q1, Q2, Q3, and Q4 are minimum size to represent a minimum load for QU and QD. Otherwise, Q1 and Q4 are sized larger for a higher drive capability of the buffer. QU and QD are accordingly larger. Note the role of the delay element in this configuration to resolve the output state until the nulling process of QU and QD is completed.

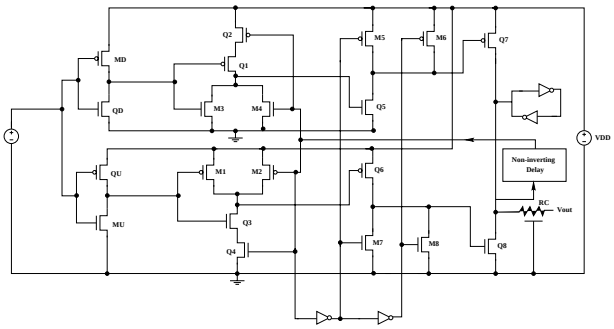

Fig. 5. The modified HDR circuit to reduce the load at specific insertion points.

The second solution obtains a minimal load at the insertion points. The drawback is that the nulling process [1] is performed by minimum size nulling transistors (MU and MD), limiting the input signal frequency (the nulling process must be completed before the next transition begins). If this condition is not satisfied, MU and MD must be increased in size. To maintain the same threshold voltages, the size of QU and QD are also increased. A situation is reached where the HDR circuit shown in Fig. 4 becomes more advantageous due to the double nulling transistors, M2 and M4 [1].

A large HDR delay can increase the total signal path delay, while an insufficient HDR output current would make the HDR ineffective when driving significant loads. Large Q1, Q2, Q3, and Q4 transistors would improve the threshold voltages, increase the output current, and decrease the delay but would increase the load of the line at the insertion points. The circuit shown in Fig. 5 ameliorates this problem. If the HDR delay is a significant portion of the total signal path delay, a two stage HDR, shown in Fig. 6, can be used to reduce the total delay. If both a minimum HDR delay and a minimum load at the insertion points are desired, a two stage HDR (shown in Fig. 6) combined with the circuit solution shown in Fig. 5 may be preferable.

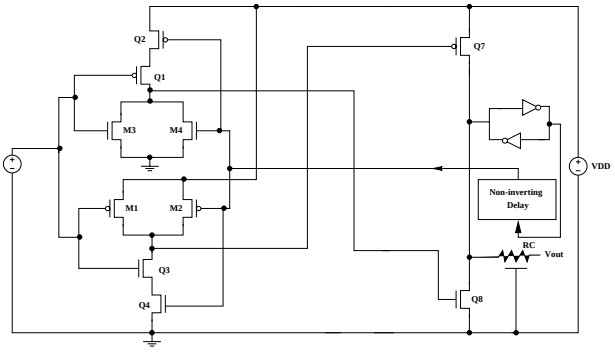

Fig. 6. A two stage HDR circuit to minimize the delay introduced in the signal path.

IV. Simulation Results and Performance Comparison

Circuit simulations based on Cadence-Spectre and a 1.2 μm CMOS technology are described in this section. The performance of the HDR circuit for different transistor sizes are compared in Table I. The HDR load in all cases is capacitive, assumed to be equal to 1 pF. The issues of interest for these simulations are the buffer threshold voltages, the intrinsic buffer delay, and the size of the output stage. If an RC load is used, the only node of interest is node 1 since it describes the intrinsic delay of the buffer (from the input to the output) which represents the delay introduced by the buffer in the signal path. The drive strength of the output stage of the buffer is approximatively equivalent [1] to the drive strength of an equally sized final stage of a cascaded tapered buffer.

TABLE I
Performance comparison for different HDR circuits with different transistor sizes

No.	Q1–Q2/ Q3–Q4 (μm)	V_{M+}/ V_{M-} (V)	Q5/Q6 (μm)	Final stage (μm)	Buffer delay (ns)
1	128/ 384	1.3/ 3.7	75/ 75	220/ 650	0.25
2	128/ 384	1.6/ 3.3	520/ 520	1700/ 5100	0.26
3	128/ 384	1.2/ 3.8	15/ 15	50/ 150	0.50
4	54/ 162	1.3/ 3.7	15/ 40	220/ 650	0.40
5	16/ 46	1.7/ 3.2	15/ 40	220/ 650	0.42

Cases 1, 2, and 3 of Table I refer to Fig. 4, while cases 4 and 5 refer to Fig. 5. Due to the size of the capacitive load (1 pF), all cases utilize a three stage configuration. Case 2 is sized to offer maximum drive strength (based on an $e = 2.7$ tapering criterion). Note the significant size of the final stage that permits the HDR to drive a much

larger load than 1 pF. Driving only a 1 pF load does not provide any speed advantage due to the delay introduced by stages 2 and 3. Due to the large size of Q5 and Q6, a decrease in the threshold voltages is observed. Case 3 demonstrates the other optimization, to obtain minimal threshold voltages by reducing Q5 and Q6 to a minimum size. However, due to the small size of the final stage, an increased buffer delay is noted. An extra amplifier stage provides additional drive strength (output current).

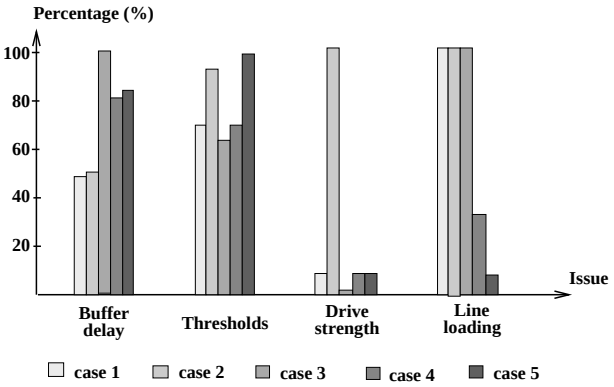

Fig. 7. A graphical comparison of the design tradeoffs of the different HDR circuit implementations according to Table I.

For cases 4 and 5, the sizes of Q1, Q2, Q3, and Q4 refer to QU–QD, and Q5–Q6 refer to Q1–Q4. Note for case 4 a reduction of the QU–QD sizes by more than a factor of two as compared to case 1, providing more than a factor of two reduction of the load at the insertion points. The final stage remains the same as in case 1, and the threshold voltages are approximately the same as in case 1. The HDR introduces a larger delay due to the extra inverters in the signal path, however, the load at the insertion points is substantially reduced. Case 5 is optimized for a close to minimal load at the insertion points. Note that the output stage has the same drive strength and the HDR has the same delay as case 4, while the threshold voltages are slightly increased. A graphical comparison of the relative performance of the different HDR implementations as listed in Table I for cases 1 to 5 is presented in Figure 7.

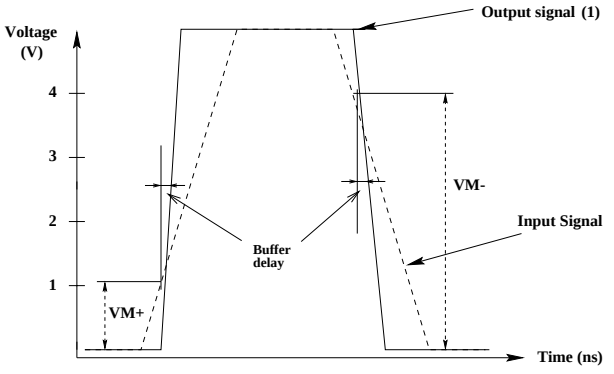

Fig. 8. A typical HDR response.

A typical HDR response is depicted in Fig. 8. Note the slow input signal transition, the HDR response at the V_{M+} and V_{M-} threshold voltages, and the sharp output waveform shape. The output transition time (for case 4) is 0.22 ns. Simulations based on a 0.8 μm CMOS technology in which the same transistor aspect ratio is maintained show an improvement in threshold voltages by up to 0.94 V (corresponding to the 1.2 V minimum listed in Table I) and a significant reduction in the delay introduced by the HDR.

The proposed circuits shown in Figs. 4, 5, and 6 permit slow input signals with a negligible penalty in short-circuit power. The actual dynamic power dissipation of the circuit can be optimized by considering multiple issues, such as the V_{M+} and V_{M-} threshold voltages, the number of stages, the transistor sizes, the magnitude and circuit implementation of the delay element, and other HD buffer related power optimization issues [1].

Preliminary simulations exhibit a gain in speed of 25% to 45% for a 0.1 KΩ, 10 pF RC line by inserting HDR circuits instead of classical inverting CMOS repeaters. A larger gain is estimated by using an optimal HDR circuit insertion methodology, similar to the insertion methodology developed in [9] for inverting repeaters.

V. Conclusions

An HDR circuit which exploits a VTC featuring low threshold voltages and hysteresis is proposed. The circuit exploits the advantages offered by the HD buffer [1]. Sizing considerations and design tradeoffs are also discussed. Several applications such as Schmitt triggers, where the HDR circuit restores the slow transition and distorted input signals with minimal speed penalty, as well as buffers that drive capacitive loads where up to a 30% power and a 500% area savings are obtained, are presented. The HDR circuit is suitable for use as a repeater to drive highly resistive RC lines, significantly decreasing the overall RC line delay in existing repeater insertion methodologies.

References

[1] R. M. Secareanu and E. G. Friedman, "A High Speed CMOS Buffer for Driving Large Capacitive Loads in Digital ASICs," *Proceedings of the IEEE ASIC Conference*, pp. 365–368, September 1998.

[2] H. C. Lin and L. W. Linholm, "An Optimized Output Stage for MOS Integrated Circuits," *IEEE Journal of Solid-State Circuits*, Vol. SC-10, No. 2, pp. 106–109, April 1975.

[3] N. Hedenstierna and K. O. Jeppson, "CMOS Circuit Speed and Buffer Optimization," *IEEE Transactions on Computer-Aided Design*, Vol. CAD-6, No. 2, pp. 270–281, March 1987.

[4] N. C. Li, G. L. Haviland, and A. A. Tuszynski, "CMOS Tapered Buffer," *IEEE Journal of Solid-State Circuits*, Vol. SC-25, pp. 1005–1008, August 1990.

[5] B. S. Cherkauer and E. G. Friedman, "A Unified Design Methodology for CMOS Tapered Buffers," *IEEE Transactions on VLSI Systems*, Vol. VLSI-3, No. 1, pp. 99–111, March 1995.

[6] B. S. Cherkauer and E. G. Friedman, "Design of Tapered Buffers with Local Interconnect Capacitance," *IEEE Journal of Solid-State Circuits*, Vol. SC-30, No. 2, pp. 151–155, February 1995.

[7] V. Adler and E. G. Friedman, "Repeater Design to Reduce Delay and Power in Resistive Interconnect," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, Vol. CAS II-45, No. 5, May 1998.

[8] V. Adler and E. G. Friedman, "Delay and Power Expressions for a CMOS Inverter Driving a Resistive-Capacitive Load," *Analog Integrated Circuits and Signal Processing*, Vol. 14, No. 1/2, pp. 29–39, September 1997.

[9] V. Adler and E. G. Friedman, "Repeater Insertion to Reduce Delay and Power in *RC* Tree Structures," *Proceedings of the Asilomar Conference on Signals, Systems, and Computers*, pp. 749–752, November 1997.

[10] S. Dhar and M. A. Franklin, "Optimum Buffer Circuits for Driving Long Uniform Lines," *IEEE Journal of Solid-State Circuits*, Vol. SC-26, pp. 151–155, January 1991.

[11] A. B. Grebene, *Bipolar and MOS Analog Integrated Circuit Design*. John Wiley & Sons, Inc., 1984.