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Thermal analysis of oxide-confined VCSEL arrays ☆

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ABSTRACT

A thermo-electric 3-D analysis of 980 nm vertical cavity surface emitting laser (VCSEL) arrays based on the finite element method (FEM) is presented in this paper. High performance VCSEL array structures with square mesas are modeled by applying a steady-state 3-D heat dissipation model. Several oxide aperture diameters (D_a), substrate thicknesses, current densities, array sizes, heat flux, and temperature profiles are considered. The analysis shows that the maximum internal temperature of a VCSEL array ranges from 306.5 K for a 20 μm D_a, 100 μm substrate thickness, 666 A/cm^2 current density, and a 1×1 array size to 412 K for a 5 μm D_a, 300 μm substrate thickness, 1200 A/cm^2 current density, and a 4×4 array size.

1. Introduction

DUE to small size, low divergence, non-astigmatic circular output beams, and inherent dynamic single longitudinal mode operation, vertical cavity surface emitting laser (VCSEL) arrays delivering optical energy are commonly applied in areas such as printing, engraving, sensors, and free-space data transmission [1–3]. However, given the small oxide apertures, relatively thick and low thermal conductive substrates, and the distributed Bragg reflectors (DBR), VCSEL structures are usually afflicted with severe thermal effects. Although a single VCSEL emitting a few milliwatts at room temperature has been demonstrated, large area VCSEL arrays emitting high output power beams producing significant heat have been developed [4,5]. Hence, understanding the thermal behavior of VCSEL arrays is crucial, since the heat limits device performance, optical output power, threshold current, modulation speed, as well as the efficiency of the heat sink.

A number of research teams have modeled VCSEL thermal effects. The accuracy of these models is different and depends upon the tradeoff among flexibility, precision, and simulation runtime [6–19]. However, although existing work has successfully modeled a VCSEL, there is significant inaccuracy in these models: some researchers only investigated 2-D structures [6–14]; while other researchers only consider a single VCSEL, not an oxide-confined VCSEL array [15–19], or use simple physical parameters [14,16]. In addition, early work on VCSEL arrays focused on "etched-well" VCSELs, which are significantly different from the modern oxide-confined VCSELs considered in this paper [20]. However, since the size of the arrays directly determines the quantity of heat and thermal distribution, and VCSEL arrays comprise different layers of materials in both the lateral and vertical directions, a physical-based 3-D simulation model is preferable in providing useful insight.

A commercial software tool COMSOL based on the finite element method (FEM) provides an appealing approach to accurately analyze the thermal behavior of VCSEL arrays [14,17–19,21]. COMSOL considers the material properties, mesh density at different locations, and irregularly shaped structures such as polyhedral domains and multi-lateral boundaries, while providing flexible control over the accuracy, memory, and computational time [17].

Based on the FEM, different size VCSEL arrays with several oxide aperture diameters (D_a), substrate thicknesses, and current densities are investigated in this paper. These parameters are used to obtain a precise thermal distribution.

The paper is organized as follows: In Section II, the material and thickness of each layer within the VCSEL structure are described. The physical characteristics of the materials and a model of the VCSEL arrays are discussed in Section III. Based on the simulation analysis, the effects of different parameters on the internal temperature are described in Section 4. Several concluding remarks are provided in the final section of this paper.

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2. VCSEL array structures

A 980 nm intra-cavity contacted oxide aperture VCSEL array with AlAs/GaAs DBR mirrors is investigated. A schematic diagram of the VCSEL structure is shown in Fig. 1. The thick top DBR and bottom DBR determine the active device. The substrate is also included in the figure. The intra-cavity contact improves the speed characteristics of the device. The two metal square loops connect above and below the active region of the quantum-well through the heavily doped (p++ and n++) GaAs contact layers. The doping concentration of the p++ and n++ contact layers are, respectively, $5\times10^{18}$and 3×10^{18} cm^{-3}. Each contact layer is 208.6 nm thick and is sandwiched between the DBR mirrors and the AlAs layers. This structure has both electrical and optical advantages. The vertical current injection path is reduced by as much as 90% without passing through the thick layer of the AlAs/GaAs mirrors. The two 83.8 nm AlAs lateral oxide layers shape the optical aperture and encapsulate the active region to reduce the threshold current while improving the quantum efficiency of the VCSEL. The active region is composed of three 8 nm $In_{0.2}Ga_{0.8}As$ quantum wells (QWs) and four 10 nm GaAs barrier layers, which is covered by two 116.8 nm thick $Al_{0.5}Ga_{0.5}As$ spacer layers. The total thickness of the core is about one third of a wavelength, ~300 nm. In addition, since no current flows through the DBR mirrors during laser operation, the mirrors are left undoped, which minimizes optical absorption and carrier scattering inside the mirror region. Note that the total thickness of the active region, aperture layers, and contact layers are one wavelength, about 980 nm.

A top view of the VCSEL is shown in Fig. 1(b). The VCSEL is typically designed with a circular or square aperture. In this case, anisotropic oxidization of AlAs produces a non-circular aperture despite the circular active region mesa [22]. A square mesa is therefore employed rather than aligning the sides with the ⟨1 0 0⟩ crystal axes, which has a higher oxidation rate than the ⟨1 1 0⟩ direction. Correspondingly, the top mirror, active region (square mesa), and internal device area (without the N++ metal contact) are 20×20, 40×40, and 60×60 μm^2, respectively. The minimum pitch size for the VCSEL arrays is equivalent to two times the width of the active area, and is therefore 80 μm. Also shown in Fig. 1(b) is the 2 μm space between the metal to the P++ contact and the top mirror sidewall to avoid metal contamination of the top mirror, and the 10 μm space between the metal contacts to facilitate the lift-off process.

The top and bottom DBR mirrors consist of an alternating sequence of high refractive index layers—GaAs (84 nm), and low refractive index layers—AlAs (70 nm). The total number of AlAs/GaAs pairs on the top and bottom layers are 22 and 25, respectively. The reflectivity of the top and bottom mirrors is, respectively, 98.8% (top) and 99.7% (bottom), based on (1–(3) [23,24],

$$R_{t,b}=\left(\frac{1-b_{t,b}}{1+b_{t,b}}\right), \tag{1}$$

$$b_t=\frac{n_{air}}{n_{GaAs}}\left(\frac{n_{AlAs}}{n_{GaAs}}\right)^{2Mt}, \tag{2}$$

$$b_b=\frac{n_{air}^2}{n_{air}n_{GaAs}}\left(\frac{n_{AlAs}}{n_{GaAs}}\right)^{2Mb}, \tag{3}$$

where $R_{t,b}$, n_{air}, n_{GaAs}, n_{AlAs}, Mt, and Mb are, respectively, the top and bottom mirror reflectivity, material reflectivity index of air, material reflectivity index of GaAs, material reflectivity index of AlAs, and top and bottom mirror layer pairs at peak reflectivity. The layer thicknesses d_{GaAs} and d_{AlAS} *are* [23]

$$d_{GaAs,AlAs}=\lambda_B/4n_{GaAs,AlAs}, \tag{4}$$

where λ_B is the Bragg wavelength.

To accurately determine the threshold gain G_{th}, the losses within the mirror and active region, and the mirror reflectivity must be considered. The gain is compensated for these losses within the cavity. In the threshold condition, the gain enhancement and penetration of the waves into the Bragg reflectors are described by G_{th} [23]

$$G_{th}=\alpha_a+\frac{1}{\Gamma_r d_a}\left[\alpha_i(L_{eff}-d_a)+\ln\frac{1}{\sqrt{R_tR_b}}\right], \tag{5}$$

where Γ_r, d_a, L_{eff}, R_t, R_b, α_i, and α_a are, respectively, the gain enhancement factor, total thickness of the active layers, effective mirror length, intensity reflection coefficients for the top and bottom mirrors, intrinsic losses in the passive section, and intrinsic losses in the active section. In most simple cases, R_t and R_b are determined from (1). The intrinsic losses in the active region do not contain band-to-band absorption, which is included in the optical gain of the active region. The value of these parameters are listed in Table 1.

Alternatively, when considering losses, the threshold condition can be formulated using the maximum reflectivity, expressed as [23]

$$R_\alpha=R_{t,b}\exp(-2\alpha_i l_{eff})\approx R_{t,b}(1-2\alpha_i l_{eff}), \tag{6}$$

where l_{eff} is the penetration depth for lightly doped AlAs and GaAs layers in the top and bottom mirrors, and the losses are much

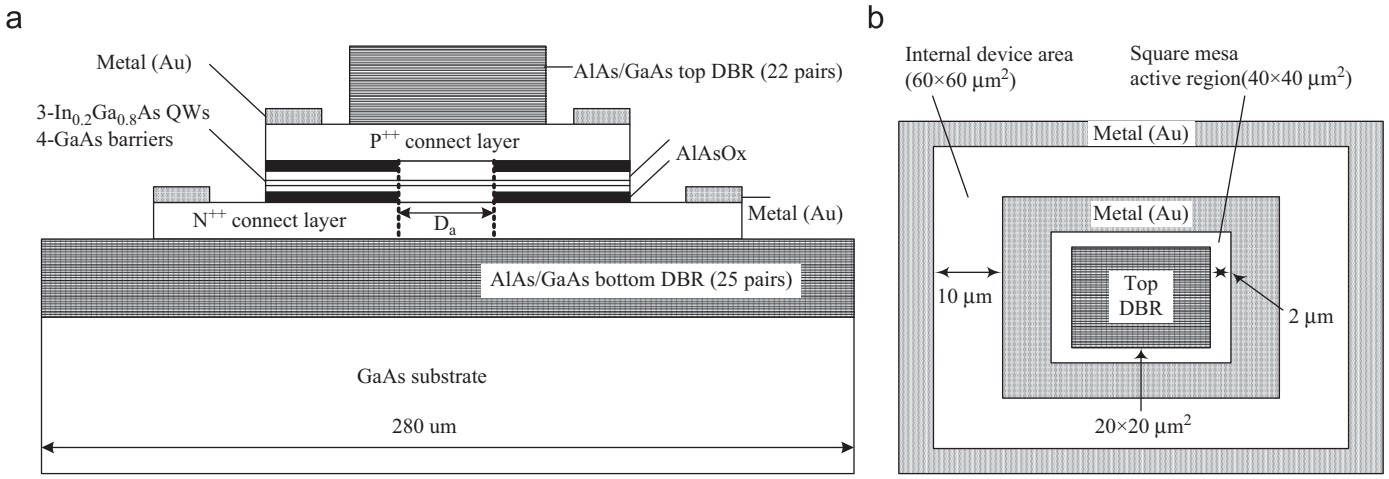

Fig. 1. Schematic diagram of VCSEL structure: (a) side view and (b) top view.

Table 1
Parameters used to calculate the threshold gain g_{th}.

Parameter	Value
Γ_r	1.8
d_a	24 nm
α_i	20 cm^{-1}
α_a	20 cm^{-1}
L_{eff}	1.3 μm
R_t	0.984
R_b	0.995

smaller, $2\alpha_i l_{eff} \ll 1$. The mirror reflectivity therefore does not change substantially.

From (1)–(6), G_{th} of the triple QW active region is 2500 cm^{-1}. The losses of the mirrors at 980 nm are low (10 cm^{-1}). The threshold current density J_{th} is exponentially dependent on the gain threshold and inverse exponentially dependent on the material gain G_0 [25],

$$J_{th} = \frac{n_w J_0}{\eta_i} \exp\left(\frac{G_{th}}{G_0}\right), \tag{7}$$

where J_0, η_i, and n_w are, respectively, the transparency current density, internal quantum efficiency, and number of wells. J_0 and G_0 are ~90 A/cm^2 and 2400 cm^{-1}, respectively, for an 8 nm thick $In_{0.2}Ga_{0.8}As$/GaAs layer emitting at 980 nm [26]. Based on these parameters, J_{th} is 666 A/cm^2.

3. VCSEL array model

VCSEL arrays are characterized with D_a equal to 5, 10, 15 and 20 μm, substrate thicknesses of 100, 200 and 300 μm, and array sizes ranging from 1×1 to 4×4. The thermal computation utilizes a steady-state three-dimensional heat dissipation model, from which a thermal distribution profile is generated. This profile depends upon the size of the simulation domain; since, the heat can originate from a single or multiple hot spots and can spread across the much larger substrate. If thermal spreading is minimal, the ambient temperature will rapidly rise. Each side of the square substrate is therefore sized as large as L_S=280 μm [18]. The basic steady-state 3-D heat dissipation models are [27,28]

$$-\nabla(k\nabla T) = Q, \tag{8}$$

$$k\nabla T = q_0 + h(T_{inf} - T) + \varepsilon\sigma(T_{amb}^4 - T^4), \tag{9}$$

where Q, k, T, q_0, h, ε, σ, T_{inf}, and T_{amb} are, respectively, the heat source density, thermal conductivity, initial temperature (assumed to be 298 K), inward heat flux, heat transfer coefficient, emissivity of the surface, Stefan–Boltzmann constant, ambient bulk temperature, and temperature of the surrounding radiation environment. The heat produced by the active region within the VCSEL arrays is transferred from the device to the environment through primarily two means: via the GaAs substrate to a copper heat sink by conduction, as modeled by (8); and convection and radiation through the top electrodes, as modeled by (9). Since the device contacts directly to the copper heat sink, and one end of the heat sink is assumed to be at room temperature (about 298 K), the heat is mostly released by conduction, and convection and radiation are assumed negligible [18].

The VCSEL arrays are composed of multilayer thin film structures, which results in many internal and external boundary interfaces. The thermal boundary resistance (TBR) generated by these interfaces reduces the thermal conductivity of the material. This issue is known as interface phonons [29]. These interface phonons increase scattering and reduce the overall thermal resistance of the VCSEL arrays [30,31]. However, there is currently a lack of understanding regarding the effect of the phonons on the interface. In this paper, to obtain the effective thermal conductivity with anisotropy, the lateral and vertical thermal conductivities are determined from the following two expressions [32],

Table 2
Thermal conductivity of composite materials in VCSEL arrays mounted on a copper heat sink [18,19, 35–38].

Layer	Material	TC (W/m K)
p^- contact metal	Au	315
Top DBR	AlAs/GaAs	k_L=32, k_V=29
P^{++} connect layer	GaAs	44
Oxidation	AlAs	0.7
Spacer layer	$Al_{0.5}Ga_{0.5}As$	11
3 MQW	$In_{0.2}Ga_{0.8}As$ (well)/ GaAs (barrier)	k_L=29, k_V=14
Spacer layer	$Al_{0.5}Ga_{0.5}As$	11
Oxidation	AlAs	0.7
N^{++} connect layer	GaAs	44
Bottom DBR	AlAs/GaAs	k_L=32, k_V=29
Substrate	GaAs	44
n^- contact metal	Au	315

TC: thermal conductivity.

$$k_L = \frac{d_1 k_1 + d_2 k_2}{d_1 + d_2}, \tag{10}$$

$$k_V = \frac{d_1 + d_2}{d_1/k_2 + d_2/k_1}, \tag{11}$$

where k_L, k_V, k_1 (k_2), and d_1 (d_2) are, respectively, the lateral thermal conductivity, vertical thermal conductivity, thermal conductivity, and thickness for layer 1 (layer 2).

In VCSEL arrays, both the AlAs/GaAs DBR regions and the InGaAs/GaAs QW regions comprise many multilayer structures [33,34]. To achieve greater accuracy in these regions, k_L and k_V in the lateral and vertical directions, respectively, are determined from simulation. As for the layers, except for the QW and DBR regions, isotropic thermal conductivity (k=k_L=k_V) is assumed. The thermal conductivity of the different materials in the VCSEL arrays attached to the copper heat sink is listed in Table 2 [18].

4. Simulation results and analysis

The heat flux and temperature distribution in the lateral direction for 3×4 and 1×1 VCSEL arrays are shown in Fig. 2. From this figure, since the VCSEL arrays are bonded with a copper heat sink below the bottom DBR and GaAs substrate, heat conducts radially from the heat sources through the substrate to the heat sink. The maximum internal temperature induced by the heat generated inside the device are 321 K for a 3×4 VCSEL array, and 306.8 K for a 1×1 VCSEL array, assuming the heat sink is initially at room temperature, 298 K. As the size of the VCSEL array increases, each individual VCSEL contributes heat that accumulates in the device body, increasing the maximum internal temperature. The four VCSELs in the cross-sectional slice with the two center VCSELs are also shown in Fig. 2(a) and exhibit a higher maximum internal temperature. The higher temperature is due to the smaller temperature difference between the center VCSELs and the surrounding material. These center VCSELs are surrounded by other VCSELs that also generate heat and produce a smaller temperature gradient.

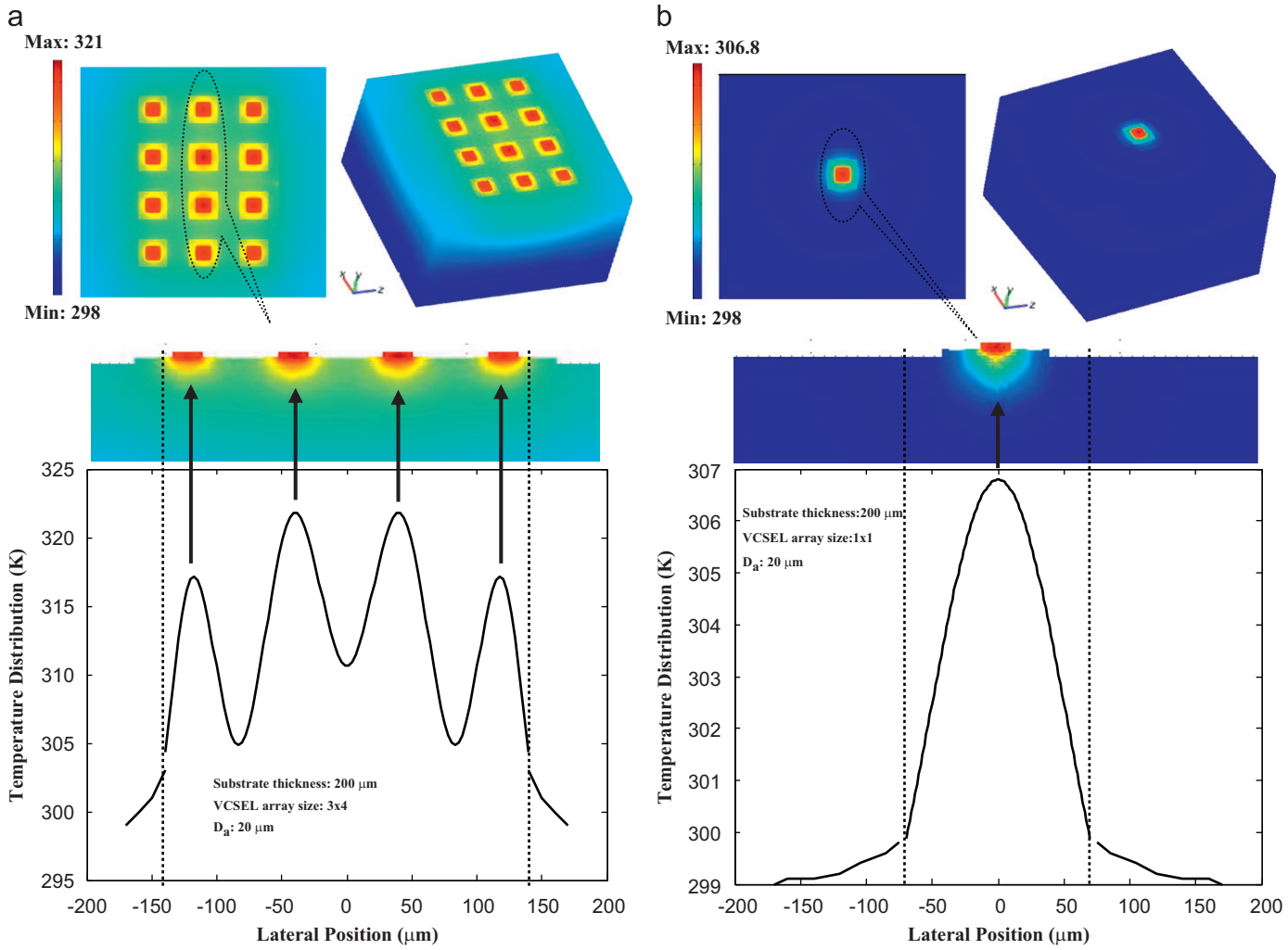

Fig. 2. Heat flux and temperature distribution in lateral direction for (a) 3×4 VCSEL array and (b) 1×1 VCSEL array.

The maximum internal temperature as a function of the oxide aperture diameter (D_a), current density, and VCSEL array size is depicted in Fig. 3. Note that the heat source density increases with a decrease in D_a. The reason is that the oxide layer adjacent to the heat generation region extends over a larger area, preventing the generated heat from spreading [18]. Thus, for the example shown in Fig. 3(d) with a 300 μm substrate, as D_a decreases from 20 to 5 μm, the maximum internal temperature difference is about 9 K for a 1×1 VCSEL array, and reaches 40.5 K for a 4×4 VCSEL array.

As illustrated in Fig. 3, the maximum internal temperature also depends significantly on the substrate thickness. The VCSEL array with a substrate thickness of 300 μm exhibits a higher maximum internal temperature as compared to substrates with a 100–200 μm thickness. This characteristic can be attributed to the long thermal path from the QW and DBR regions through the thick substrate to the heat sink. For the example shown in Fig. 3(a), where D_a=20 μm and J_{th}=666 A/cm^2, the substrate thickness varies from 100 to 300 μm, ∇T increases by 4 K for a 1×1 VCSEL array, and increases by 25 K for a 4×4 VCSEL array. This behavior indicates that VCSEL arrays formed by the bottom emitting VCSEL and epi-layer bonding scheme with a thin substrate are expected to exhibit a lower thermal resistance due to the shorter transfer path between the heat source and heat sink.

The current density also affects the internal temperature of the VCSEL arrays. The internal temperature dependence on the injection current is [18,39]

$$T_{int} = T_{hs} + R_{th}(VI + R_s I^2 - P_{opt}), \tag{12}$$

where T_{int}, T_{hs}, R_{th}, R_s, V, I, and P_{opt} are, respectively, the internal temperature, heat sink temperature, thermal resistance (K/W), series resistance (Ω), forward voltage, injection current, and optical output power. The R_s resistive term is an electrical parameter given in ohms, while R_{th} is a thermal resistance in Kelvins per watt. According to (12), the maximum internal temperature increases with higher injection current. A VCSEL array with a narrow D_a experiences a significant rise in temperature caused by an increase in the injection current, leading to poor heat dissipation and internal heating. Accordingly, at an injection current density of 1200 A/cm^2, ∇T is 115 K for a D_a=5 μm, a 300 μm substrate thickness, and a 4×4 VCSEL array. ∇T is only 86 K when the injection current is decreased to 666 A/cm^2 for the same parameters, as illustrated in Figs. 3(a) and (d).

In summary, the maximum internal temperature of intra-cavity contacted oxide aperture VCSEL arrays is affected by many factors including the aperture and array size. The maximum internal temperature is lower with decreasing current density. It is also worth noting that a thicker substrate can further degrade the thermal characteristics of the device due to an increase in the thermal resistance.

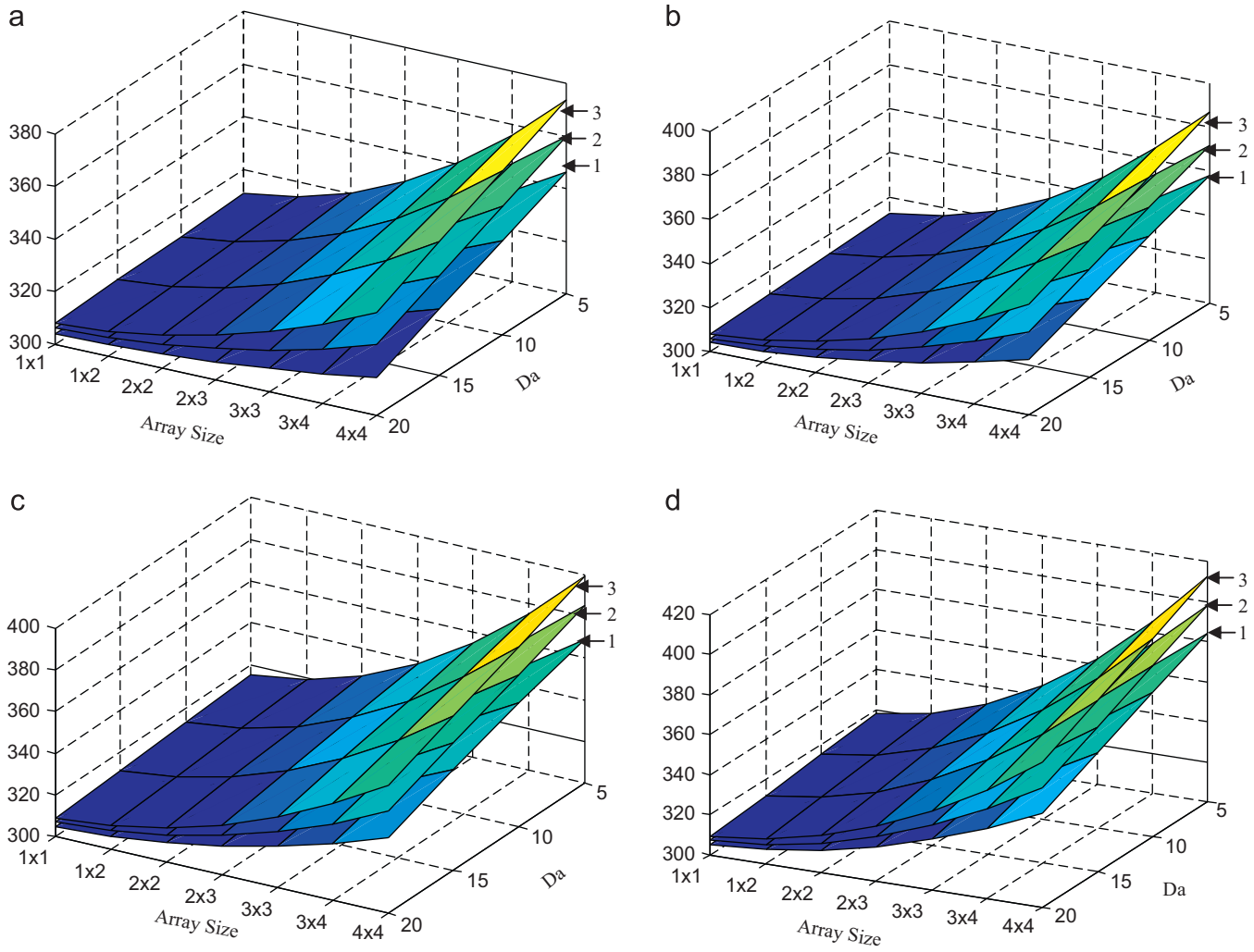

Fig. 3. Maximum internal temperature for several D_a, VCSEL array sizes, and current densities, (a) J=666 A/cm^2, (b) J=800 A/cm^2, (c) J=1000 A/cm^2 and (d) J=1200 A/cm^2 1: 100 μm substrate thickness; 2: 200 μm substrate thickness; 3: 300 μm substrate thickness.

5. Conclusions

Complex VCSEL arrays are modeled and the thermo-electrical behavior is analyzed, describing the heat flux and temperature distribution. These results indicate that the maximum internal temperature of intra-cavity contacted oxide aperture VCSEL arrays depends strongly on the oxide aperture diameter, array size, current density, and substrate thickness. The oxide aperture diameter, array size, and injection current determine the magnitude of the generated heat; a thinner substrate reduces the physical distance to the heat sink. The maximum internal temperature of the VCSEL arrays can range from 306.5 K for a 20 μm D_a, 100 μm substrate thickness, 666 A/cm^2 current density, and 1×1 array size to 412 K for a 5 μm D_a, 300 μm substrate thickness, 1200 A/cm^2 current density, and 4×4 array size. To the authors' knowledge, this work is the first investigation on the thermal properties of oxide-confined VCSEL arrays.

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