Microelectronics Journal 126 (2022) 105336

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

Inductive noise coupling in multilayer superconductive ICs☆

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ARTICLE INFO

Keywords:
Single flux quantum
Superconductive integrated circuits
Superconductive digital electronics

ABSTRACT

Superconductive cryogenic circuits are an emerging energy efficient technology that can replace or supplement existing CMOS VLSI systems. State-of-the-art superconductive circuits utilize more than ten niobium layers for the logic circuits and interconnect. Multiple sources of inductive coupling noise exist within these systems. In this paper, these inductive noise sources are evaluated and the effects of coupling noise are discussed. In particular, the effects of coupling noise within passive transmission lines, where the magnitude of the data signals is unusually small, are characterized and discussed. The effects of the bias current coupling to the inductors within the logic gates are also described, as the gates require accurate bias conditions. Guidelines to manage the deleterious effects of coupling noise are provided.

1. Introduction

Rapid single flux quantum (RSFQ) is a promising superconductive electronics technology which has recently been considered as an energy efficient alternative to conventional CMOS circuits in stationary, high performance, large scale computing systems [1,2]. Advances in niobium-based technology [3] and automated design tools [4,5] are necessary to enable SFQ-based VLSI superconductive systems. These systems dissipate extremely low power (on the order of 10^{-19} Joules per bit [1]) while operating at clock frequencies up to hundreds of gigahertz [6].

State-of-the-art superconductive niobium-based fabrication technologies support over ten metal layers [3]. A large fraction of these niobium layers, however, is used by the active parts of the circuit; only a few layers are available for routing.

VLSI complexity RSFQ circuits primarily utilize interconnect based on passive transmission lines (PTL) for routing data and clock signals among standard cells [7,8]. This type of interconnect consists of a driver/receiver circuit and a stripline or microstripline [9]. PTL interconnect poses unique challenges on the automated routing process, as the available metal resources are significantly limited. Alternative routing topologies have been proposed to reduce the number of metal layers required by the interconnect structures [10,11]. These different topologies, however, increase the coupling noise among adjacent striplines as compared to topologies with additional ground planes.

Mitigation and modeling of interconnect coupling is an important issue in modern VLSI circuits, and an active area of research, particularly in beyond-CMOS technologies [12,13]. In this paper, issues related to inductive coupling noise in multilayer superconductive ICs are discussed, and approaches to characterize and mitigate this coupling noise in superconductive systems are proposed (see early work in [14]). This work also considers inductive coupling of bias currents between the bias lines and logic gates.

This paper is organized as follows. The primary sources of inductive coupling noise are described in Section 2. Inductive coupling noise in common circuit structures is characterized in Section 3. The effects of inductive coupling noise on circuit behavior and related mitigation guidelines are presented in Section 4. The paper is concluded in Section 5.

2. Sources of inductive coupling noise

Multiple sources of coupling noise exist in multilayer ICs, as shown in Fig. 1. PTL striplines are the primary structure for routing data and clock signals in large scale RSFQ circuits [7]. Single flux quantum (SFQ) pulses propagating along these lines can inductively couple to other lines, producing coupling noise. This inductive noise can produce incorrect switching [15] and reduced parameter margins [16]. These noise sources are introduced in this section. In Section 2.1, sources

☆ The effort depicted is supported by the Department of Defense Agency – U.S. Intelligence Advanced Research Projects Activity (IARPA) through the U.S. Army Research Office under Contract No. W911NF-17-9-0001. The content of the information does not necessarily reflect the position or the policy of the Government, and no official endorsement should be inferred.

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https://doi.org/10.1016/j.mejo.2021.105336
Received 9 June 2021; Received in revised form 3 December 2021; Accepted 6 December 2021
Available online 25 April 2022

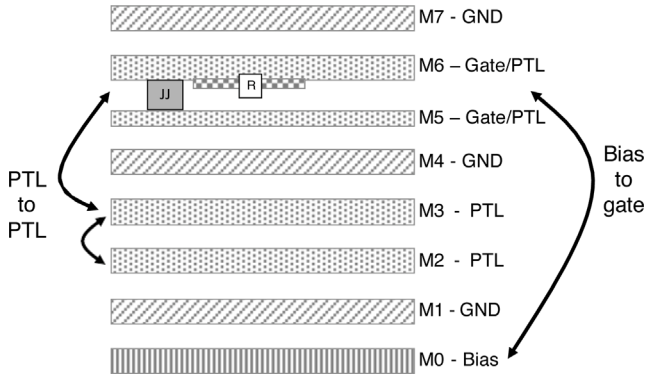

Fig. 1. Sources of inductive coupling noise in a superconductive IC (MIT LL SFQ5ee process [17]).

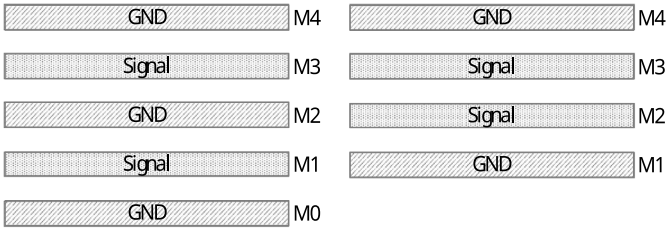

Fig. 2. Organization of metal layers for two PTL routing topologies, (a) three ground planes [11], and (b) two ground planes [10].

of inductive coupling noise in PTL interconnect lines are described. In Section 2.2, inductive coupling of bias current in logic gates is discussed. In Section 2.3, techniques and tools to evaluate inductive coupling noise are introduced.

2.1. PTL noise coupling

Metal resources are limited in superconductive fabrication technologies [17]. Modern niobium fabrication facilities only provide up to ten niobium layers, where the Josephson junctions (JJs) are placed between specific layers. Several of these layers are occupied by the junctions and related gate level connections, reducing the available metal resources for routing [10]. A stripline within a PTL ideally consists of a signal line sandwiched between two ground planes. This topology is however impractical for VLSI circuits.

Two alternative topologies exist to reduce the number of layers used for routing, as shown in Fig. 2. One topology uses a shared ground plane between two PTLs [11], as shown in Fig. 2(a). Five metal layers are used to produce two routing layers. Another topology utilizes an asymmetric stripline, where two signal layers are sandwiched between two ground planes [10], as depicted in Fig. 2(b). For each signal metal layer in this topology, the separation between the ground planes and therefore the thickness of the dielectric layers are different. No ground plane exists between these signal layers. This approach requires four niobium layers to produce two routing layers. These alternative topologies affect the mutual inductive coupling between striplines.

2.2. Coupling of bias current

The bias lines in the MIT LL SFQ5ee process [17] are usually placed along the edges (top or bottom) of the metal stack to reduce inductive coupling of the bias current to the sensitive RSFQ gates. Despite this technique, inductive coupling occurs in these structures. High current within the bias lines can affect the operation of the circuits despite a small mutual inductance. In addition, in certain topologies of the bias tracks, the bias lines are located close to the PTL interconnect. This proximity can also couple noise into the interconnect.

Table 1
Comparison of mutual inductance extracted in FastHenry with experimental data. The experimental data and layout topology are based on [19].

Layers	Experimental M, pH	FastHenry M, pH	Difference	Experimental standard deviation
M0-M1-M2-M7	3.37	3.58	+6.2%	1.12%
M1-M2-M3-M7	3.27	3.30	+0.9%	0.90%
M2-M3-M4-M7	3.04	3.13	+3.0%	2.04%
M3-M4-M5-M7	2.75	2.94	+6.9%	2.89%
M4-M5-M6-M7	1.95	1.89	−3.2%	1.43%

2.3. Techniques for coupling evaluation

Inductance extraction tools are used to characterize the magnitude of the coupling noise. Field solvers are necessary to extract the inductive characteristics of these complex multilayer structures. FastHenry [18] is a commonly used and relatively accurate open source tool for inductance extraction of superconductive circuits. The inductance estimates can be used as guidelines for automated routing tools and for the design of standard cells. In the following sections, the magnitude and characteristics of inductive coupling noise are evaluated to determine effective noise mitigation guidelines for different circuit topologies.

3. Inductive coupling within common circuit structures

The topology of an IC layout is limited by the design rules of the fabrication process. In a standard cell-based design flow, specific layout structures are common or ubiquitous. In this section, the inductive noise characteristics of these common circuit structures are evaluated.

3.1. Existing experimental data

To verify the correctness and relative error of the inductance extracted with FastHenry, a comparison with experimental data is useful. In this section, the extracted self-inductance and mutual inductance are compared to published experimental results.

The self-inductance of different structures in the MIT LL SFQ5ee process [17] is relatively well characterized. The self-inductance is determined in FastHenry by attaching a port to the input signal and ground planes while shorting the output signal to ground. The self-inductance of different structures, extracted in FastHenry, is compared here to experimental data. These self-inductances are in close agreement – the error is on the order of 5%, sufficient for evaluating inductive noise.

Available experimental data on the mutual inductance in the SFQ5ee process are limited. The mutual inductance in the SFQ5ee process has been experimentally measured as part of the InductEx tool calibration process [19]. Extraction of the mutual inductance in FastHenry is similar to extraction of the self-inductance – an additional port is attached to the second inductor. In Table 1, the inductance extracted from FastHenry is compared to the experimental mutual inductance. These inductances are within 6.9% – in sufficient agreement to support coupling noise analysis.

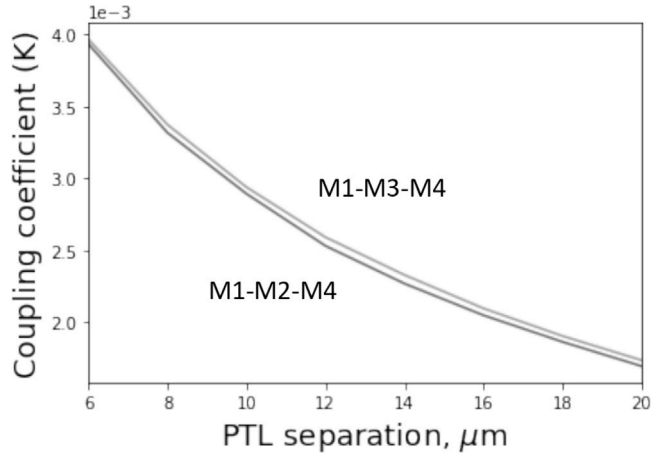

Fig. 3. Coupling between two identical parallel PTLs within the same layers with signal lines in M2 and M3.

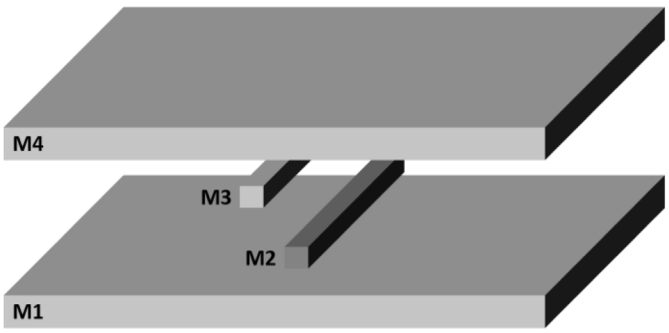

Fig. 4. Two identical parallel PTLs in adjacent layers with signal lines in M2 and M3.

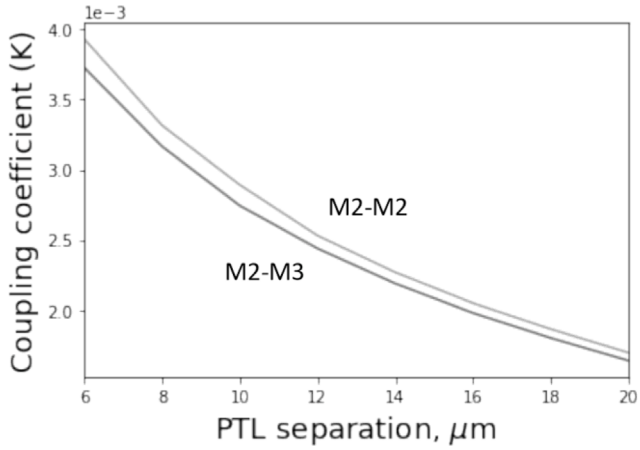

Fig. 5. Coupling between two identical parallel PTLs in adjacent layers with signal lines in M2 and M3.

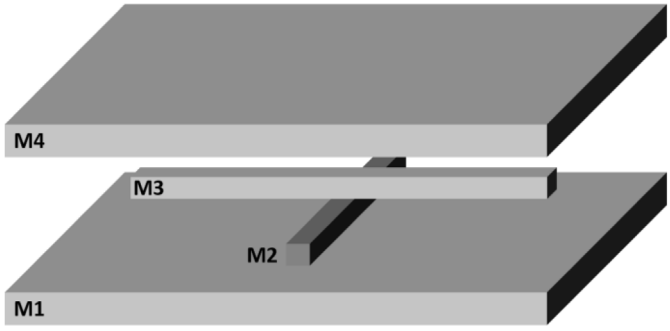

Fig. 6. Two perpendicular PTLs in adjacent layers with signal lines in M2 and M3.

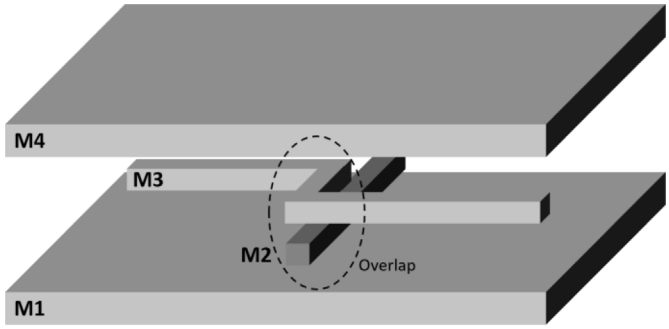

Fig. 7. Two perpendicular PTLs in adjacent layers with signal lines in M2 and M3 with a short overlap.

3.2. Coupling between parallel PTL lines

In this section and the following sections, the PTL topology shown in Fig. 2(b) is evaluated. The width of the PTL signal lines is assumed to be 5.2 μm, while the ground planes are in M1, M4, and M7.

Parallel PTL lines in close proximity typically exhibit the largest inductive coupling coefficient, on the order of 10^{-2} for narrowly spaced lines. The dependence of this coupling coefficient on the signal line separation is depicted in Fig. 3 for two M1-M3-M4 PTLs or two M1-M2-M4 PTLs. These striplines share the same M1 and M4 ground planes. The coupling coefficient exponentially depends upon the separation between the signal lines. This structure is ubiquitous in RSFQ circuits. Although the increased separation between PTL tracks reduces coupling, a tradeoff exists between the spacing between striplines and the routing congestion.

For PTL striplines in adjacent layers sharing the same ground planes, the dependence of the coupling coefficient on the separation between layers is similar. For the topology depicted in Fig. 4 (PTLs in M1-M2-M4 and M1-M3-M4), this dependence is illustrated in Fig. 5. Any additional vertical separation between these lines slightly reduces the inductive coupling noise.

Inductive coupling between PTLs separated by a ground plane, *e.g.* M4-M5-M7 and M1-M3-M4, is drastically reduced by approximately an order of magnitude. Vias connecting the ground planes of a stripline (stitching vias, *e.g.*, M1 and M4 in Fig. 5) further reduce the inductive coupling. A vertical overlap between striplines in adjacent layers (as shown in Fig. 7) significantly increases the coupling coefficient in proportion to the area of the overlap (or crossover).

3.3. Coupling between perpendicular PTL lines with and without overlap

To reduce inductive noise in PTLs in adjacent layers, the routing tracks in these layers can be arranged in perpendicular directions, as shown in Fig. 6 for PTLs in M1-M3-M4 and M1-M2-M4. This structure negates any practical effect from adjacent layer coupling – the coupling coefficient is two orders of magnitude smaller than the parallel case.

In a layout with constrained routing resources, some PTLs in adjacent layers may require a short overlap to reduce routing congestion. This case is evaluated for the structure shown in Fig. 7 – perpendicular PTLs in M1-M3-M4 and M1-M2-M4. The dependence of the coupling coefficient on the width of the overlap is depicted in Fig. 8. The zero on the horizontal axis corresponds to a simple crossing of perpendicular lines, while the larger offset is the length of the additional overlap. The coupling coefficient linearly depends upon the width of the overlap.

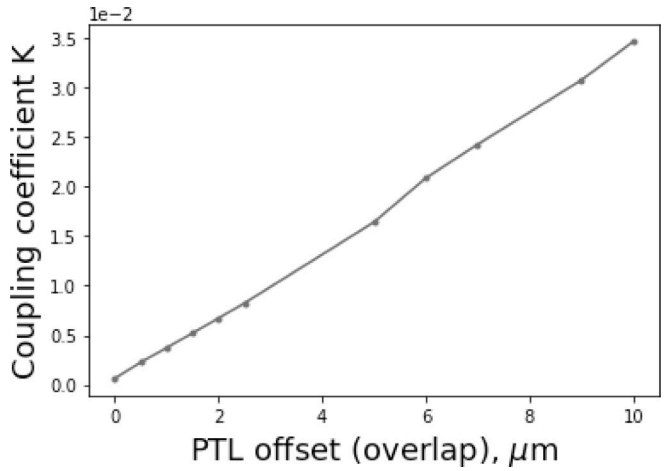

Fig. 8. Coupling between two perpendicular PTLs in adjacent layers with signal lines in M2 and M3 with a short overlap (see Fig. 7).

3.4. Coupling between M0 bias lines and logic gates

In the topology shown in Fig. 1, the bias lines are routed in M0. Unlike PTL lines that carry small voltage signals, these bias lines carry relatively high current, which can couple to the inductors within the sensitive RSFQ gates (*e.g.*, in M5 and M6). This coupling is however reduced by the presence of two ground planes – M1 and M4 – between the gates and bias lines.

Parasitic coupling to the RSFQ gate inductors depends upon the shape and relative position of the inductors. A critical practical case is assumed here – a long (~22 μm) and narrow (~0.5 μm) straight inductor in M5 with an inductance of ~8.5 pH (a typical inductance of a storage loop within a DFF). Cell libraries typically utilize more compact inductor geometries which exhibit a smaller coupling coefficient. A wider and longer inductor produces a higher coupling coefficient. This structure is however highly inefficient in terms of gate area and is therefore not a practical geometry.

From FastHenry simulations, the approximate inductive coupling coefficient between the M0 bias lines and M5 gate inductors is on the order of 10^{-4} if the inductors overlap in the vertical dimension. This coupling coefficient is reduced to 10^{-5} if the inductors do not overlap. Although small, this coupling can affect circuit operation due to the high current within the bias lines.

4. Mitigation guidelines

Different circuit structures exhibit a different sensitivity to inductive coupling noise, producing different types of errors. In this section, the effects of inductive noise on circuit operation are described for PTLs and logic gates in, respectively, Sections 4.1 and 4.2.

4.1. Effects of PTL noise coupling

An SFQ pulse traveling on an active (aggressor) PTL produces a transient current spike at the receiver of the passive (victim) line, as depicted in Fig. 9. Two cases are considered here, a small coupling coefficient (~0.01) and a large coupling coefficient (~0.4). The case of a large coupling coefficient corresponds to long distance, overlapping PTL striplines in adjacent layers. The case of a small coupling coefficient corresponds to other practical interconnect topologies, where the overlap between striplines is small.

The effects of inductive coupling noise on circuits are evaluated in WRSPICE [20]. WRSPICE does not normally support coupled transmission lines: therefore, a decoupling technique for lossless transmission lines is used [21].

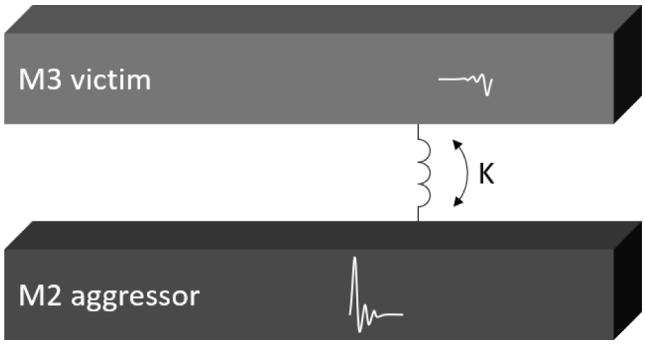

Fig. 9. Inductive coupling between parallel PTLs. Note the aggressor and victim lines.

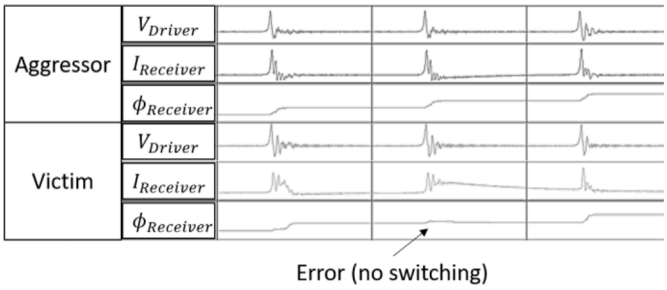

Fig. 10. Error in signal transmission (absence of switching) produced by significant coupling ($K = 0.5$) between the aggressor and victim lines.

In the case of small inductive coupling, additional current at the receiver of the victim PTL is on the order of a few μA – negligible as compared to the bias current of a typical PTL receiver. In this case, the transient coupling noise momentarily reduces the parameter margins of the receiver when this parasitic current is present. The degradation in margins does not exceed a few per cent.

In the case of significant coupling, the coupled current at the receiver of the victim line can exceed tens to hundreds of μA. This large noise current is typically insufficient to switch the JJ within the receiver of the victim PTL. If, however, this coupled noise waveform coincides with the signal waveform on the victim line, this current can prevent the JJ in the receiver from switching, as shown in Fig. 10. Unless the data signals on the aggressor and victim lines are synchronized to different phases of the same clock signal, this condition will eventually produce an error. To mitigate the effects of inductive coupling noise in PTLs, the routing algorithm should avoid long overlapping striplines in adjacent layers.

4.2. Effects of bias current coupling

Coupling of bias current from the M0 lines to the gate inductors produces a different effect than transient noise within a PTL. These bias lines produce an additional constant current within the inductive loops of the gates.

The effect of bias current coupling on an RSFQ DFF is shown in Fig. 11. This additional current degrades the bias margins of the individual JJs, and therefore the overall bias margins of the gate. This reduction in margins is state dependent, as the noise current is coupled in a specific direction.

To mitigate the effects of bias coupling on the gates, layout algorithms should avoid vertical overlaps between the bias lines and the gate inductors. This topology produces smaller inductive coupling coefficients, reducing any change in gate currents due to inductive noise, as shown in Fig. 11, returning the bias margins to the design specifications. Alternatively, the current carried by the bias lines should

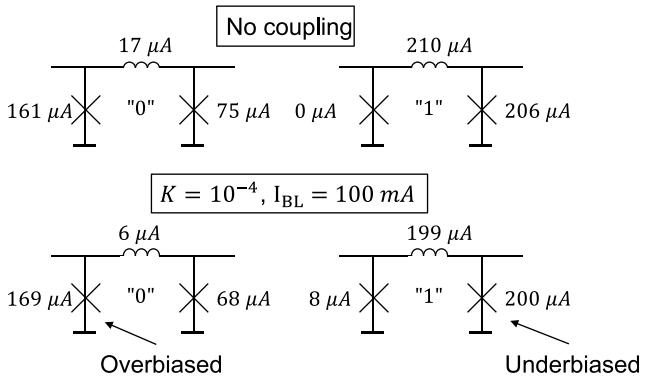

Fig. 11. Effects of bias coupling noise from the M0 bias line on the current distribution within a DFF in M5–M6. I_{BL} is the current carried by the bias line. The stored state is shown in the middle of each storage loop.

be limited to the maximum allowed change in the gate currents (margins). Although this approach reduces the constraints on the routing algorithms, it introduces additional constraints on the bias distribution network.

5. Conclusions

Inductive coupling noise is an important issue in both conventional and superconductive large scale integrated circuits. Inductive noise can introduce errors, degrade parameter margins, and reduce performance. RSFQ circuits are particularly vulnerable to inductive coupling noise due to the highly sensitive gates, low signal amplitudes, and cryogenic, low noise environment.

Different sources of inductive coupling in multilayer VLSI complexity RSFQ circuits for a standard cell design flow are reviewed in this paper. Inductive coupling within the MIT LL SFQ5ee process is described for common circuit structures. The effects of inductive noise on PTLs are described based on the extracted coupling characteristics. Coupling of the bias current from the bias lines to the logic gates and PTLs is also evaluated. Mitigation techniques to reduce the effects of inductive coupling on circuit behavior are presented. These techniques enable higher density SFQ circuits with wider parameter margins.

CRediT authorship contribution statement

Gleb Krylov: Conceptualization, Methodology, Software, Validation, Investigation, Visualization, Writing – original draft. **Eby G. Friedman:** Conceptualization, Supervision, Writing – review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

References

[1] M.A. Manheimer, Cryogenic computing complexity program: Phase 1 introduction, IEEE Trans. Appl. Supercond. 25 (3) (2015) 1–4.
[2] G. Krylov, E.G. Friedman, Single Flux Quantum Integrated Circuit Design, Springer Publishers, 2022, ISBN # 978-3-030-76885-0.
[3] S.K. Tolpygo, V. Bolkhovsky, R. Rastogi, S. Zarr, A.L. Day, E. Golden, T.J. Weir, A. Wynn, L.M. Johnson, Advanced fabrication processes for superconductor electronics: Current status and new developments, IEEE Trans. Appl. Supercond. 29 (5) (2019) 1–13.
[4] K. Gaj, Q.P. Herr, V. Adler, A. Krasniewski, E.G. Friedman, M.J. Feldman, Tools for the computer-aided design of multigigahertz superconducting digital circuits, IEEE Trans. Appl. Supercond. 9 (1) (1999) 18–38.
[5] K. Gaj, Q.P. Herr, V. Adler, D.K. Brock, E.G. Friedman, M.J. Feldman, Toward a systematic design methodology for large multigigahertz rapid single flux quantum circuits, IEEE Trans. Appl. Supercond. 9 (3) (1999) 4591–4606.
[6] W. Chen, A.V. Rylyakov, V. Patel, J.E. Lukens, K.K. Likharev, Rapid single flux quantum T-flip flop operating up to 770 GHz, IEEE Trans. Appl. Supercond. 9 (2) (1999) 3212–3215.
[7] T. Jabbari, G. Krylov, S. Whiteley, E. Mlinar, J. Kawa, E.G. Friedman, Interconnect routing for large-scale RSFQ circuits, IEEE Trans. Appl. Supercond. 29 (5) (2019) 1102805, 1–5.
[8] T. Jabbari, G. Krylov, S. Whiteley, J. Kawa, E.G. Friedman, Repeater insertion in SFQ interconnect, IEEE Trans. Appl. Supercond. 30 (8) (2020) 5400508, 1–8.
[9] T. Jabbari, G. Krylov, J. Kawa, E.G. Friedman, Splitter trees in single flux quantum circuits, IEEE Trans. Appl. Supercond. 31 (5) (2021) 1302606, 1–6.
[10] A. Inamdar, D. Amparo, B. Sahoo, J. Ren, A. Sahu, RSFQ/ERSFQ cell library with improved circuit optimization, timing verification, and test characterization, IEEE Trans. Appl. Supercond. 27 (4) (2017) 1–9.
[11] C.J. Fourie, C.L. Ayala, L. Schindler, T. Tanaka, N. Yoshikawa, Design and characterization of track routing architecture for RSFQ and AQFP circuits in a multilayer process, IEEE Trans. Appl. Supercond. 30 (6) (2020) 1–9.
[12] C. Panem, R.S. Gad, B.K. Kaushik, Vertical traversal approach towards TSVs optimisation over multilayer network on chip (NoC), Microelectron. J. (2021) 105231.
[13] L. Qian, Y. Xia, G. Liang, Study on crosstalk characteristic of carbon nanotube through silicon vias for three dimensional integration, Microelectron. J. 46 (7) (2015) 572–580.
[14] G. Krylov, E.G. Friedman, Inductive noise coupling in superconductive passive transmission lines, in: Proceedings of the IEEE International Midwest Symposium on Circuits and Systems, 2021, pp. 727–731.
[15] G. Krylov, E.G. Friedman, Design for testability of SFQ circuits, IEEE Trans. Appl. Supercond. 27 (8) (2017) 1302307, 1–7.
[16] G. Krylov, E.G. Friedman, Design methodology for distributed large scale ERSFQ bias networks, IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 28 (11) (2020) 2438–2447.
[17] S.K. Tolpygo, V. Bolkhovsky, T.J. Weir, A. Wynn, D.E. Oates, L.M. Johnson, M.A. Gouker, Advanced fabrication processes for superconducting very large-scale integrated circuits, IEEE Trans. Appl. Supercond. 26 (3) (2016) 1–10.
[18] S.R. Whiteley, FastHenry 3.0wr, [Online]. Available: http://www.wrcad.com/ftp/pub/readme.fasthenry.
[19] C.J. Fourie, C. Shawawreh, I.V. Vernik, T.V. Filippov, High-accuracy inductex calibration sets for MIT-LL SFQ4ee and SFQ5ee processes, IEEE Trans. Appl. Supercond. 27 (2) (2017) 1–5.
[20] S.R. Whiteley, Josephson junctions in SPICE3, IEEE Trans. Magn. 27 (2) (1991) 2902–2905.
[21] C.R. Paul, A simple SPICE model for coupled transmission lines, in: Proceedings of the IEEE International Symposium on Electromagnetic Compatibility, 1988, pp. 327–333.