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Double magnetic tunnel junction two bit memory and nonvolatile logic for *in situ* computing☆

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ABSTRACT

In exascale computing, a huge amount of data is processed in real-time. Conventional CMOS-based computing paradigms follow the read, compute, and write back mechanism. This approach consumes significant power and time to compute and store data. *in situ* computation – where data are processed within the memory system – is considered a platform for exascale computation. Spin transfer torque perpendicular magnetic tunnel junctions (PMTJ) is a nonvolatile memory device with several potential advantages (fast read/write, high endurance, and CMOS compatibility) to become a next generation memory solution. A double magnetic tunnel junction (DMTJ) consists of two PMTJs constructed in a vertical arrangement. In this paper, DMTJ offers the possibility of constructing not only standalone and embedded RAM but also MTJ-based VLSI computing. A DMTJ-based two bit memory cell that supports a nonvolatile logic compute paradigm is presented. The multi-level cell supports both a high speed read/write two bit memory cell and a nonvolatile logic gate that computes and stores input data in real-time.

1. Introduction

Many integrated systems have become data centric, where huge amounts of data are collected and processed in real-time. Processing "big data" and exascale computing with 10^{18} floating point operations per second is not achievable with conventional computing architectures. Conventional von Neumann architectures, where the memory is separate from the processing elements, struggle despite advanced memory solutions. In data centric architectures, data motion is greatly decreased by integrating the computational process within the storage system at different levels of the memory and storage hierarchy. This capability for *in situ* computation can be achieved by exploiting an emerging memory technology that exhibits two modes of operation within the same platform, memory and compute.

The classical von Neumann separation between memory and computing expends significant energy and space. These systems are volatile and leak significant current. Non-volatile memory (NVM) technologies have been proposed to replace CMOS memory within different parts of the memory hierarchy. Some of these NVM solutions support in-memory computing, such as memristor-based logic [1–3] and spintronic-based compute-in-memory [4–7]. Memristors exhibit a low endurance rate (up to 10^{10} cycles [8]) as compared to the high endurance characteristics of spintronic systems (10^{15} write cycles [9]). This higher endurance makes spintronic memristors an effective solution for in-memory compute applications.

Magnetic random access memory (MRAM) is a spintronic NVM, considered as a possible solution at all memory hierarchies. This breadth is supported by the development of multiple magnetic memory technologies, serving each level of the memory hierarchy, such as magnetic tunnel junctions (MTJ) [10], domain wall motion devices [11,12], all spin logic [13], spin orbital torque (SOT) MTJ [14,15], magnetic skyrmions [16], and topological insulator/ferromagnetic memory [17]. MRAM exhibits a retention time of almost ten years with high endurance rates, high speed, small size, and CMOS compatibility. While most of these spintronic MRAM solutions target in-memory computing [5–7], these systems are large in size and only support a one bit memory cell.

Most MRAM solutions are based on a perpendicular MTJ (PMTJ) with spin transfer torque (STT). This technology has attracted considerable attention due to the high endurance rate, fast switching, CMOS compatibility, simple device structure, and ability to scale to sub−10 nm dimensions [18]. STT MRAM, however, requires a high critical current density to switch a device. Consequently, the memory cell is scaled to satisfy both density and power demands. These scaled PMTJ devices, however, suffer from aging and low endurance. Hence,

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a multi-level cell is proposed here to further increase memory density. A double magnetic tunnel junction (DMTJ) is a multi-level STT PMTJ cell composed of two serially connected PMTJ devices. The DMTJ is manufactured in a vertical stack, with an area comparable to a single PMTJ. The DMTJ device exhibits four stable resistance states, 00, 01, 10, and 11, where the most significant bit (MSB) represents the resistance state of the larger PMTJ device, and the least significant bit (LSB) represents the resistance state of the smaller PMTJ. 0 and 1 represent the resistance state of a PMTJ device in, respectively, the parallel and antiparallel state.

In this paper, the DMTJ structure is combined with CMOS to provide a hybrid two bit memory cell and a nonvolatile logic AND, OR, and NOT element. The contribution of this paper lies in two aspects. First, a write circuit for the DMTJ-based STT PMTJ is proposed. Second, a nonvolatile AND, OR, and NOT logic gate based on the multi-level MTJ is presented. This logic gate is described by a state diagram and the physical operation of the DMTJ device. The paper is organized as follows. In Section 2, background on recent compute-in-memory solutions utilizing different nonvolatile memory technologies is discussed. The structure and physical model of the DMTJ device are described in Section 3. The DMTJ-based two bit memory cell is presented in Section 4, where a hybrid CMOS/DMTJ read/write circuit is also proposed. The DMTJ-based nonvolatile AND, OR, and NOT gates are described in Section 5. Simulation results are presented in Section 6. A comparison between the proposed work and earlier approaches is offered in Section 7. The paper is concluded in Section 8.

2. NVM-based logic

NVM is based on an emerging memristive device that exhibits a hysteresis characteristic, acting as a state machine. The current state of a memristive device is maintained unless a perturbation (e.g., voltage, current, magnetic field, or electric field) is applied [19]. Multiple logic functions can be demonstrated by the state diagram of one or multiple connected memristive devices. Several NVM-based logic in-memory systems have previously been proposed [1,3–5,20]. Memristors and spin orbital torque (SOT) devices are often considered as a base element for logic in-memory systems. At least two memristors and up to three clock cycles are required in memristor-based in-memory systems to deliver a functionally complete logical operation [1,3]. Similar to the system proposed here, these memristive systems require multiple cycles to perform a logical operation.

MRAM solutions, particularly SOT devices, exhibit a high endurance rate. SOT devices are more frequently considered for logic in-memory solutions than STT devices due to the higher endurance rate of SOT devices and the decoupled read and write paths [5]. Similar to the proposed system, SOT-based logic requires the initial state to be written [20] and the output described by a nonvolatile resistance state which is read by a standard memory read operation [20].

These compute-in-memory systems are based on a single bit memory cell. Multi-level STT MTJs (e.g., DMTJ) improve the density of STT MRAM and reduce the cost per bit [21,22]. Limited work exists on DMTJ STT-based logic in-memory systems. The DMTJ STT in-memory system proposed in [4] is volatile. This structure is achieved by adding circuitry to the sense scheme to support the logical AND, OR, and XOR operations [4]. The drawbacks of this earlier system lie in the need to initially store the input within the DMTJ before calculation, while the output is volatile and not stored. Hence, this system requires additional time and power to perform a nonvolatile logical operation. Alternatively, fully nonvolatile memory and logic based on the DMTJ is proposed in this paper.

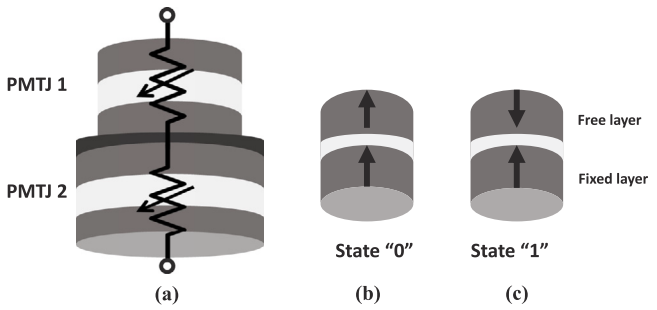

Fig. 1. Multi-level STT MRAM cell composed of two serially connected PMTJs, (a) two PMTJs connected in series modeled as a variable resistance based on the state of operation, (b) state “0” when the magnetization state of the free and reference layer is in parallel, and (c) state “1” when the magnetization state is in the antiparallel state.

3. Multi-level STT-MRAM cell

A DMTJ is a multi-level STT PMTJ cell composed of two serially connected PMTJ devices. The two PMTJs share the same characteristics but with different diameters, D_{MTJ1} and D_{MTJ2}. A DMTJ is a two terminal device modeled as two serially connected resistors, as shown in Fig. 1. A model of a DMTJ resistor is described in the Appendix. Each PMTJ exhibits two stable resistance states, parallel (0) and antiparallel (1), whereas the DMTJ exhibits four different resistance states, represented as R_{00}, R_{01}, R_{10}, and R_{11}. The MSB represents the state of the large PMTJ (PMTJ2), and the LSB represents the state of the small PMTJ (PMTJ1). In the R_{01} state, PMTJ2 operates in the parallel state, and PMTJ1 operates in the antiparallel state. Since PMTJ2 has a larger diameter than PMTJ1, PMTJ2 exhibits a lower resistance than PMTJ1. Consequently, PMTJ2 requires a greater current than PMTJ1 to switch between the parallel and antiparallel states.

The simple MTJ cell structure requires two additional mask steps to integrate the STT storage elements into a logic compatible CMOS process [23]. A DMTJ cell has previously been demonstrated with four distinctive resistive states with successful read and write operations [24–26]. The DMTJ is applicable to a wide variety of applications, supporting high density, low power cache memory [21,22,27–35]. In a previous study, a systematic analysis of the sources of variations in DMTJ STT MRAM and the reliability of the read and write operations is described. This study concludes that a DMTJ with series connected PMTJs exhibits higher read and write reliability than parallel connected PMTJs [36].

A compact model capturing the static and dynamic behavior of a perpendicular magnetic anisotropy MTJ, including the influence of the device dimensions and temperature on the perpendicular magnetic anisotropy of a PMTJ, is described in [37,38]. A version of this macrospin model, described in the Appendix, is used to support the hybrid MTJ/CMOS circuit design and simulation process. The model considers the influence of current and temperature on the device tunneling magnetoresistance, layer spin polarization, saturation magnetization, and device interfacial and bulk magnetic anisotropy constant [37,38].

A state flow diagram of a DMTJ is shown in Fig. 2, where $+I_{c2}$ and $-I_{c2}$ are, respectively, the critical current to switch PMTJ2 between the parallel and antiparallel states, where I_{c1} is the critical current to switch PMTJ1 between the parallel and antiparallel states. I_{c2} is larger than I_{c1}. In the following section, a two bit hybrid MTJ/CMOS memory cell is proposed. The circuit requires a two step write scheme and a one step read scheme.

4. DMTJ STT PMTJ as two bit memory cell

To employ a DMTJ as a two bit memory cell, the cell should supply bidirectional current and exhibit two different current levels. A circuit

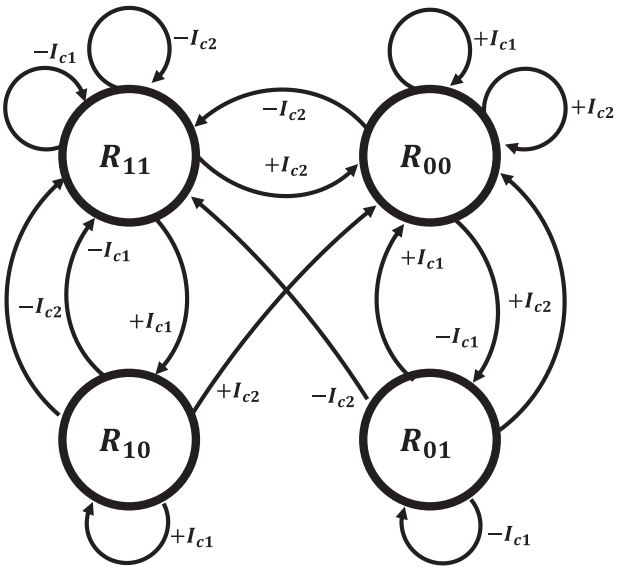

Fig. 2. State flow diagram of a DMTJ with two serially connected PMTJs. The device provides four resistance states and switches between the states based on the applied current.

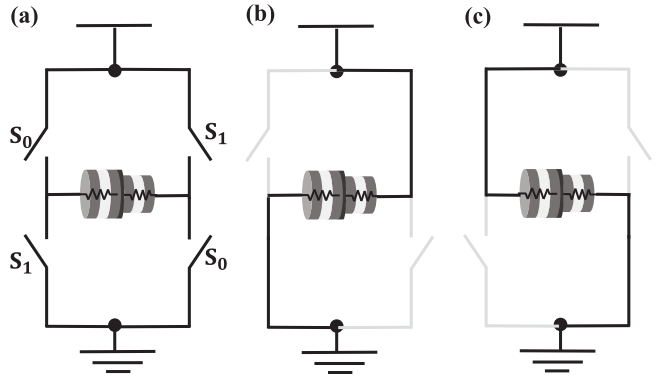

Fig. 3. H-bridge circuit, (a) switches S_0 and S_1 control the direction of the current within the DMTJ, (b) S_1 is closed, and (c) S_0 is closed.

commonly known as an H-bridge [39] (see Fig. 3) is modified to achieve the write capability of the DMTJ. When switch S_0 is closed, the current supplied to the DMTJ is in the opposite direction than when switch S_1 is closed. The H-bridge has been previously adopted to switch an STT-based MTJ, while in this paper, an H-bridge circuit is modified to switch a DMTJ, as discussed in Section 4.1.

Based on the current resistance state, a DMTJ transitions to another state in one step except for the transition between the R_{01} and R_{10} resistance states, as illustrated in the state diagram of a DMTJ shown in Fig. 2. A reset step is initially required, followed by a write step. Since no sense step is used before the write operation, a one step process writes the R_{00} or R_{11} state by applying, respectively, a high positive current pulse or a negative current pulse. The two step write process consists of a *reset* step and a *write* step to produce the other two resistance states of the DMTJ. The write and read operations of a DMTJ are described in the following subsections.

4.1. Write technique

The proposed write circuit utilizes an H-bridge topology. Each switch of the write circuit, shown in Fig. 3, utilizes the CMOS network shown in Fig. 4. Each CMOS network sources critical current to switch a DMTJ. The right side of the branch within each CMOS network, shown

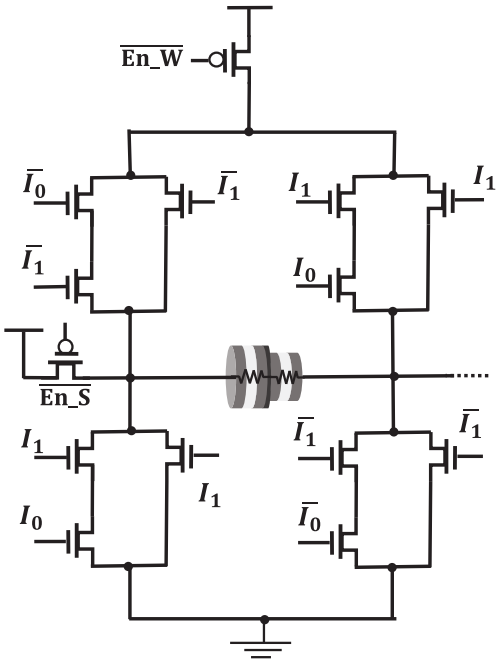

Fig. 4. Two bit DMTJ memory cell based on a multi-level STT PMTJ. En_W enables the write operation, En_S enables the sense operation, and I_0 and I_1 are, respectively, the magnitude and direction of the current supplied to the DMTJ.

in Fig. 4, includes only one transistor; therefore, if $I_1 = 1$, the NMOS transistor at the right branch of the top right CMOS network and the NMOS transistor at the right branch of the bottom left CMOS network are connected to the DMTJ. Hence, two CMOS transistors are connected in series with the DMTJ. These transistors are small, providing low current to the DMTJ, sufficient to switch a small PMTJ. If both $I_1 = 1$ and $I_0 = 1$, both sides of the CMOS network produce a large current. Note that the transistors in the left side within each CMOS network are larger than the transistors in the right side to source this larger current. The size of the CMOS networks is critically dependent on the four resistance states within the DMTJ and the critical current to switch the PMTJs within the DMTJ. Hence, the sourced current is sufficiently large to switch the DMTJ into the target state by switching either the small PMTJ or both the small and large PMTJs.

To better understand the circuit operation, a notation is used to represent the current supplied to a DMTJ, as follows: I_{00} represents $+I_{c2}$, I_{01} represents $+I_{c1}$, I_{10} represents $-I_{c1}$, and I_{11} represents $-I_{c2}$. The MSB is the direction of the current, positive if zero and negative if one. The LSB represents the current magnitude, where zero is less current and one is more current. The hybrid CMOS/MTJ two bit memory is shown in Fig. 4 where I_1 and I_0 represent, respectively, the MSB and LSB of each current. As an example, if I_{00} is the applied current, $I_0 = 0$ and $I_1 = 0$. Hence, the top left CMOS network operates with the bottom right CMOS network. En_W enables the write operation, and En_S enables the sense operation.

4.2. Read technique

In the proposed memory cell, a one step read scheme senses the resistance of the DMTJ [24]. The sense circuit is illustrated in Fig. 5 where the voltage across the DMTJ is compared with three different voltage references. The read circuit includes three sense amplifiers to simultaneously compare the selected DMTJ cell voltage with the voltage references followed by an encoder that identifies the state of the MSB and the LSB. The sense current is sufficiently small to not switch the DMTJ.

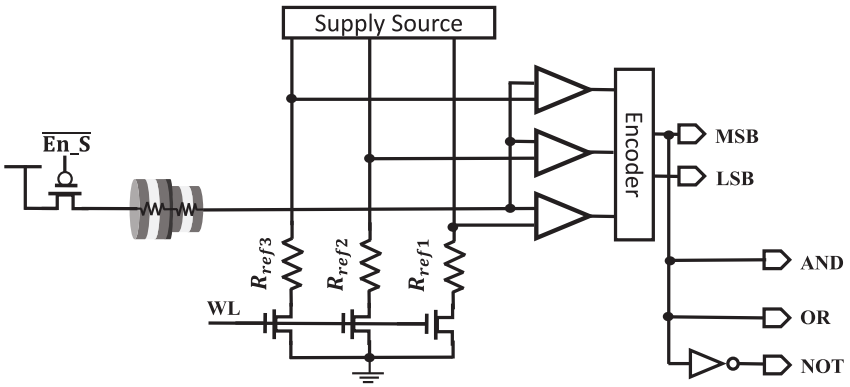

Fig. 5. One step read scheme for a four level cell memory [24] with the DMTJ-based nonvolatile AND, OR, and NOT gates.

Table 1
Truth table of a DMTJ as a state machine.

S_1	S_0	I_1	I_0	S_1'	S_0'
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	1
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	0	1
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	1	1	0
1	0	1	0	1	1
1	0	1	1	1	1
1	1	0	0	0	0
1	1	0	1	1	0
1	1	1	0	1	1
1	1	1	1	1	1

5. DMTJ STT PMTJ as AND, OR, and NOT logic gates

The behavior of a DMTJ operating as a nonvolatile logic element is illustrated in the state flow diagram shown in Fig. 2. The DMTJ is treated as a state machine with two one bit inputs and four states. The two one bit inputs, I_1 and I_0, refer, respectively, to the direction and magnitude of the supplied current. The four states refer to the four resistance states of a DMTJ. The truth table of a DMTJ, as a state machine, is listed in Table 1. S_1 and S_0 represent, respectively, the present state of the large PMTJ and small PMTJ, and S_1' and S_0' represent, respectively, the future state of the large PMTJ and small PMTJ.

The boolean representation of the future state bits, S_0' and S_1', in terms of the current state of a DMTJ and input current bits, illustrated in Fig. 6, is, respectively,

$$S_0' = I_1 \tag{1}$$

$$S_1' = I_1 I_0 + S_1 I_0 + S_1 I_1. \tag{2}$$

A DMTJ transitions into a non-volatile state once a current is applied. The future memory state of a DMTJ is represented by S_0' and S_1', where S_0' and S_1' are, respectively, the future state of the small PMTJ and large PMTJ. Based on (1), S_0' cannot represent a logical operation of the input bits. However, as described by (2), S_1' is the logical computation of the input bits which can produce a logic family through the following relationship: When $S_1 = 0$, $S_1' = I_1 I_0$; hence, the future memory state of the large PMTJ is the AND operation between the two input bits, I_1 and I_0. When $S_1 = 1$, $S_1' = I_1 I_0 + I_0 + I_1$. S_1' is therefore the OR output of I_1 and I_0.

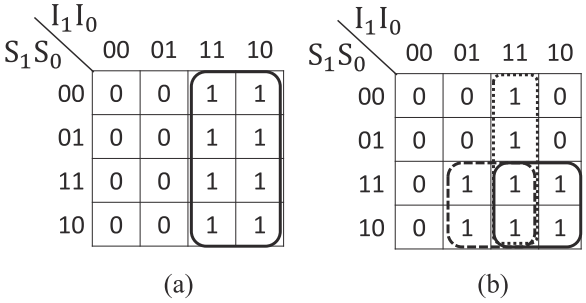

Fig. 6. Karnaugh map of the future state bits of a DMTJ, (a) S_0', and (b) S_1'.

Accordingly, a DMTJ operates as an AND gate when the device is initially reset to the state where $S_1 = 0$, such as R_{00} or R_{01}. The input to the AND gate is I_1 and I_0, and the output is stored in the large PMTJ. To operate a DMTJ as an AND gate, the DMTJ is reset to the R_{00} state since only one pulse is required to set the PMTJs into this state.

To configure a DMTJ as an OR gate, the DMTJ device is initially reset to the state where $S_1 = 1$ such as R_{11} or R_{10}. The output of the OR operation is stored within the large PMTJ. The R_{11} state is chosen as a *reset* state when a DMTJ behaves as an OR gate since the R_{11} state can be written by the single pulse write scheme.

The DMTJ can be realized as a NOT gate by storing the input signal within a DMTJ; hence, the output of the NOT gate can be achieved by a CMOS inverter, as shown in Fig. 5. I_1 is the input to the NOT gate. To operate the DMTJ as a NOT gate, the device is initially reset to the R_{11} state, followed by a *calculate* state where the input is applied to the I_1 node and I_0 is set to zero. Based on (2), where $S_1 = 1$ and $I_0 = 0$, $S_1' = I_1$. The output of the NOT gate is as shown in Fig. 5.

The primary advantage of the proposed system lies in the ability to perform a logical operation and store the result in real-time as a non-volatile memory state. The proposed logical operation of a DMTJ is supported by the same memory system without requiring any additional circuitry. The operational mechanism and simulation of a DMTJ behaving as a two bit memory cell and a nonvolatile logic element are described in the following section.

6. Operational mechanism and simulation results

A hybrid CMOS/DMTJ architecture that supports a read/write/nonvolatile logic operation is shown in Fig. 7. A DMTJ is treated as a state machine, where the next state of a DMTJ is based on the input current and the present state of the DMTJ. The input current is based on the input bits and the output is stored within the DMTJ in a nonvolatile state. The operation of a DMTJ as a memory element and a nonvolatile logic element is based on a macrospin model of a DMTJ composed of

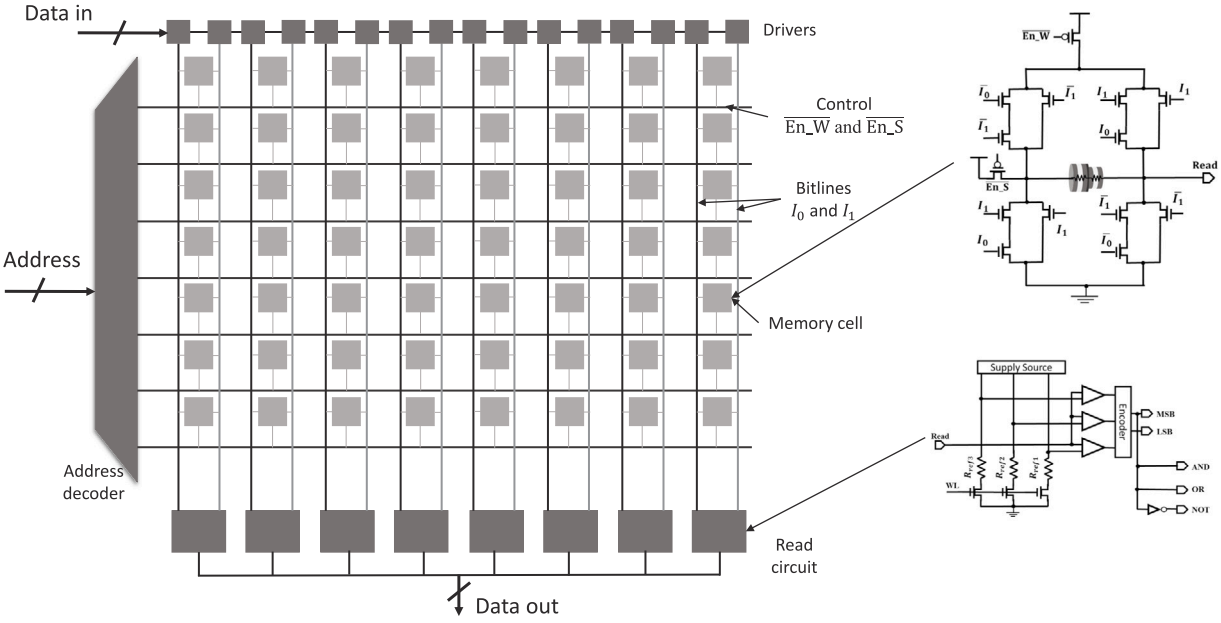

Fig. 7. Proposed DMTJ-based two bit memory cell that supports the compute-in-memory paradigm. The system input chooses the row being read/write/calculate through a decoder. The decoder enables the cell to perform the write/read/calculate operation. The read lines are connected to a read scheme which produces the system output.

Table 2
Operational mechanism of the proposed DMTJ-based nonvolatile compute-in-memory system.

Operation		Input		Output
		Step 1	Step 2	
Memory	Write 00	$I_1I_0 = 00$	NA	NA
	Write 01	$I_1I_0 = 00$	$I_1I_0 = 10$	
	Write 10	$I_1I_0 = 11$	$I_1I_0 = 01$	
	Write 11	$I_1I_0 = 11$	NA	
Logical AND	C = A.B	$I_1I_0 = 00$	$I_0 = A, I_1 = B$	$C = S_1$
Logical OR	C = A + B	$I_1I_0 = 11$	$I_0 = A, I_1 = B$	$C = S_1$
Logical NOT	$C = \overline{B}$	$I_1I_0 = 11$	$I_0 = 0, I_1 = B$	$C = \overline{S_1}$

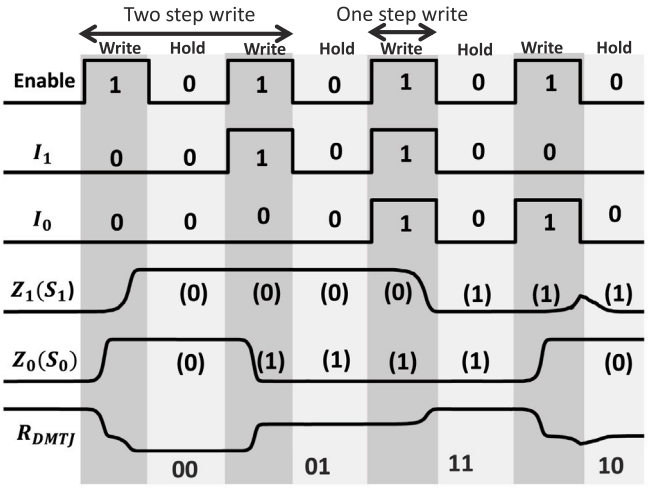

Fig. 8. Waveform of a DMTJ behaving as a two bit memory element, where Enable is the control signal, I_0 and I_1 are the inputs, Z_0 and Z_1 are the perpendicular magnetization of, respectively, the small PMTJ and large PMTJ, S_0 and S_1 are, respectively, the corresponding state of the small PMTJ and large PMTJ, and R_{DMTJ} is the change in the resistance of the DMTJ.

two serially connected STT PMTJs with a diameter of, respectively, 30 nm and 40 nm. A 32 nm predictive technology model is used to characterize the CMOS transistors [40]. The CMOS transistors are sized to provide sufficient current to switch each PMTJ based on inputs I_1 and I_0. The size of the CMOS transistors and the diameter of the two PMTJs are critical since the greater the size of a PMTJ, the lower the resistance and the larger the critical current required to switch the DMTJ cell.

The operational mechanism of the proposed system is listed in Table 2. Based on the functional operation (memory write or logical AND, OR, or NOT), a one step or two step scheme is followed. The output of the logical operation is collected at the MSB port (stored in the status of PMTJ1 – see Fig. 7).

A waveform of a DMTJ-based two bit memory cell is illustrated in Fig. 8 where the write operation is controlled by the enable write signal En_W. En_W supports two modes of operation. When $En_W = 1$, the circuit operates in the write mode and a current is produced. When $En_W = 0$, the circuit operates in the *hold* mode with no supply current; hence, the DMTJ is set in a stable state. The pulse width of the *write* and *hold* time signals is carefully chosen. Limitations on the *write* and *hold* time are governed by the influence of the spin transfer torque on the PMTJ. The wider the pulse of the supply current, the less critical current required to switch the PMTJ. Limitations on the width of the write pulse are due to the worst case write scenario (the write signal only switches the smaller PMTJ, not the larger PMTJ). The width of the minimum write pulse is chosen to switch the smaller PMTJ, while the width of the maximum write pulse is set to not switch the larger PMTJ.

The direction and magnitude of the supplied current are, controlled respectively, by I_1 and I_0. Z_0 and Z_1 are, respectively, the orientation of the perpendicular magnetization of PMTJ1 and PMTJ2 within the DMTJ. The pinned ferromagnetic layer of the DMTJ is magnetized in the positive z direction (pointing up). As an example, if $Z_0 = 1$, PMTJ1 is in the parallel state with $S_0 = 0$. The input signals to write the four resistance states within a DMTJ are shown in Fig. 8. A minimum and maximum write pulse of, respectively, 25 ns and 35 ns is required to

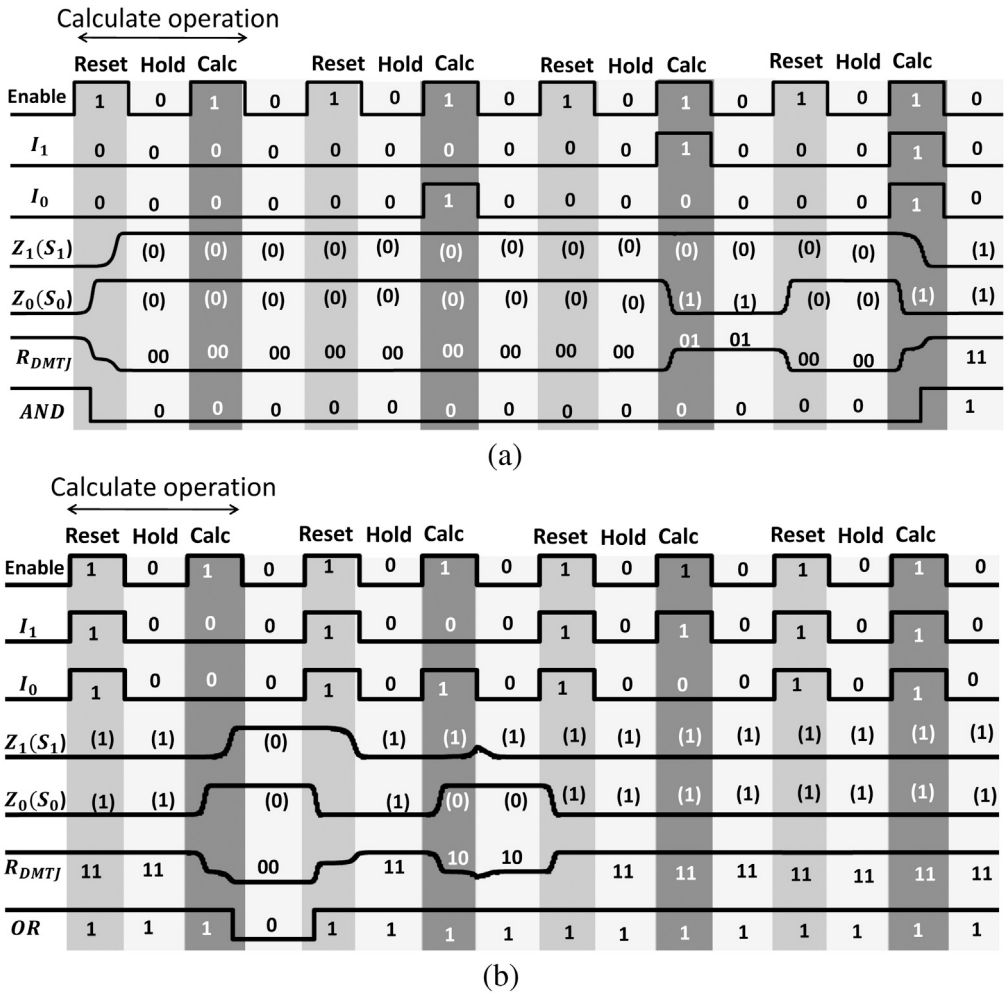

Fig. 9. Operation of a nonvolatile DMTJ logic gate, (a) AND gate, and (b) OR gate. Enable is the control signal, I_0 and I_1 are the inputs, Z_0 and Z_1 are, respectively, the perpendicular magnetization of the small PMTJ and large PMTJ, S_0 and S_1 are, respectively, the corresponding state of the small PMTJ and large PMTJ, and R_{DMTJ} is the change in the resistance of the DMTJ.

Table 3
Comparison of nonvolatile AND in-memory compute systems.

Technology	Device requirement	# of steps	Delay	Process
DMTJ	One DMTJ (Two serially connected PMTJs)	Two	70 ns	32 nm CMOS
Memristor [3]	Two serially connected memristors with opposite polarities	Two	100 ns	–
SOT [20]	One voltage-gated spin hall effect device	Two	~10 ns	40 nm CMOS

write a state within a DMTJ. A minimum hold time of 10 ns is required once each *write* state is set to ensure the device remains in a stable state.

Operating a DMTJ as a non-volatile logic element is achieved in two steps. A *reset* state is initially written into the DMTJ based on the logical operation, the R_{00} state for an AND operation and the R_{11} state for an OR operation. This step is followed by the *calculate* state, where the logical operation is computed in real-time, and the non-volatile state is stored within the DMTJ. A waveform of a DMTJ-based AND gate and OR gate is shown, respectively, in Figs. 9(a) and 9(b).

A critical current of approximately 100 μA and 140 μA is required to switch, respectively, the smaller and larger STT PMTJs. Significant development has recently been achieved in decreasing the critical current required to switch an STT PMTJ. These approaches primarily use (1) low damping materials for the thick free layers [41], and (2) new composites (such as MgO_xN_{1-x} [42]) as a tunnel barrier to overcome the inter-layer diffusion [42]. These recent developments in STT PMTJ memory are producing higher switching speeds, greater endurance, and lower critical currents [41,42].

7. Comparison with state-of-the-art memristive-based compute-in-memory systems

The proposed DMTJ-based compute-in-memory system is different from alternative memristive-based compute-in-memory systems such as a single STT MTJ MRAM-based system [43], SOT-MRAM-based system [20], and memristor-based systems [3]. In single STT MRAM-based compute-in-memory systems [43], where each memory cell stores a single bit, circuitry is needed after the sense amplifier to perform the logical operation, producing a volatile output. A comparison of the delay and system requirements of the proposed compute-in-memory system with recent *in situ* MRAM-based in-memory computing schemes is listed in Table 3. The memristor-based in-memory compute system, described in [3] with Ta/GeTe/Ag memristors with an area of the GeTe functional layer of 10 × 10 μm^2, requires two cycles (100 ns) to perform a nonvolatile AND operation, while the DMTJ system proposed here requires 70 ns. The SOT-based logic in-memory system proposed in [20] requires approximately 10 ns for a nonvolatile AND operation assuming a 40 nm CMOS technology with a voltage-gated spin hall

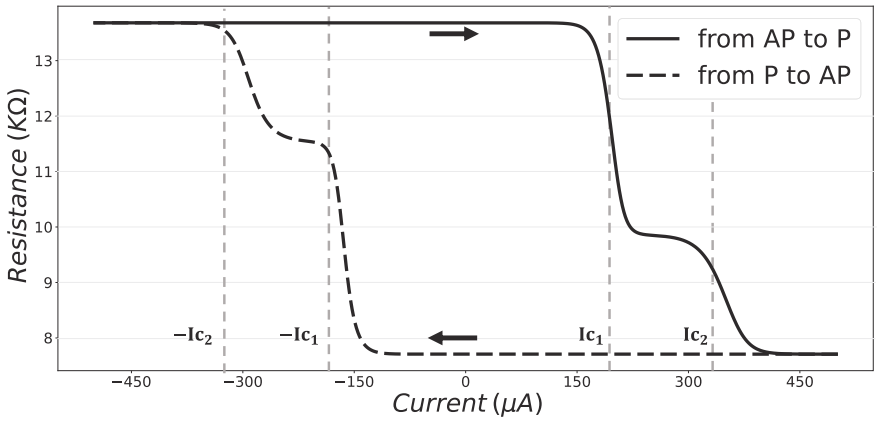

Fig. A.10. Antiparallel to parallel (AP–P) transition and parallel to antiparallel (P–AP) transition of a DMTJ. The vertical axis is the resistance of the DMTJ at 0 V, and the horizontal axis is the current to switch a DMTJ.

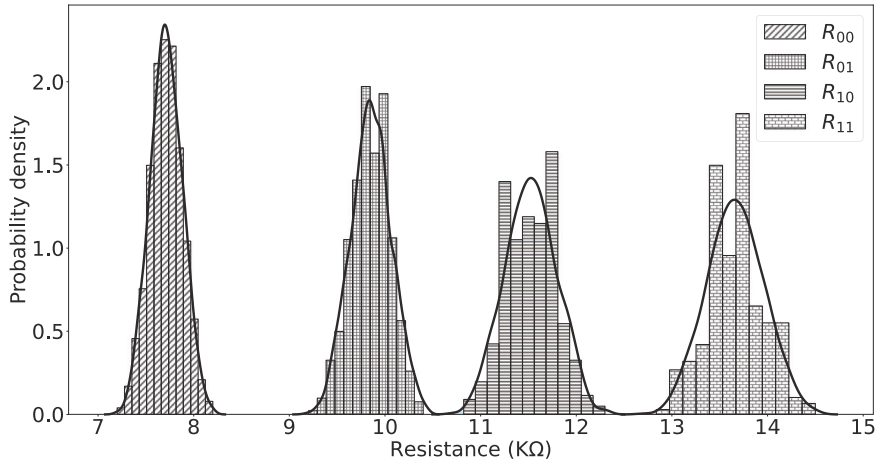

Fig. A.11. Monte Carlo simulation of the four state resistance distributions of a DMTJ with process and temperature variations.

effect MRAM cell. The length of each row in the SOT crossbar array is however limited by the resistance of the heavy metal layer that supports spin orbital torque interactions within multiple SOT devices, leading to different write conditions for the SOT cells along the heavy metal layer.

8. Conclusions

A double magnetic tunnel junction (DMTJ) is a device composed of two serially connected perpendicular magnetic tunnel junctions with different diameters, providing four different resistance states. In this work, the DMTJ is proposed both as a two bit memory element and as a nonvolatile logic element. A hybrid CMOS/DMTJ circuit supports a read/write/nonvolatile logic operation. The DMTJ behaves as a two bit memory element through a two step write mechanism producing two resistance states, a one pulse write mechanism for the two resistance states and a one step read mechanism. The DMTJ also behaves as a nonvolatile logic element. The DMTJ is reset to an initial state followed by a calculate state. The output of the logical operation is stored as a nonvolatile state within the DMTJ. The DMTJ behaves as a nonvolatile AND, OR, and NOT gate with, for a 32 nm CMOS technology node, a delay of 70 ns. The proposed nonvolatile memory/logic cell exhibits an access time of 35 ns with a one step write scheme to write either the R_{00} state or R_{11} state, and 70 ns for a two step write scheme to write either the R_{01} state or R_{10} state.

Appendix. Macrospin model of a multi-level STT-PMTJ device

A macrospin compact model of a double magnetic tunnel junction device based on two serially connected spin transfer torque perpendicular MTJs is described in this Appendix [37]. The model parameters are listed in Table A.1. The model considers the dynamic response of the magnetic and electrical performance of the device. The magnetization dynamics of the free ferromagnetic (FM) layer are characterized by the modified Landau–Lifshitz–Gilbert equation [44,45],

$$\frac{\partial \vec{M}}{\partial t} = -\frac{\gamma \mu_o}{1+\alpha^2}[\vec{M} \times \vec{H}_{eff} + \alpha\ \vec{M} \times \frac{\partial \vec{M}}{\partial t}] + \gamma \sum \vec{\tau}_i, \tag{A.1}$$

where $\vec{M}$ is the normalized free layer magnetization, t is the time variable, $\vec{H_{eff}}$ is the effective magnetic field expressed in A/m, γ is the electron gyromagnetic ratio, $\gamma \approx -2\pi \times 27.99$ GHz/T, μ_o is the permeability of free space, α is the Gilbert damping factor, and $\vec{\tau}_i$ is the applied torque due to other perturbations such as current which exerts a spin transfer torque τ_{STT} [46].

The macrospin model includes the static and dynamic micromagnetic behavior related to the system energy. The applied effective magnetic field across the free layer $\vec{H_{eff}}$ is

$$\vec{H}_{eff} = \vec{H}_{UA} - \vec{H}_{dem} + \vec{H}_c + \vec{H}_{ext} + \vec{H}_{th}, \tag{A.2}$$

where $\vec{H_{UA}}$ is the uniaxial anisotropy field, sometimes defined as $\vec{H}_K$ [47], $\vec{H_{dem}}$ is the demagnetization field, $\vec{H}_c$ is the coupling field

Table A.1
Physical parameters of double PMTJ.

Parameters	Description	Value
D_{MTJ1}	Diameter of small PMTJ	30 nm
D_{MTJ2}	Diameter of large PMTJ	40 nm
t_{FL}	FM thickness	15 nm
t_{ox}	Barrier thickness	0.85 nm
Φ_{BL}	Barrier height	0.4 eV
M_S	Saturation magnetization	1.2×10^6 A/m
K_i	Interfacial magnetic anisotropy density	2.2×10^{-3} J/m^2
K_u	Bulk magnetic anisotropy density	-0.11×10^6 J/m^3
α	Magnetic damping constant	0.005
P	Spin polarization	0.57
RA	Resistance area product	4 Ω μm^2
T	Temperature	300 K
TMR_0	TMR ratio with 0 bias	1

due to the other FM layer, $\vec{H_{ext}}$ is the applied external magnetic field, and $\vec{H_{th}}$ is the stochastic magnetic field due to thermal variations. $H_{th} = \sigma\sqrt{2K_BT\alpha/\mu_0 M_S \gamma V_{FL}\Delta t}$, where σ is a random noise variance, K_B is the Boltzmann constant, T is the ambient temperature, V_{FL} is the FM layer volume, Δt is the simulation time step, and μ_0 is the permeability in free space. The resistance–current characteristic of a DMTJ based on two serially connected STT PMTJs is shown in Fig. A.10, indicating the four resistance states of the DMTJ and the critical current at which each PMTJ switches.

The performance and reliability of a DMTJ cell resensitive to CMOS and MTJ device variations and thermal induced randomness. To avoid a read failure (an overlapping distribution of resistances), the size of each PMTJ within the DMTJ is critical. The distribution density of the four resistance states in a DMTJ is shown in Fig. A.11. The distribution density is based on Monte Carlo simulations with a sigma value of 3% and 1,000 samples for the thickness of the oxide material of the PMTJ t_{ox}, thickness of the ferromagnetic layer t_{FL}, length of the ferromagnetic layer l_{FL}, and width of the ferromagnetic layer W_{FL}.

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