THE LIMITING PERFORMANCE OF A CMOS BISTABLE REGISTER BASED ON WAVEFORM CONSIDERATIONS

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ABSTRACT

Closed form solutions describing the output response of a CMOS bistable register are presented. From these results, the fundamental latching behavior of a CMOS register is developed in terms of its physical and circuit characteristics. Necessary and sufficient conditions for latching data are described in terms of small signal circuit parameters. From these necessary and sufficient conditions, the limiting condition for latching and the onset of metastability are presented and verified.

1. INTRODUCTION

Early work in the area of sensing and latching input waveforms has focused on the design of sense amplifiers in memory circuits. Lynch and Boll [1] derive an optimal waveform shape for latching data into a two transistor (with pull-ups) sense amplifier cell. Recently, Yuan and Liou [2] expanded their work by considering effects such as capacitive coupling on the waveform shape required for latching data in a DRAM sense amplifier. This paper, however, describes the optimal latching requirements of a different, though related, and very common circuit structure, a CMOS bistable register. Some relevant research analyzing a CMOS bistable register and its response due to non-step input waveforms has been performed in the investigation of metastability [3-8]. In [9], the latching behavior of a CMOS register based on waveform considerations is described. This paper is similar to the related research on metastability in that the set of conditions which define the onset of metastability are determined; in addition, necessary and sufficient conditions for latching data into a bistable register are also determined, defining the minimum temporal requirement for latching.

Three responses of a register can occur; 1) the data signal is successfully latched into the register, 2) the data signal is not successfully latched into the register and the register returns to its initial state, and 3) the register enters a state of metastability in which neither binary state is reached within a time period consistent with the normal operation of the register. The register will remain in this tenuous state of equilibrium until some circuit parameter varies sufficiently to drive the state of the register into one of the two binary states [10]. Thus, the state of metastability is categorized as a type of reliability problem.

The circuit behavior of the latch can be broken up into four separate regions of operation. Each of these regions is analyzed in detail, and small signal closed form solutions of the output response for each region are summarized in section 2. The closed loop regenerative latch behavior occurs in the third region of operation. This permits the development of necessary and sufficient conditions for latching data into a register. From these conditions, the fundamental limiting condition for latching data into a CMOS bistable register is presented and verified through simulation. This relation also provides a limiting definition of metastability. These are described in section 3 of this paper. Some concluding remarks are made in section 4.

2. LATCHING DATA INTO A CMOS REGISTER

In order to latch data into a register, the clock and data signals must appear at the input of the register at the correct relative time and at the correct voltage magnitudes. These time and voltage requirements are described in analytical form in sections 2 and 3 of this paper. In this analysis, the input clock and data waveforms are assumed to behave as ramp signals, not as step inputs, so as to better represent the effects of the waveform shape on the output response.

The initial conditions of $V_1(0) = G_{ND}$ and $V_2(0) = V_{DD}$ have been chosen to exemplify the latching phenomenon, where G_{ND} and V_{DD} are the lower and upper power supply voltages, typically 0 volts and 5 volts, respectively. Assuming the clock signal, V_{CLK}, is at V_{DD} and the data signal, V_{DATA}, is at G_{ND}, the circuit exists in a restoring equilibrium state. In order to change the polarity of the output voltages at V_1 and V_2, both the clock and the data input signals must switch. The clock signal must decrease from V_{DD}, and the data signal must increase from G_{ND}.

The response of the bistable register to its changing input signals can be broken down into four separate regions. Each region represents the bistable register operating under different circuit conditions, and therefore each region has a different output response.

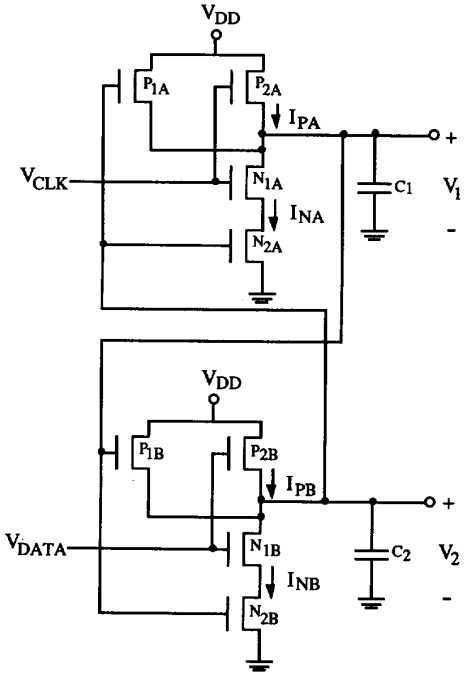

Figure 1: CMOS Implementation of Bistable Register

Region 1

As V_{CLK} decreases from V_{DD} to $V_{DD} + V_{TP}$, no current can flow through the upper NAND gate (see Figure 1) since 1) both P-channel devices

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are in cutoff, P_{2A} due to $V_{CLK} \geq V_{DD} + V_{TP}$ and P_{1A} due to $V_2 \geq V_{DD} + V_{TP}$, and 2) V_1 is at the same potential as the sources of the two N-channel devices. Thus, region 1 represents the time required for V_{CLK} to reach $V_{DD} + V_{TP}$ and turn on P_{2A}, thereby permitting current to flow. Throughout this region V_1 remains at 0 volts, as shown in Figure 2, and the time delay, t_1, of this region is given by equation (1).

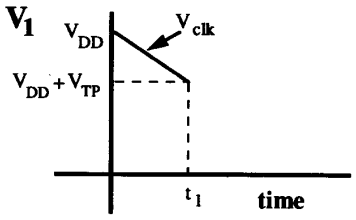

Figure 2: Region 1 Timing Diagram

$$t_1 = \left| \frac{V_{TP}}{K_c} \right| \tag{1}$$

where k_C is the decreasing rate of change of the clock signal in volts per second and V_{TP} is negative for an enhancement mode P-channel device.

Region 2

Once V_{CLK} decreases below $V_{DD} + V_{TP}$, current will flow between V_{DD} and ground. As V_{CLK} decreases further, the current supplied by P_{1A} will become greater than the current sunk by the N-channel tree. Once this occurs, $V_1(t)$ will begin to rise. In this region, the bistable NAND gate register can be represented by a single NAND gate with one changing input (since $V_2 = V_{DD}$). This circuit can be represented by the small signal model shown in Figure 3, where v_c represents the incremental change in V_{CLK} and v_1 represents the incremental change in V_1.

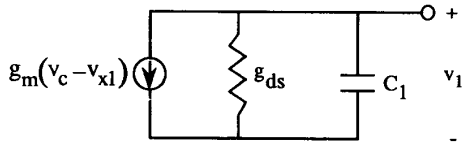

Figure 3: Small Signal Model of Region 2

From this model, $V_1(t)$ can be determined for a ramp input clock signal decreasing at a rate of k_C volts/second. $V_1(t)$ for region 2 is

$$V_{1out}(t) = k_c \frac{AC_1}{B^2}\left[e^{-Bt/C_1} + \frac{Bt}{C_1} - 1\right] \tag{2}$$

Note that in region 2, $V_1(t)$ increases from G_{ND} and terminates at V_{TN} volts, as shown in Figure 4. Assuming V_{DATA} is greater than V_{TN}, the circuit

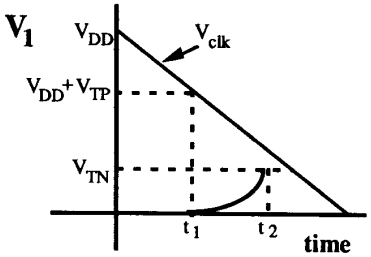

Figure 4: Region 2 Timing Diagram

will enter region 3, the regenerative region of operation. A and B in equation (2) represent the transconductance and output conductance of the single NAND gate (device A) in region 2, respectively, and are given by equations (3) and (4), respectively.

$$A = g_m' + g_{mp} - \frac{g_m' g_{n1}}{g_{n1} + g_{n2} + g_{mn}} \tag{3}$$

$$B = g_{ds} - \frac{g_m' g_{n1}}{g_{n1} + g_{n2} + g_{mn}} \tag{4}$$

where

$$g_m' = \frac{g_{mn} g_{n2}}{g_{n1} + g_{n2}} \tag{5}$$

$$g_{ds} = \frac{g_{n1} g_{n2}}{g_{n1} + g_{n2}} \tag{6}$$

g_{mn} and g_{mp} are the transconductance of the N-channel tree and the P-channel tree of device A, respectively, when driven by the input clock signal. g_{n1} and g_{n2} are the output conductances of the two serial N-channel transistors of device A.

Region 3

Once V_1 reaches V_{TN} volts, N_{2B} is turned on (see Figure 1). If V_{DATA} is also greater than V_{TN} of the top N-channel device plus V_{DS} of the lower N-channel device, N_{1B} will also be turned on; with both on, current can flow between V_{DD} and ground. At some point in time, depending upon the transistor characteristics and the magnitude of V_{DATA} and V_1, the N-channel tree will sink more current than the P-channel tree will source. At this point, $V_2(t)$ will decrease from V_{DD} volts. Once V_2 decreases below $V_{DD} + V_{TP}$, P_{1A} will turn on and source additional current, furthering the rate of increase of V_1, as shown in Figure 5. This in turn will enhance the current sinking capability of the N-channel tree of the lower NAND gate, further decreasing V_2. Herein lies the closed loop regenerative mode of operation inherent to the bistable NAND gate circuit configuration and fundamental to the latching behavior of a register. Note that the circuit is a two time constant system.

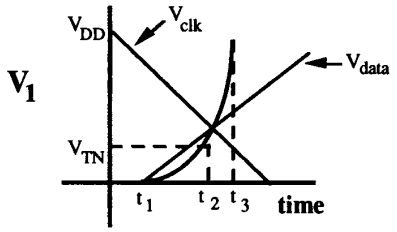

Figure 5: Region 3 Timing Diagram

At a certain operating point, the data is fully latched into the register and the clock input signal can be returned to V_{DD} and the state of the register will still enter its correct state ($V_1 = V_{DD}$ and $V_2 = 0$). This irreversible latching point represents the limiting ability to latch data into a register and is further explored in section 3 of this paper.

The regenerative circuit configuration of region 3 can be represented by the small signal models depicted in Figures 6 and 7, where Figure 6 represents the small signal model for the upper NAND gate, A, and Figure 7 represents the small signal model for the lower NAND gate, B. Note that Figures 6 and 7 are coupled together through v_1 and v_2.

In the regenerative mode of region 3 with a decreasing ramp shaped clock input signal, $V_1(t)$ is composed of three terms [as shown in equation (7)]: one due to the initial condition of region 3, $V_{23}(0) = V_{TN}$; the second due to the input clock signal; and the third due to the input data signal.

$$V_1(t) = V_{1A} + V_{1C} + V_{1D} \quad (7)$$

The complete solution to equation (7) is provided in [9].

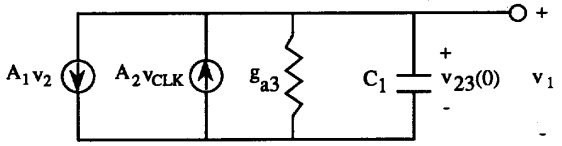

Figure 6: Small Signal Model of Device A in Region 3

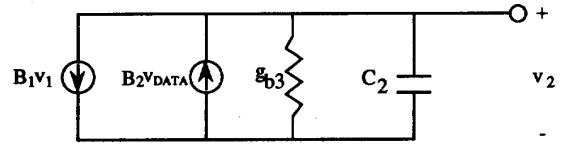

Figure 7: Small Signal Model of Device B in Region 3

Each of the transconductance and output conductance terms shown in Figures 6 and 7 require definition. A_1 and B_1 represent the transconductance of the two feedback output voltages, V_2 and V_1, respectively. A_2 and B_2 are the transconductances of the input clock and data signals, respectively. A_1, B_1, A_2, and B_2 are described in equations (8) - (11) in terms of their small signal parameters.

$$A_1 = \frac{g_{mn1a}\, g_{mn2a}}{g_{n2a} + g_{mn1a}} - g_{mp1a} \quad (8)$$

$$B_1 = \frac{g_{mn1b}\, g_{mn2b}}{g_{n2b} + g_{mn1b}} - g_{mp1b} \quad (9)$$

$$A_2 = \frac{g_{mn1a}\, g_{n2a}}{g_{n2a} + g_{mn1a}} - g_{mp2a} \quad (10)$$

$$B_2 = \frac{g_{mn1b}\, g_{n2b}}{g_{n2b} + g_{mn1b}} - g_{mp2b} \quad (11)$$

where g_{n2a} (g_{n2b}) is the output conductance of the lower N-channel transistor of device A (device B), g_{mn1a} and g_{mn2a} (g_{mn1b} and g_{mn2b}) are the transconductances of the top and bottom N-channel transistors of device A (device B), and g_{mp1a} and g_{mp2a} (g_{mp1b} and g_{mp2b}) are the transconductances of the two P-channel transistors of device A (device B), as shown in Figure 1.

Region 4

As V_1 increases toward V_{DD} and as V_2 decreases toward ground, V_{DS} across P_{1A}, P_{2A}, N_{1B}, and N_{2B} becomes very small, and both A_1 and A_2 approach zero. This breaks the regenerative loop of region 3, and the bistable register becomes once again an open loop single time constant system in which the P-channel devices of device A charge the capacitor C_1 up to V_{DD} (see Figure 8). Equation (12) defines $V_1(t)$ within region 4 where

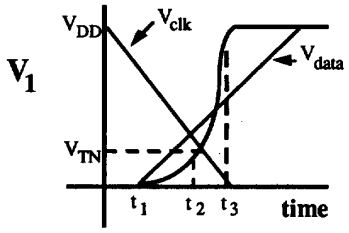

Figure 8: Region 4 Timing Diagram

$V_{34}(0)$ is the initial condition of region 4 and g_{a4} is the output conductance of device A in region 4.

$$V_{1out}(t) = V_{DD} - [V_{DD} - V_{34}(0)]\, e^{g_{a4}/C_1} \quad (12)$$

Register Output Waveform

Figure 9 shows the output voltage waveform at node V_1 of the bistable register for an input clock signal decreasing at 1 volt/ns and a data signal increasing at 1 volt/ns skewed from the clock signal, $T_{D\text{-}C}$, by 1 ns. This analytically derived output waveform is compared to a waveform generated from the SPICE circuit simulator program [11] using Level 2 I-V MOSFET equations with the same circuit, geometric, and process characteristics. Close agreement within each region is apparent.

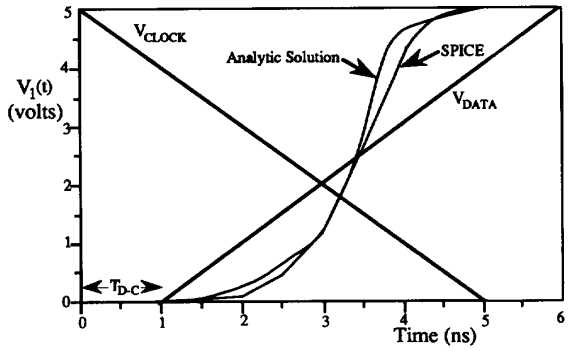

Figure 9: Transient Response of Bistable Register

3. CONDITIONS FOR LATCHING

As mentioned above, necessary and sufficient conditions are required to irreversibly latch data into a bistable register. This latch condition, which occurs in region 3, permits the development of fundamental limiting relationships which define whether the bistable register will latch, not latch, or become metastable. Once a register has correctly latched, the clock signal can be returned to V_{DD} and still the register will maintain its correct state. The time required to satisfy these limiting conditions is the minimum required time for a CMOS bistable register to latch, assuming a given set of input signal, geometric, and process conditions.

Necessary and Sufficient Conditions for Latching

Equations (13) through (16) give the four necessary and sufficient conditions for latching data into a bistable register.

$$V_{CLK} < V_{DD} + V_{TP} \quad (13)$$

$$V_{DATA} > V_{TN} + V_{X2} \quad (14)$$

$$A_1 V_2 + A_2 V_{CLK} > 0 \quad (15)$$

$$B_1 V_1 + B_2 V_{DATA} > 0 \quad (16)$$

The terms A_1, A_2, B_1, and B_2 are the transconductance parameters described in region 3 and given as equations (8) - (11). Equation (15) states that the P-channel tree in device A sources more current than the N-channel tree in device A sinks, thereby increasing V_1. Equation (16) states that the N-channel tree in device B sinks more current than the P-channel tree in device B sources, thereby decreasing V_2. If these four conditions are satisfied for all operating points within region 3, the device will latch.

Limiting Requirement for Latching

Equation (15) provides the fundamentally limiting condition for latching. If in device A, the P-channel tree sources more current than the N-

channel tree sinks, V_1 will increase. As V_1 increases, it turns on N_{2B} more strongly, increasing I_{NB} of device B, thereby decreasing V_2. This, in turn, further turns on P_{1A} which increases V_1. Thus, the transconductance term A_1, used in equation (15) and defined in equation (8), contains the limiting condition for latching.

To further exemplify the latching requirement, consider the situation, shown in Figure 10, where the clock signal V_{CLK} decreases from V_{DD}. If the limiting condition for latching can be satisfied before V_{CLK} reaches 0 volts, then the clock waveform can be returned to V_{DD} before it reaches 0 volts while still sucesssfully latching the data signal. The minimum value of voltage that V_{CLK} reaches just before it returns to V_{DD} is described as $V_{CLK}(min)$. Once $V_{CLK}(min)$ is reached (see Figure 10) and the clock signal is returned to V_{DD}, V_2 will continue to decrease further from V_{DD}. If at the operating point, $V_{CLK} = V_{DD} + V_{TP}$ (P_{2A} becomes cutoff), the current supplied by P_{1A} (and driven by V_2) is larger than the current sunk by the N-channel tree of device A, thereby maintaining a monotonically increasing voltage at V_1, the device will latch. The time for V_{CLK} to decrease from V_{DD} to $V_{CLK}(min)$ and return to $V_{DD} + V_{TP}$ is the minimum amount of time (i.e., the minimum latch time) for the data to successfully latch into the bistable register. This condition can be represented by the inequality shown below:

$$A_1V_2 > A_2V_{CLK} \text{ and } A_1V_2 \text{ is a positive quantity} \qquad (17)$$

In terms of the small signal parameters of equation (8), equation (17) can be presented as

$$g_{mp1a} > g_{mn} = \left.\frac{g_{mn1a}g_{mn2a}}{g_{n2a}+g_{mn1a}}\right|_{V_{CLK+}=V_{DD}+V_{TP}} \qquad (18)$$

where V_{CLK+} represents the operating point at which $V_{CLK} = V_{DD} + V_{TP}$ after reaching its minimum value and rising to $V_{DD} + V_{TP}$ (see Figure 10). Equation (18) represents the fundamentally limiting condition for latching data into a CMOS bistable register.

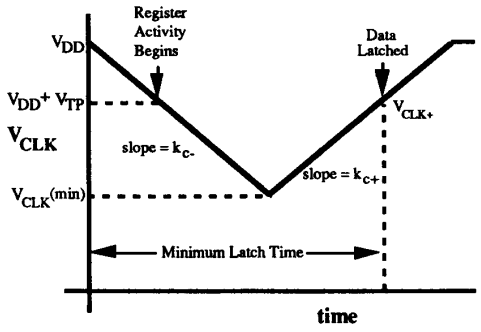

Figure 10: Timing Diagram of Limiting Condition for Latching

Table I describes an example circuit which operates just at the latch breakpoint. One parameter, V_{DATA}, is varied to exemplify the limiting nature of equation (18). The other circuit characteristics are kept constant and are listed below:

$V_{CLK}(min) = 1.7$ volts
$K_p', K_n' = 4.316 \times 10^{-5}$ amperes/volt^2
$k_{c-}, k_{c+} = 1$ volt/nanosecond
W/L ratio = 5

Table I: Example of Limiting Latch Condition

V_{DATA}	g_{mp}	g_{mn}	Latch?
2.55 volts	6.578x10-4℧	6.603x10-4℧	no
2.60 volts	7.907x10-4℧	7.907x10-4℧	breakpoint
2.65 volts	1.548x10-3℧	0	yes

Thus, Table I describes an experiment in which V_{DATA} is perturbed over a small range of voltage, keeping all other conditions constant. For the case where equation (18) is not satisfied (i.e., $g_{mn} > g_{mp}$), the data does not successfully latch into the register. For the case where equation (18) is satisfied (i.e., $g_{mp} > g_{mn}$), the data latches successfully into the register. Finally, for the interesting breakpoint case, where g_{mp} equals g_{mn}, the output voltage enters what is effectively a metastable state [3-8]. As long as $g_{mn} = g_{mp}$, the register remains in the metastable state.

4. CONCLUSIONS

Closed form solutions of each of the four regions of operation of a bistable register have been developed. Close agreement with a SPICE generated output response of a CMOS bistable register was shown. Necessary and sufficient conditions for latching data into a bistable register were developed. From these conditions, the limiting requirement for latching, not latching, and becoming metastable in a CMOS bistable register is defined. This result was corroborated by testing equation (18) at $V_{CLK+} = V_{DD} + V_{TP}$ with breakpoint conditions, and the result fully agreed with expectations. From these results, fundamentally limiting conditions for analyzing the latching mechanism in a CMOS bistable register are described.

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