Transient *IR* Voltage Drops in CMOS-Based Power Distribution Networks

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Abstract— **Decreased power supply levels have reduced the tolerance to voltage changes within power distribution networks in CMOS integrated circuits. High on-chip currents, required to charge and discharge large on-chip loads while operating at high frequencies, produce significant transient *IR* voltage drops within a power distribution network. Analytical expressions characterizing these transient *IR* voltage drops are presented in this paper. The peak value of the transient *IR* voltage drops based on the analytical expressions is within 6% as compared to SPICE. Circuit- and layout-level design constraints to manage the peak value of the transient *IR* voltage drops are also discussed.**

I. Introduction

As modern VLSI technology moves into the very deep submicrometer (VDSM) regime, millions of transistors will be integrated onto a single chip (a system-on-a-chip), operating at frequencies much greater than a gigahertz. The die size is expected to increase from $400\,\text{mm}^2$ in 1999 to $1120\,\text{mm}^2$ by 2009 while average on-chip currents will increase from 50 amperes in 1999 to 190 amperes by 2009 [1]. Power distribution networks in high complexity CMOS integrated circuits must be able to provide sufficient current to support average and peak power demand within all parts of an integrated circuit [2–4]. The large chip dimensions and on-chip average currents require special design strategies to maintain a constant voltage supply within a power distribution network [5, 6].

The voltage supply is expected to decrease from 1.8 volts in 1999 to 0.9 volts by 2009 [1], reducing the tolerance to voltage changes within a power distribution network. Because of the lossy characteristics of the metal interconnections in CMOS integrated circuits, *IR* voltage drops within a mesh structured power distribution network are no longer negligible [7, 8]. For example, metal 4 in the Alpha 21164 provides the power supply for each element within the entire integrated circuit [9]. The thickness of metal 4 is $1.53\,\mu\text{m}$ and the pitch is $6.0\,\mu\text{m}$ [3]. The average on-chip current is about 15 amperes. The current density is approximately $1.2\,\text{mA}/\mu\text{m}^2$ and the current is about 5.5 mA for a $3.0\,\mu\text{m}$ wide line. For a 9.0 mm long aluminum power line with a resistivity of $4.0\,\mu\Omega$-cm, a parasitic line resistance of $59\,\Omega$ results in an average *IR* voltage drop of close to 0.33 volts, which is about 10% of the voltage supply (3.3 volts for the Alpha 21164). Transient *IR* voltage drops which occur during logic transitions in a synchronous CMOS integrated circuit are even greater than these average *IR* voltage drops.

Therefore, significant transient *IR* voltage drops can occur in a synchronous CMOS integrated circuit [10]. These *IR* voltage drops can create delay uncertainty within data paths due to momentary changes in the power supply voltage, making the maximum and minimum propagation delays difficult to estimate, such as needed in the design of high performance clock distribution networks [11].

An analysis of transient *IR* voltage drops is presented in this paper. The MOS transistors are characterized by the nth power law I-V model [12]. Analytical expressions describing these transient *IR* voltage drops are developed based on an assumption of a fast ramp input signal. The peak *IR* voltage drops are shown to occur when the input signal completes a transition. The peak value of the transient *IR* voltage drops based on the analytical expressions is within 6% as compared to SPICE. Circuit- and layout-level design constraints are also addressed to manage the maximum *IR* voltage drops.

Analytical expressions characterizing these transient *IR* voltage drops are developed in Section II. A comparison of the analytical result with SPICE and discussions of circuit- and layout-level constraints are presented in Section III followed by some concluding remarks in Section IV.

II. Modeling of Transient *IR* Voltage Drops

Transient *IR* voltage drops are caused by a large number of logic gates switching close to the same time in a synchronous integrated circuit. For a switching CMOS logic gate, the current through the power lines is assumed to be m times greater than the current through a single CMOS logic gate. This assumption is equivalent to m simultaneously triggered logic gates connected to the same power line.

An analytical expression characterizing the transient *IR* voltage drops on the ground rail is developed in this section for a high-to-low output transition. $R_{V_{ss}}$ is the par-

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asitic resistance of the ground rail. In order to derive an analytical expression characterizing the transient *IR* voltage drops on the power rail, the short-circuit current is neglected based on an assumption of a fast ramp input signal [13],

$$V_{in}(t) = \frac{t}{\tau_r} V_{dd} \quad \text{for} \quad 0 \leq t \leq \tau_r, \tag{1}$$

permitting the current through the PMOS transistor to be neglected.

Once the input voltage exceeds the threshold voltage of the NMOS transistor, the NMOS transistor turns ON and is assumed to operate solely in the saturation region during the input transition. The drain-to-source current in this region is

$$I_{DS} = B_n(V_{in} - V_{TN} - mR_{V_{ss}} I_{DS})^{n_n}. \tag{2}$$

Assuming that $mR_{V_{ss}} I_{DS}$ is less than $V_{in} - V_{TN}$, the drain-to-source current can be approximated as

$$I_{DS} = \frac{B_n(V_{in} - V_{TN})^{n_n}}{1 + mR_{V_{ss}} n_n B_n (V_{in} - V_{TN})^{(n_n - 1)}}. \tag{3}$$

Therefore, the transient *IR* voltage drops in this region are

$$V_{IR} = mR_{V_{ss}} \frac{B_n(\frac{t}{\tau_r} V_{dd} - V_{TN})^{n_n}}{1 + mR_{V_{ss}} n_n B_n (\frac{t}{\tau_r} V_{dd} - V_{TN})^{(n_n - 1)}}, \tag{4}$$

for $\tau_n \leq t \leq \tau_r$ and $\tau_n = \frac{V_{TN}}{V_{dd}} \tau_r$. Transient *IR* voltage drops reach a maximum voltage at $t = \tau_r$,

$$V_{IR,max} = mR_{V_{ss}} \frac{B_n(V_{dd} - V_{TN})^{n_n}}{1 + mR_{V_{ss}} B_n (V_{dd} - V_{TN})^{n_n - 1}}. \tag{5}$$

The NMOS transistor is assumed to remain saturated when the input transition is completed. The drain-to-source current is a constant, independent of the output voltage. The transient *IR* voltage drops in this region are the same as $V_{IR,max}$.

After τ_{sat}, the NMOS transistor operates in the linear region. In order to derive a tractable expression, the drain-to-source current is characterized by $\gamma_n V_{DS}$, where γ_n is the effective output conductance of the NMOS transistor. The transient *IR* voltage drops in this region can be characterized as

$$V_{IR} = V_{IR,max} e^{-\alpha(t - \tau_{sat})} \quad \text{for} \quad t \geq \tau_{sat}, \tag{6}$$

where $\alpha = \frac{\gamma_n}{C_L(1 + mR_{V_{ss}} \gamma_n)}$ and C_L is the load capacitance. However, the effective output conductance of a MOS transistor also depends upon the output voltage in the linear region, changing from γ_{nsat} to $2\gamma_{nsat}$ [12]. In order to accurately characterize the transient *IR* voltage drops in the linear region, a value of γ_n is chosen between γ_{nsat} and $2\gamma_{nsat}$.

III. Characteristics of Transient *IR* Voltage Drops

The waveform and peak value of the transient *IR* voltage drops based on (5) are compared to SPICE in Section III-A. Circuit- and layout-level design constraints to manage the peak value of the transient *IR* voltage drops are discussed in Sections III-B and III-C, respectively.

A. Comparison with SPICE

A comparison of the analytical expression characterizing the waveform of the transient *IR* voltage drops with SPICE is shown in Fig. 1 for both the V_{ss} and V_{dd} rails. The transient *IR* voltage drops at the V_{ss} rail increase the potential on the V_{ss} rail, while the transient *IR* voltage drops at the V_{dd} rail decrease the potential on the V_{dd} rail, as shown in Fig. 1. Thus, the overall voltage swing is decreased, degrading system speed. Transient *IR* voltage drops on the power supply rails increase the effective gate voltage required to turn on the MOS transistors ($V_{GS} = V_{TN} + V_{IR}$ for the NMOS transistor). Note that the analytical prediction is quite close to SPICE. The difference is caused by the effective output conductance of the MOS transistors changing from γ_{sat} to $2\gamma_{sat}$ in the linear region [12].

The results of comparing the peak value of the transient *IR* voltage drops with SPICE are listed in Tables I and II for both the high-to-low and low-to-high output transitions, respectively, with $w_n = 1.8\,\mu$m, $w_p = 3.6\,\mu$m, and $C_L = 0.1$ pF. The peak value of the transient *IR* voltage drops based on (5) is within 6% of SPICE.

B. Circuit-level constraints

Assuming the maximum *IR* voltage drops should be less than a critical voltage V_c, the product of m and $R_{V_{ss}}$ must satisfy

$$mR_{V_{ss}} \leq \frac{V_c}{B_n(V_{dd} - V_{TN})^{n_n} - V_c B_n (V_{dd} - V_{TN})^{n_n - 1}}. \tag{7}$$

The constraint defined in (7) demonstrates that the product of m and $R_{V_{ss}}$ should be less than a constant determined by the right hand side of (7). Therefore, the maximum parasitic resistance of a power rail can be determined for a fixed m; the maximum number of simultaneously triggered logic gates can also be determined for a target power rail resistance of $R_{V_{ss}}$ as shown in Fig. 2(a).

C. Layout-level constraints

For a metal interconnection, the parasitic resistance can be expressed as

$$R = \rho \frac{l}{wt}, \tag{8}$$

TABLE I

COMPARISON OF PEAK *IR* VOLTAGE DROPS ON THE V_{ss} RAIL WITH SPICE

$R_{V_{ss}}$ (Ω)	τ_r (ps)	m	Analytic (V)	SPICE (V)	δ (%)
40.0	100	20	0.971	0.968	0.3
		15	0.786	0.800	1.8
		10	0.569	0.595	4.4
	150	20	0.971	0.945	2.8
		15	0.785	0.780	0.6
		10	0.568	0.578	1.7
	200	20	0.971	0.931	4.3
		15	0.785	0.767	1.0
		10	0.568	0.569	0.2
30.0	100	20	0.785	0.786	0.1
		15	0.626	0.641	2.3
		10	0.445	0.468	4.9
	150	20	0.785	0.766	2.5
		15	0.626	0.624	0.3
		10	0.445	0.455	2.2
	200	20	0.785	0.754	4.1
		15	0.626	0.614	2.0
		10	0.445	0.447	0.4
20.0	100	20	0.568	0.571	0.5
		15	0.445	0.458	2.8
		10	0.311	0.329	5.5
	150	20	0.568	0.556	2.2
		15	0.445	0.445	0.0
		10	0.311	0.319	2.5
	200	20	0.568	0.546	4.0
		15	0.445	0.439	1.4
		10	0.311	0.313	0.6
Maximum error					5.5
Average error					2.0

TABLE II

COMPARISON OF PEAK *IR* VOLTAGE DROPS ON THE V_{dd} RAIL WITH SPICE

$R_{V_{dd}}$ (Ω)	τ_f (ps)	m	Analytic (V)	SPICE (V)	δ (%)
40.0	100	20	4.07	3.95	3.0
		15	4.23	4.13	2.4
		10	4.43	4.35	1.8
	150	20	4.07	3.99	2.0
		15	4.23	4.16	1.7
		10	4.43	4.37	1.4
	200	20	4.07	4.00	1.8
		15	4.23	4.18	1.2
		10	4.43	4.39	0.9
30.0	100	20	4.23	4.13	2.4
		15	4.37	4.29	1.9
		10	4.54	4.48	1.3
	150	20	4.23	4.16	1.7
		15	4.37	4.32	1.2
		10	4.54	4.50	0.9
	200	20	4.23	4.18	1.2
		15	4.37	4.33	0.9
		10	4.54	4.52	0.4
20.0	100	20	4.43	4.35	1.8
		15	4.54	4.48	1.3
		10	4.67	4.63	0.8
	150	20	4.43	4.38	1.1
		15	4.54	4.50	0.9
		10	4.67	4.65	0.4
	200	20	4.43	4.39	0.9
		15	4.54	4.52	0.4
		10	4.67	4.66	0.2
Maximum error					3.0
Average error					1.3

where ρ is the resistivity of the material, and l, w, and t are the length, width, and thickness of the metal line, respectively. In practical CMOS integrated circuits, the current density must be less than a limit set by the electromigration constraint [8]. Therefore, for a metal interconnection with a fixed thickness, the minimum width and maximum length of the metal line can be determined by combining (7) and (8). The maximum length of the power supply rail with $w = 3.0\ \mu$m, $t = 1.53\ \mu$m, and $\rho = 4.0\ \mu\Omega$-cm is shown in Fig. 2(b).

Both (7) and (8) provide design guidelines for managing the transient *IR* voltage drops within a power distribution network. The use of additional power planes is an effective design technique to reduce the peak value of the transient *IR* voltage drops, significantly reducing the parasitic resistance associated with a power distribution network.

IV. CONCLUSIONS

An analytical model and design constraint expressions characterizing transient *IR* voltage drops are presented in this paper. The peak *IR* voltage drops occur when the input signal completes a transition (for a fast ramp input signal). The peak value of the transient *IR* voltage drops based on the proposed analytical expression is within 6% as compared to SPICE. Circuit- and layout-level design constraints are also addressed to manage the maximum value of the transient *IR* voltage drops, providing guidelines for the design of power distribution networks.

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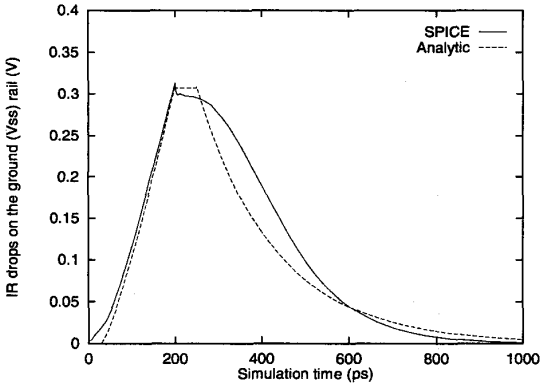
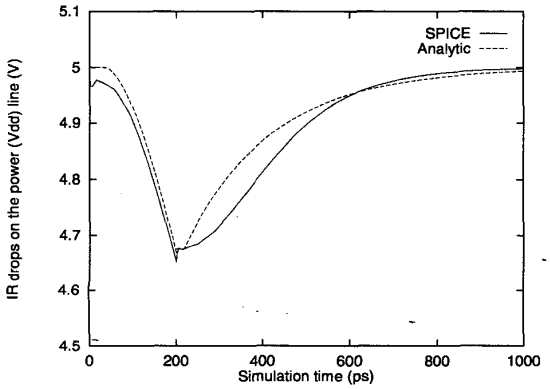
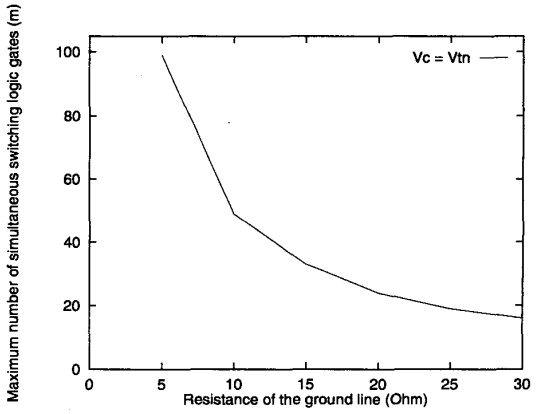


(a) $R_{V_{ss}} = 20.0\,\Omega$, $C_L = 0.1\,\text{pF}$, and $\tau_r = 0.20\,\text{ns}$

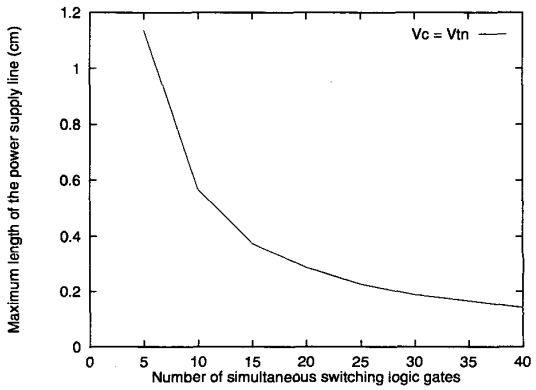


(b) $R_{V_{dd}} = 20.0\,\Omega$, $C_L = 0.1\,\text{pF}$, and $\tau_f = 0.20\,\text{ns}$

Fig. 1. Comparison of the analytical waveform of transient *IR* voltage drops with SPICE for $w_n = 1.8\,\mu\text{m}$, $w_p = 3.6\,\mu\text{m}$, and $m = 10$.



(a) Maximum number of simultaneously switching logic gates versus the ground line resistance.



(b) Maximum length of the power supply rail versus the number of simultaneously switching logic gates with $w = 3.0\,\mu\text{m}$, $t = 1.53\,\mu\text{m}$, and $\rho = 4.0\,\mu\Omega\text{-cm}$.

Fig. 2. Maximum number of simultaneously switching logic gates and maximum length of the power supply rail for $V_c = V_{TN}$.

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