On the Stability of Distributed On-Chip Low Dropout Regulators

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***Abstract*—Distributed on-chip low dropout (LDO) voltage regulators have become common due to the increasing number of on-chip voltage domains, dynamic voltage scaling, and the need for high quality power. Due to the current limitations of on-chip LDOs, hundreds of these regulators are required to deliver high quality power within modern high performance microprocessors. As the number of parallel connected LDOs increases, however, the stability of the power grid degrades due to the off-chip and in-package parasitic inductance. In this paper, the stability of the on-chip power grid composed of multiple distributed LDO regulators is evaluated from the perspective of the parasitic impedance. The relation between the grid stability and the number of LDOs that share the grid is described, and a guideline for evaluating grid stability is proposed. Moreover, several design solutions are offered to compensate for the off-chip inductance to enhance the stability of on-chip power grids, supporting the deployment of a large number of LDO regulators.**

I. Introduction

Distributed on-chip low dropout (LDO) regulators have been proposed to enhance on-chip quality of power (QoP) [1]–[3]. Due to the advantages of fast regulation and small size, a large number of LDOs can be deployed within an integrated circuit (IC), supporting higher granularity and local power management [4], [5]. By minimizing the distance between the regulator and the load, the response time is further improved, supporting sub-μs dynamic voltage scaling (DVS) [6]. Moreover, due to the fast response of on-chip regulators, the time to exit and enter sleep modes for low power applications is reduced [7].

Modern state-of-the-art microprocessors require hundreds of amperes to operate at high performance [8]. Due to the limited output current of on-chip capacitor-less LDOs [9], [10], hundreds of these regulators are required to regulate the power of high performance microprocessors. A power delivery system that contains multiple on-chip LDO regulators can however exhibit instability [2], [3]. Previous work on the stability of capacitor-less on-chip LDOs has focused on a single LDO and does not consider the overall power delivery system [9], [11]–[14]. In [3], the stability of distributed LDOs that share a common grid is considered. This work however does not consider off-chip parasitic impedances which can significantly degrade the stability of an on-chip power grid. The analysis proposed in [2] considers the parasitic network of the off-chip as well as on-chip interconnects, and provides a comprehensive discussion of the stability of the on-chip power grid. This analysis however does not provide intuition and guidelines to design a power delivery system composed of distributed LDO regulators. The sources of instability in a complex power grid shared by a large number of LDO regulators also remain unclear.

In this paper, the effects of the off-chip parasitic impedance on a power delivery system composed of distributed LDO regulators are considered. The relationship between the number of LDOs and the grid stability is described, and a methodology is proposed to evaluate the stability for the specific condition when the LDO regulators operate under the same load. Moreover, several solutions are proposed to compensate for the parasitic network to enhance stability when deploying a large number of on-chip LDO regulators. In section II, the stability of a parallel connected LDO network incorporating off-chip and in-package parasitic inductances is described. Moreover, the stability in terms of the number of LDOs as well as a circuit model for evaluating the system are discussed. In section III, solutions to enhance the stability of an inductive power delivery system are proposed. In section IV, some conclusions are offered.

II. Stability of Parallel Connected LDOs

To evaluate the effects of the off-chip parasitic impedance on the stability of a grid composed of many distributed LDOs, a set of parallel connected LDOs are considered with an RLC network representing the parasitic impedance of the package and printed circuit board (PCB), as shown in Fig. 1a. Here, a conventional LDO comprised of a single error amplifier with a single pass transistor is considered. The pass transistor controls the load from the input to the output of the LDO regulator. The effect of the on-chip RLC network on the stability of the LDO is neglected since the on-chip inductance and capacitance are orders of magnitude smaller than the off-chip and in-package parasitic inductance and capacitance [15].

To illustrate the effects of an LC network on the stability of a distributed system of on-chip LDO regulators, consider the case where the LDOs share a common load. Although this condition reflects a constrained case (e.g., a multicore processor), this application describes the potential degradation in stability when a set of LDOs perform under a balanced load condition. Under this condition, a model of the system is shown in Fig. 1b. This system of parallel connected LDOs can be reduced to the circuit model shown in Fig. 2.

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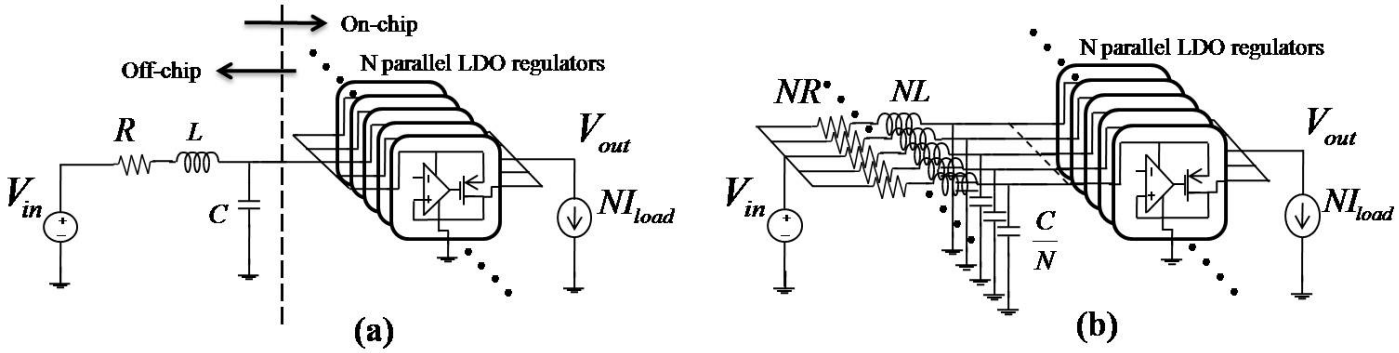

Fig. 1: Simplified model of the power delivery system with distributed LDOs, (a) with the off-chip parasitic impedance network, and (b) distribution of the parasitic impedance when the LDOs operate under similar load conditions.

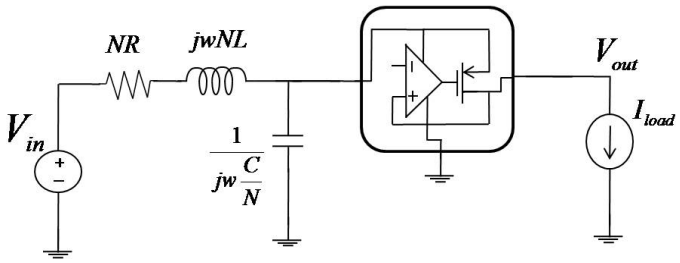

Fig. 2: Reduced circuit model of a set of parallel connected LDOs operating under similar load conditions.

The reduction of this complex system into a single LDO regulator connected to a parasitic impedance network with a single closed loop greatly simplifies the stability analysis. This simplification can be used to provide intuition into the relationship between the number of LDOs and the stability of the power grid. In section II-A, the effect of the LC resonance on system stability is explained. In section II-B, the requirements for a stable distributed LDO system are discussed.

A. Sources of Instability

The stability of a system depends upon the loop gain and phase of that system. The system becomes unstable if the loop gain is greater than unity when the phase is below 0^o. To analyze the stability, a small-signal model of the simplified circuit model, shown in Fig. 3, is used.

The LDO is modeled as a two pole system [10]. The dominant pole is generated by the error amplifier. The second pole is from the capacitor at the output (C_{out}) of the LDO regulator. The parasitic impedance at the input of the LDO regulator is shown in Fig. 3. The open loop gain of the LDO regulator is

$$\frac{V_{out}}{V_{in}} \approx -\frac{A_{ol}}{(1+sC_{ea}r_{ea})(1+sC_{out}(r_o+g_m r_o Z))}, \quad (1)$$

$$A_{ol} = g_m r_o A_{ea}, \quad (2)$$

$$A_{ea} = g_{m_{ea}} r_{ea}, \quad (3)$$

$$Z = \frac{R+sL}{1+sRC+s^2LC}, \quad (4)$$

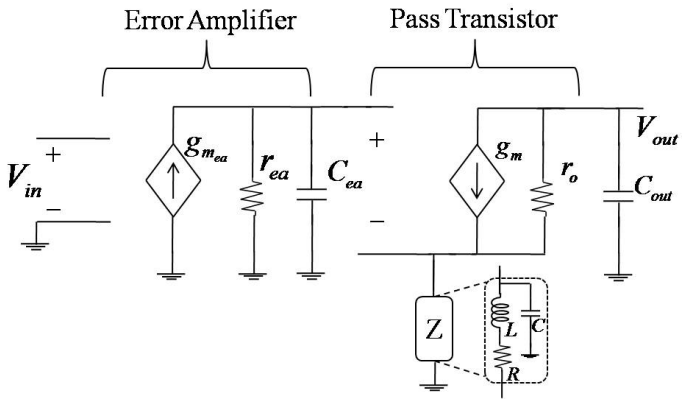

Fig. 3: Small-signal model of the simplified circuit shown in Fig. 2.

where R, L, and C are, respectively, the parasitic resistance, inductance, and capacitance at the input, and A_{ol} and A_{ea} are, respectively, the open-loop gain of the LDO regulator and the error amplifier over the midband frequency range. Considering the parasitic impedance at the input of the LDO regulator, two additional poles and zeros form within the system. The LC pair forms a resonant frequency which is the source of instability. The resonant frequency is

$$f_{res} = \frac{1}{2\pi\sqrt{LC}}. \quad (5)$$

The spike formed at the frequency of resonance is further exacerbated as the number of on-chip LDOs grows since the inductance and capacitance per LDO, respectively, increases and decreases by the total number of LDOs. Since the off-chip and in-package inductance can be as high as hundreds of pH [15], the parasitic inductance at the input of hundreds of distributed on-chip regulators can be on the orders of nH. The magnitude of the resonant spike therefore increases, significantly degrading the phase, potentially resulting in a finite gain above the unity gain frequency of the regulator. SPICE simulations demonstrating this effect are shown in Fig. 4.

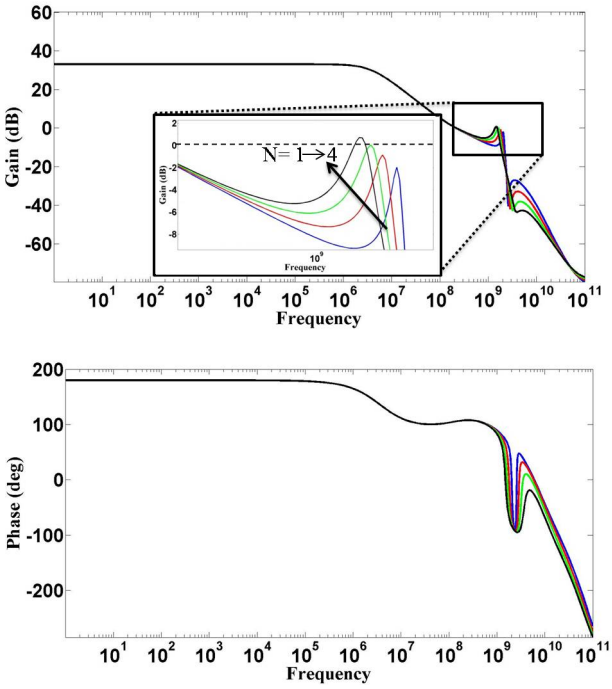

Fig. 4: Effect of increasing the number of parallel LDOs on (a) the loop gain, and (b) phase. With four parallel LDOs, the loop gain rises above 0 dB beyond the unity gain frequency, producing an unstable system.

B. Condition for Stability

The stability of a single capacitor-less on-chip LDO is limited by the minimum load condition (< 1 mA). To provide sufficient phase margin, the two poles need to be sufficiently apart in the frequency domain. Under heavy load conditions (> 100 mA), the pole due to the output capacitor moves to higher frequencies as compared to the dominant pole from the error amplifier. LDO stability is therefore maintained. In a system of parallel connected LDOs, however, due to the inductance of the parasitic impedance at the input of the LDOs, the loop gain exhibits a peak at the resonant frequency. Due to the non-monotonic behavior of the loop gain (see Fig. 4), a positive phase margin at the unity gain frequency does not guarantee system stability.

If the resonant spike is significant, the gain increases while lowering the phase below 0^o, causing instability. Due to the non-monotonic frequency response, the loop gain and phase have to be evaluated at both the resonant frequency and the unity gain frequency of the regulator. To ensure stability, the phase has to be greater than 0^o when the loop gain is greater than unity at all frequencies.

III. Enhancing Grid Stability

To compensate for the effect of the RLC network with a system of N LDO regulators, the inductance and capacitance are, respectively, decreased and increased by a factor of N. For a distributed power delivery system composed of hundreds of LDO regulators, this factor of N is impractical due to the finite inductance of the PCB traces and the C4 bumps

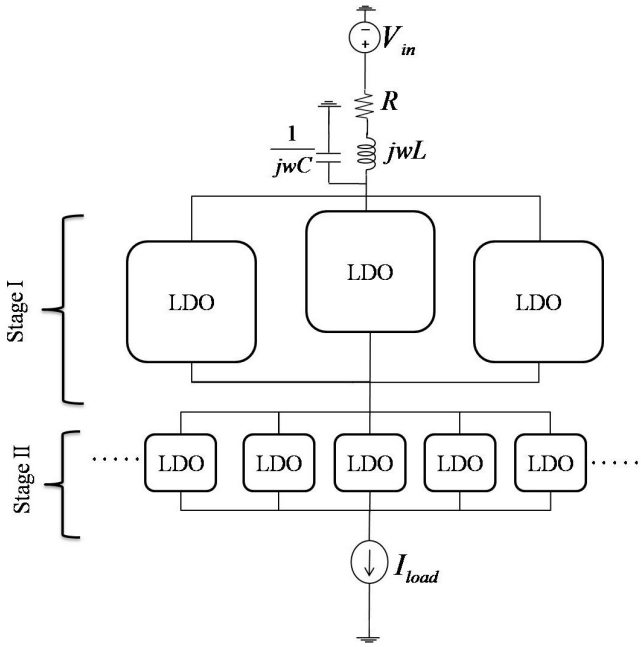

Fig. 5: LDO regulation in two stages where the first stage consists of fewer but larger LDO regulators and the second stage consists of smaller multiple LDO regulators.

[15]. Moreover, the size of the capacitor is limited by die and PCB area constraints. An in-package power supply [16] therefore provides enhanced grid stability as compared to a board level power supply. This approach however significantly increases packaging costs. An alternative lower cost approach is to provide LDO regulation in multiple stages.

A. Staged LDO Regulation

For a system composed of a large number of parallel connected LDOs, the significance of the RLC network increases, degrading grid stability as well as scalability of the power delivery system. To mitigate this issue, regulation can be provided in two stages, as shown in Fig. 5.

The first stage of the regulation system consists of a fewer number of LDOs that are larger in size to provide sufficient current to the second stage LDOs that are smaller in size but greater in number. The benefits of dividing the regulation process into two stages are twofold. First, by requiring fewer LDOs at the input, the total input parasitic impedance decreases. The second benefit is the first stage isolates the off-chip parasitic impedance from the second stage group of LDOs. The transient behavior of a single stage is compared to two stage regulation in Fig 6.

Dividing the regulation process into stages significantly decreases the impedance at the input of the second stage. To illustrate the isolation capability of the first stage, consider the stacked LDO configuration shown in Fig. 7. The impedance at the input of the first stage is attenuated by the open loop gain of the error amplifier, significantly decreasing the load at the input of the second stage. The output impedance of the first and second stages in the midband frequency range are, respectively,

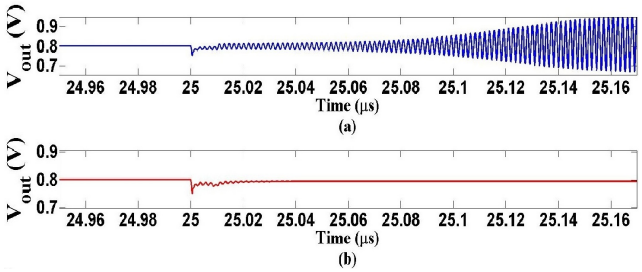

Fig. 6: Transient response of a power grid with four LDO regulators for $V_{in} = 1$ volt and $V_{out} = 0.8$ volts, assuming a load transition from 100 μA to 100 mA per LDO, (a) single stage regulation, and (b) two stage regulation with one LDO on the first stage.

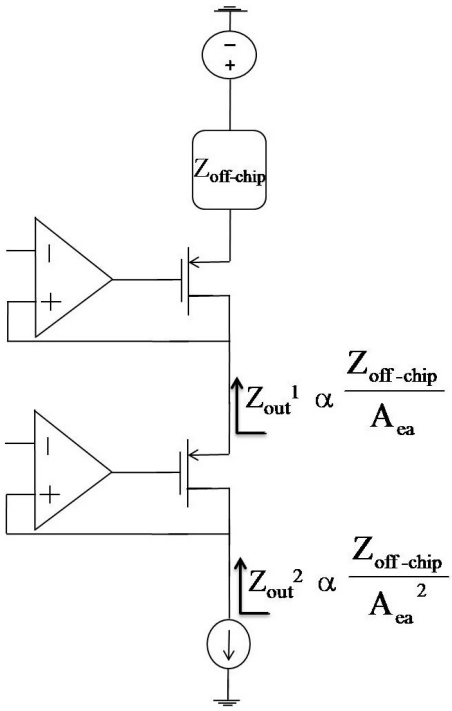

Fig. 7: Stacked LDO configuration to isolate the second stage from the parasitic impedance of the first stage.

$$Z^1_{out} \approx \frac{r_o}{1 + A_{ol}} + \frac{Z_{off-chip}}{A_{ea}}, \quad (6)$$

$$Z^2_{out} \approx \frac{r_o}{1 + A_{ol}} + \frac{r_o}{(1 + A_{ol})A_{ea}} + \frac{Z_{off-chip}}{A^2_{ea}}. \quad (7)$$

Since the parasitic impedance at the second stage is reduced, the capacitance required to compensate for the inductance decreases, supporting the use of a greater number of second stage LDOs. To not compromise the efficiency of the regulation system, the difference between the input and output voltages can be shared between the two stages. If this voltage is not sufficiently high, the size of the pass transistors can be increased to provide higher current while maintaining the output voltage.

IV. Conclusions

The stability of a power delivery system composed of distributed on-chip LDO regulators is explored in this paper. The stability of the system decreases as the number of regulators increases due to the RLC parasitic network impedance formed by the PCB traces and C4 bumps. The impedance at the input of each LDO increases as the number of regulators that share a common grid grows, exacerbating the resonant effect and resulting in an unstable system. To maintain stability, the phase margin at both the unity gain frequency and the resonant frequency of an LDO must be satisfied. To support a larger number of on-chip LDOs while maintaining a stable system, the regulation process can be composed of two stages. The first stage isolates the parasitic RLC network from the input of the following stages, allowing a larger number of distributed LDOs.

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