Inductive Noise Coupling in Superconductive Passive Transmission Lines

Gleb Krylov and Eby G. Friedman Department of Electrical and Computer Engineering University of Rochester Rochester, New York gkrylov@ur.rochester.edu

Abstract—Superconductive niobium-based circuits is a promising energy efficient beyond-CMOS technology that can supplement or replace existing large scale CMOS systems. Modern superconductive circuits utilize more than ten metal layers for gates and interconnect. Many sources of inductive coupling noise exist within this environment. Superconductive circuits are particularly vulnerable to inductive coupling, as the operation of the logic gates and flip flops depends on precise bias conditions, and the signal magnitude is relatively small. These inductive coupling sources are characterized, and the effects of inductive coupling noise in different circuit structures are described. Guidelines to mitigate the deleterious effects of coupling noise are presented.

Index Terms—Single flux quantum; superconductive integrated circuits; superconductive digital electronics

I. INTRODUCTION

Rapid single flux quantum (RSFQ) is an emerging beyond-CMOS technology which has recently attracted considerable attention as an energy efficient alternative to CMOS in high performance, stationary computing systems [1], [2]. Advances in fabrication [3] and design tools [4], [5] are enabling large scale SFQ-based superconductive systems which exhibit low power dissipation while achieving clock frequencies on the order of hundreds of gigahertz [6].

Modern superconductive niobium-based fabrication technologies support over ten metal layers. A significant portion of these metal layers, however, is occupied by the active parts of the logic cells; only a few metal layers are used for interconnect.

Large scale RSFQ circuits primarily use interconnect based on passive transmission lines (PTL) for routing signals among standard cells [7], [8]. This type of interconnect requires a driver/receiver circuit and a stripline or microstripline [9]. This interconnect topology poses unique challenges on the routing process, as the available routing resources are severely limited. Different alternative topologies have been considered to reduce the number of metal layers required by these structures [10], [11]. These alternative topologies, however, increase the inductive noise between adjacent striplines as compared to topologies with additional ground planes.

Fig. 1: Sources of inductive coupling noise in a superconductive IC (MIT LL SFQ5ee process [12]).

Sources of coupling noise are reviewed in Section II. Inductive coupling noise in common circuit structures is described in Section III. The effects of this coupling noise on circuit behavior are discussed in Section IV. The paper is concluded in Section V.

II. SOURCES OF INDUCTIVE COUPLING NOISE

Many sources of inductive coupling exist in complex multilayer ICs. PTL striplines are the primary type of transmission line for signal routing in VLSI RSFQ circuits [7]. The SFQ signals propagating along these lines can couple to other lines, producing noise, as shown in Figure 1. Coupling noise can produce erroneous switching [13] as well as reduce parameter margins [14]. In this section, these noise sources are described.

In modern superconductive circuit fabrication, the metal resources are severely limited [12]. State-of-the-art niobium fabrication facilities only provide up to ten niobium layers, where the JJs are between specific layers. Several of these layers are required for the Josephson junctions and related connections, reducing the number of available layers for routing [10]. A stripline within a PTL ideally consists of a signal line sandwiched between two ground planes. This structure is however impractical for large scale circuits.

The effort depicted is supported by the Department of Defense (DoD) Agency – Intelligence Advanced Research Projects Activity (IARPA) through the U.S. Army Research Office under Contract No. W911NF-17-9-0001. The content of the information does not necessarily reflect the position or the policy of the Government, and no official endorsement should be inferred.

Fig. 2: Topologies to allocate metal layers for two PTL routing strategies, (a) three ground planes [11], and (b) two ground planes [10].

Two approaches exist to reduce the number of layers used by PTLs, as shown in Figure 2. One approach is to use a shared ground plane between two PTLs [11], as depicted in Figure 2a. With this technique, five metal layers are necessary to produce two routing layers. Another approach is to utilize an asymmetric stripline, where two signal layers are sandwiched between two ground planes [10], as shown in Figure 2b. For each signal routing layer in this structure, the distance to the ground planes and therefore the thickness of the dielectric layers are different. Moreover, no ground plane exists between signal layers. This structure only requires four metal layers to produce two routing layers.

These approaches increase the mutual inductive coupling between striplines. A tradeoff exists between the pitch of the striplines and the mutual inductance. A smaller pitch increases the available routing resources while also increasing the coupling noise and decreasing the parameter margins. It is therefore important to characterize this tradeoff to determine the optimal pitch of the PTL tracks.

To evaluate the magnitude of the inductive coupling, inductance extraction tools are necessary. Field solvers are used to extract the coupling characteristics of these structures. FastHenry [15] is a popular and relatively accurate open source tool for inductance extraction of superconductive circuits. The inductance characteristics produced by these simulation tools can be used as guidelines for automated routing algorithms, as well as for the design of cell libraries. In the following sections, the magnitude and effects of inductive coupling noise are characterized to determine the minimum PTL track pitch and other guidelines for a variety of circuit structures and topologies.

III. INDUCTIVE COUPLING WITHIN COMMON CIRCUIT **STRUCTURES**

Although the topology of an IC layout is in general only limited by the design rules of the fabrication process, in a standard cell-based design flow, specific structures are common or ubiquitous. In this section, the coupling characteristics of these common circuit structures are described (based on FastHenry).

A. Existing experimental data

To verify the correctness and relative error of the extracted inductance, a comparison with data from other tools and/or

Fig. 3: Coupling between two identical parallel PTLs within the same layers with signal lines in M2 and M3.

experimental data is necessary. In this section, both the selfinductance and mutual inductance are compared to published experimental results.

The self-inductance of different structures in the MIT LL SFQ5ee process [12] is relatively well characterized. The selfinductance is determined in FastHenry by attaching a port to the input signal and ground planes, while shorting the output signal to ground. The self-inductance of different structures, extracted in FastHenry, is compared to existing experimental data. These self-inductances are in relatively close agreement – the error is on the order of 5%, sufficient for coupling noise evaluation.

The available data describing the mutual inductance within the SFQ5ee process is more scarce. The mutual inductance has been experimentally measured as part of the InductEx tool calibration process [16]. Mutual inductance extraction in FastHenry is similar to self-inductance extraction – an additional port is attached to the second inductor. In Table I, the experimental mutual inductance is compared to the inductance extracted from FastHenry. These inductances are within 5%, exhibiting sufficient agreement for coupling noise analysis.

B. Coupling between parallel PTL lines

In this section and the following sections, the PTL topology shown in Figure 2b is evaluated assuming $5.2 \mu m$ wide PTL signal lines and the ground planes in M1, M4, and M7. Structures with extended parallel PTL lines in close proximity generally exhibit the largest inductive coupling coefficient, on the order of 10[−]² for narrowly spaced lines. The dependence of this coupling coefficient on the separation between the signal lines is shown in Figure 3 for coupling between two M1-M2-M4 PTLs or two M1-M3-M4 PTLs. These PTLs share the same ground planes, M1 and M4. The coupling coefficient exponentially depends upon the separation between the signal lines.

TABLE I: Comparison of mutual inductance extracted in FastHenry with experimental data. The experimental data and layout topology are based on [16].

| Layers | Experimental M, pH | FastHenry M, pH | Difference | Experimental standard deviation |
|-------------|-----------------------|--------------------|------------|------------------------------------|
| M0-M1-M2-M7 | 3.37 | 3.58 | $+6.2\%$ | 1.12% |
| M1-M2-M3-M7 | 3.27 | 3.30 | $+0.9\%$ | 0.90% |
| M2-M3-M4-M7 | 3.04 | 3.13 | $+3.0\%$ | 2.04% |
| M3-M4-M5-M7 | 2.75 | 2.94 | $+6.9\%$ | 2.89% |
| M4-M5-M6-M7 | 1.95 | 1.89 | -3.2% | 1.43% |

Fig. 4: Two identical parallel PTLs in adjacent layers with signal lines in M2 and M3.

Fig. 5: Coupling between two identical parallel PTLs in adjacent layers with signal lines in M2 and M3.

For PTL signal lines in adjacent layers sharing the same ground planes, the dependence of the coupling noise on the separation between layers is similar. For the topology depicted in Figure 4 (PTLs in M1-M2-M4 and M1-M3-M4), this dependence is shown in Figure 5. The vertical separation between these lines slightly reduces the coupling coefficient.

Coupling between the PTLs separated by a ground plane, *e.g.* M1-M3-M4 and M4-M5-M7, is significantly smaller, by approximately an order of magnitude. Any stitching vias – vias connecting the ground planes of a stripline (*e.g.*, M1 and M4 in Figure 5) – further reduce the inductive coupling. Any vertical overlap between signal lines in adjacent layers (shown

Fig. 6: Two perpendicular PTLs in adjacent layers with signal lines in M2 and M3.

Fig. 7: Two perpendicular PTLs in adjacent layers with signal lines in M2 and M3 with a short overlap.

in Figure 7) drastically increases the coupling coefficient in proportion to the area of the overlap (or crossover).

C. Coupling between perpendicular PTL lines with and without overlap

To reduce coupling between PTLs in adjacent layers, the interconnect tracks in these layers can be routed in perpendicular directions, as shown in Figure 6 for PTLs in M1-M2-M4 and M1-M3-M4. This topology negates any effect from adjacent layer coupling – the coupling coefficient is reduced by two orders of magnitude as compared to the parallel case.

In a layout with highly constrained metal resources, some adjacent layer PTLs may require a short overlap to reduce routing congestion. This case is evaluated for the topology shown in Figure 7 – perpendicular PTLs in M1-M2-M4 and M1-M3-M4. The dependence of the coupling coefficient on the width of the overlap is shown in Figure 8. The zero

Fig. 8: Coupling between two perpendicular PTLs in adjacent layers with signal lines in M2 and M3 with a short overlap (see Figure 7).

Fig. 9: Inductive coupling between parallel PTLs showing the aggressor and victim lines.

on the horizontal axis corresponds to a simple crossing of perpendicular lines, while the larger offset corresponds to the length of the additional overlap. The coupling coefficient exhibits a linear dependence on the length of the overlap.

IV. EFFECTS OF COUPLING ON CIRCUITS AND MITIGATION GUIDELINES

The state of a circuit affects the sensitivity to parasitic coupling noise, producing several types of errors. In this section, the effects of coupling on the operation of PTLs are described.

An SFQ pulse traveling on an active (aggressor) PTL produces a transient current spike at the receiver of the passive (victim) line, as shown in Figure 9. Two cases are considered here, a small (\sim 0.01) coupling coefficient and a large (\sim 0.4) coupling coefficient. The case of a large coupling coefficient corresponds to PTLs in adjacent layers overlapping over a long distance. The case of a small coupling coefficient corresponds to all other practical routing topologies.

The effects of PTL coupling noise are evaluated in WRSPICE [17]. Since WRSPICE does not normally support coupled transmission lines, a decoupling technique for lossless transmission lines is used [18].

In the case of small coupling, any additional current at the receiver of the victim line is on the order of a few μ A – negligible as compared to the bias current of a typical PTL receiver. In this case, the coupling noise momentarily degrades the bias margins of the receiver when this parasitic current is present. The reduction in margins does not exceed a few per cent.

In the case of large coupling, the additional current at the receiver of the victim line can exceed tens to hundreds of μ A. This large current is typically not sufficient to switch the receiver junction of the victim line. If this coupled noise waveform however coincides with the signal waveform on the victim line, any additional current can prevent the Josephson junction in the receiver from switching. Unless the data signals on the aggressor and victim lines are synchronized to different phases of the same clock signal, this condition will eventually produce an error. To mitigate the effects of PTL coupling noise, the routing algorithm should avoid long overlapping PTLs in adjacent layers.

V. CONCLUSIONS

Inductive coupling noise is an important issue in large scale superconductive integrated circuits. Inductive coupling can reduce performance, introduce errors, and degrade parameter margins. RSFQ circuits are particularly vulnerable to inductive noise due to the highly sensitive gates and low signal amplitudes. In this paper, different sources of inductive noise in multi-layer standard cell RSFQ circuits are reviewed. The coefficient of inductive coupling for the MIT LL SFQ5ee process is determined for different common circuit structures. Based on the magnitude of the coupling, the effects of inductive noise on PTLs are described. Mitigation techniques to reduce the effects of inductive noise on the circuit behavior are presented, enabling higher density SFQ circuits with wider parameter margins.

REFERENCES

- [1] M. A. Manheimer, "Cryogenic Computing Complexity Program: Phase 1 Introduction," *IEEE Transactions on Applied Superconductivity*, vol. 25, no. 3, pp. 1–4, June 2015.
- [2] G. Krylov and E. G. Friedman, *Single Flux Quantum Integrated Circuit Design*, Springer, ISBN # 978-3-030-76884-3, 2022 (in press).
- [3] S. K. Tolpygo, V. Bolkhovsky, R. Rastogi, S. Zarr, A. L. Day, E. Golden, T. J. Weir, A. Wynn, and L. M. Johnson, "Advanced Fabrication Processes for Superconductor Electronics: Current Status and New Developments," *IEEE Transactions on Applied Superconductivity*, vol. 29, no. 5, pp. 1–13, August 2019.
- [4] K. Gaj, Q. P. Herr, V. Adler, A. Krasniewski, E. G. Friedman, and M. J. Feldman, "Tools for the Computer-Aided Design of Multigigahertz Superconducting Digital Circuits," *IEEE Transactions on Applied Superconductivity*, vol. 9, no. 1, pp. 18–38, March 1999.
- [5] K. Gaj, Q. P. Herr, V. Adler, D. K. Brock, E. G. Friedman, and M. J. Feldman, "Toward a Systematic Design Methodology for Large Multigigahertz Rapid Single Flux Quantum Circuits," *IEEE Transactions on Applied Superconductivity*, vol. 9, no. 3, pp. 4591–4606, September 1999.
- [6] W. Chen, A. V. Rylyakov, V. Patel, J. E. Lukens, and K. K. Likharev, "Rapid Single Flux Quantum T-Flip Flop Operating up to 770 GHz," *IEEE Transactions on Applied Superconductivity*, vol. 9, no. 2, pp. 3212– 3215, June 1999.
- [7] T. Jabbari, G. Krylov, S. Whiteley, E. Mlinar, J. Kawa, and E. G. Friedman, "Interconnect Routing for Large-Scale RSFQ Circuits," *IEEE Transactions on Applied Superconductivity*, vol. 29, no. 5, pp. 1–5, Art no. 1 102 805, August 2019.
- [8] T. Jabbari, G. Krylov, S. Whiteley, J. Kawa, and E. G. Friedman, "Repeater Insertion in SFQ Interconnect," *IEEE Transactions on Applied Superconductivity*, vol. 30, no. 8, pp. 1–8, Art no. 5 400 508, December 2020.
- [9] T. Jabbari, G. Krylov, J. Kawa, and E. G. Friedman, "Splitter Trees in Single Flux Quantum Circuits," *IEEE Transactions on Applied Superconductivity*, vol. 31, no. 5, pp. 1–6, Art no. 1 302 606, August 2021.
- [10] A. Inamdar, D. Amparo, B. Sahoo, J. Ren, and A. Sahu, "RSFQ/ERSFQ Cell Library with Improved Circuit Optimization, Timing Verification, and Test Characterization," *IEEE Transactions on Applied Superconductivity*, vol. 27, no. 4, pp. 1–9, June 2017.
- [11] C. J. Fourie, C. L. Ayala, L. Schindler, T. Tanaka, and N. Yoshikawa, "Design and Characterization of Track Routing Architecture for RSFQ and AQFP Circuits in a Multilayer Process," *IEEE Transactions on Applied Superconductivity*, vol. 30, no. 6, pp. 1–9, September 2020.
- [12] S. K. Tolpygo, V. Bolkhovsky, T. J. Weir, A. Wynn, D. E. Oates, L. M. Johnson, and M. A. Gouker, "Advanced Fabrication Processes for Superconducting Very Large-Scale Integrated Circuits," *IEEE Transactions on Applied Superconductivity*, vol. 26, no. 3, pp. 1–10, April 2016.
- [13] G. Krylov and E. G. Friedman, "Design for Testability of SFQ Circuits," *IEEE Transactions on Applied Superconductivity*, vol. 27, no. 8, pp. 1–7, Art no. 1 302 307, December 2017.
- [14] G. Krylov and E. G. Friedman, "Design Methodology for Distributed Large Scale ERSFQ Bias Networks," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 28, no. 11, pp. 2438–2447, November 2020.
- [15] Stephen R. Whiteley. FastHenry 3.0wr. [Online]. Available: http://www.wrcad.com/ftp/pub/readme.fasthenry
- [16] C. J. Fourie, C. Shawawreh, I. V. Vernik, and T. V. Filippov, "High-Accuracy InductEx Calibration Sets for MIT-LL SFQ4ee and SFQ5ee Processes," *IEEE Transactions on Applied Superconductivity*, vol. 27, no. 2, pp. 1–5, January 2017.
- [17] S. R. Whiteley, "Josephson Junctions in SPICE3," *IEEE Transactions on Magnetics*, vol. 27, no. 2, pp. 2902–2905, March 1991.
- [18] C. R. Paul, "A Simple SPICE Model for Coupled Transmission Lines," *Proceedings of the IEEE International Symposium on Electromagnetic Compatibility*, pp. 327–333, August 1988.