Optimum Wire Shaping of an RLC Interconnect

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Abstract—**The optimum wire shape for minimum signal propagation delay across an RLC line is shown to have a general exponential form. The line inductance makes exponential tapering more attractive for RLC lines than for RC lines. For RLC lines, optimum wire tapering achieves a higher reduction in the signal propagation delay as compared to uniform wire sizing. Wire tapering can reduce both the propagation delay and power dissipation. A reduction of 15% in the propagation delay and of 16% in the power is achieved for an example circuit.**

1 Introduction

Interconnect design has become a dominant issue in high speed integrated circuits (ICs). With the decreased feature size of CMOS circuits, on-chip interconnect now dominates both circuit delay and power dissipation. Many algorithms have been proposed to determine the optimum wire size that minimizes a cost function such as delay. It is shown in [1] that the optimum interconnect shape which minimizes the signal propagation delay in an RC interconnect is an exponential function. Different extensions to this work have been applied to consider other circuit parameters such as fringing capacitance [2]-[4].

Wire tapering increases the interconnect width at the near end (the driver end) of the line as shown in Fig. 1. Tapering reduces the total line resistance, increasing the inductive behavior of the line [5]. No previous work has been published that determines the optimum wire shape to minimize the propagation delay of an RLC line. The inductive behavior of the interconnect, however, can no longer be neglected, particularly in long interconnect lines [5, 6]. Wire tapering is usually applied to long lines, further increasing the importance of including the line inductance in the optimization process.

The research described in [7] shows that wire tapering improves the speed by only 3.5% as compared to uniform wire sizing if an optimum repeater system is used to minimize the propagation delay of an RC line. Uniform wire sizing is also easier to implement if a repeater system is available. The inductance, however, has not been considered in the line model described in [7]. Furthermore, for practical reasons, a repeater system is not always possible. Moreover, repeater insertion increases the dynamic power due to the additional input gate capacitance of the repeaters.

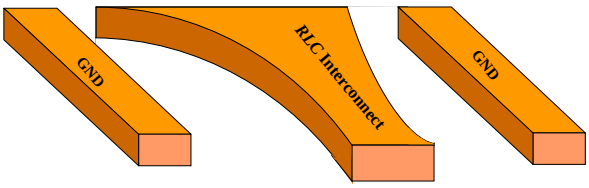

Figure 1: Coplanar tapered RLC interconnect

It is shown in this paper that exponential wire tapering is the optimum shape for an RLC interconnect. In this work it is assumed that no repeaters are inserted along the line. Wire tapering is shown to reduce the power dissipation as well as the propagation delay.

The paper is organized as follows. In section 2, the optimum wire shape that produces the minimum signal propagation delay of an RLC line is characterized. Different constraints on interconnect tapering are discussed in section 3. In section 4, a comparison between tapered RC and RLC lines is presented. Some simulation results are presented in section 5. In section 6, some conclusions are provided.

2 Optimum Wire Shape for Minimum Propagation Delay

The signal propagation delay of a distributed RLC interconnect is described in [8, 9]. Two time constants characterize the signal speed and shape in long interconnects, the resistive-capacitive (RC) time constant and the inductive-capacitive (LC) time constant (or the time of flight through the line $t_f = \sqrt{L_{int}C_{int}}$), where C_{int} and L_{int} are the line capacitance and inductance, respectively). For highly resistive (less inductive) lines, an RC delay model is adequate to characterize the signal delay.

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The optimum tapering for these lines is an exponential tapering factor [1]. If the inductive behavior of the line dominates the resistive behavior, the time-of-flight can dictate the time for the signal to propagate through the line [10]. The optimum shape that minimizes the propagation delay of a line is the shape function that minimizes the time-of-flight.

The line inductance and capacitance per unit length, respectively, can be expressed in terms of the line width by the simple relations,

$$L_{int}(W) = \frac{L_0}{W(x)}, \tag{1}$$

$$C_{int}(W) = C_0 W(x) + C_f, \tag{2}$$

where L_0 is the line inductance per square, C_f is the fringing capacitance per unit length, and C_0 is the line capacitance per unit area. $W(x)$ is the line width as a function of x, the distance from the load as shown in Fig. 2.

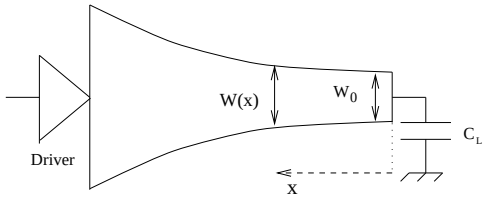

Figure 2: RLC line tapered by a general width tapering function $W(x)$

The time-of-flight for the signal is

$$t_f = \sqrt{\int_0^l \frac{L_0}{W(x)} \int_0^x (C_0 W(y) + C_f) dy dx}, \tag{3}$$

where l is the line length. If functions F and $u(x)$ are defined as

$$\begin{aligned} F &\equiv \frac{L_0}{W(x)} \int_0^x (C_0 W(y) + C_f) dy, \\ u(x) &\equiv \int_0^x W(y) dy, \end{aligned}$$

respectively, and Euler's differential equation is used to minimize (3), as similarly described in [1], the optimum $u(x)$ should satisfy the differential equation,

$$u'(x) = \frac{2L_0 C_0}{c} u(x) + \frac{2C_f L_0 l}{c}. \tag{4}$$

Thus,

$$W(x) = W_0 \, e^{\frac{2L_0 C_0}{c} x}, \tag{5}$$

where $c = \frac{2C_f L_0 l}{W_0}$. W_0 is obtained by substituting (5) into (3) and differentiating (3) with respect to W_0. Setting the result to zero produces the nonlinear equation which can be solved numerically.

As shown in (5), the optimum tapering function of the width of an LC line is an exponential function. For either an RC or LC line, the general form of the optimum shaping function that minimizes the propagation delay is an exponential function. The RC and LC models are the two limiting cases of a general RLC interconnect. The optimum tapering function of an RLC line must satisfy the general exponential form $W(x) = qe^{px}$, where q is the line width at the load end, as shown in Fig. 2, and p is the tapering factor. The optimum value of q and p for an RLC line reduces to the value given in [1] if the line inductance is negligible (an RC line) and to the value given in (5) if the line resistance is negligible (an LC line). The optimum value of q and p for an RLC line is between these two limits.

As described in [6, 11], for an RLC line, the signal propagation delay is minimum when the line is matched with the driver. The matching condition, from [11], is

$$R_{tr} = |Z_{line}(q,p)|, \tag{6}$$

which can be used to determine the optimum tapering function. $Z_{line}(q,p)$ is the lossy characteristic impedance of a line, where

$$|Z_{line}(q,p)| = \sqrt{\frac{\sqrt{R_{line}(q,p)^2 + (\omega L_{line}(q,p))^2}}{\omega C_{line}(q,p)}}, \tag{7}$$

$$\omega = \frac{2\pi}{3t_r}, \tag{8}$$

and R_{tr} is the equivalent output resistance of the driver. $R_{line}(q,p)$, $L_{line}(q,p)$, and $C_{line}(q,p)$ are the line resistance, inductance, and capacitance as functions of q and p, respectively. t_r is the signal transition time at the near end of the line which is determined from the reduced order model described in [11].

As there is one equation, (6), and two unknowns, q and p, there are two degrees of freedom in designing an optimum RLC line tapered for minimum delay. For a width q, there is an optimum tapering factor p_{opt} which satisfies (6) and at which the propagation delay is minimum. Other design constraints, such as the minimum and maximum line width and power dissipation, are discussed in section 3 to determine a power efficient solution.

3 Constraints on Optimum Tapering for RLC Lines

Tapering an interconnect assigns a small width for the line at the far end. The line width increases at the near end

as shown in Fig. 2. As discussed in section 2, the width increases exponentially to obtain the minimum propagation delay. By choosing q and solving (6) as a nonlinear equation in one unknown, the optimum tapering factor p_{opt} can be determined. There are two practical limits for choosing q,

(1) $q \geq W_{min}$, where W_{min} is the minimum wire width of a target technology.

(2) $q \leq W_{max}e^{-pl}$, where W_{max} is the maximum wire width of a target technology.

These two constraints should be satisfied while designing a tapered line. q cannot be lower than the minimum wire width allowed by the technology. Alternatively, increasing q may result in a width at the near end (the largest width of the line) which may be greater than the maximum available wire width.

Another important design constraint is power dissipation. Wire sizing affects the two primary transient power components, the dynamic power dissipated in charging and discharging the line capacitance and the short-circuit power dissipated within the load gate. The short-circuit power is minimum when the line is matched with the driver [12, 13], which is also the optimum solution for minimum delay.

The dynamic power is directly proportional to the line capacitance. To decrease the line capacitance, the line width should be as narrow as possible, as the line capacitance increases superlinearly with the width [14]. In order to satisfy both high speed and low power design objectives, q should be chosen equal to W_{min}. The optimum value for the tapering factor p_{opt} is obtained by solving (6) for $q = W_{min}$. Optimum wire tapering is compared in section 4 with uniform wire sizing for both RC and RLC lines.

4 Tapering versus Uniform Wire Sizing in RC and RLC Lines

Interconnect tapering is more efficient in RLC lines than in RC lines. Two effects reduce the signal propagation delay of an exponentially tapered RLC line. The first effect is the shape of the line structure which minimizes both the RC and LC time constants.

The second effect is an increase in the inductive behavior of the line. Tapering an interconnect line decreases the line resistance, reducing the attenuation along the line. This effect increases the inductive behavior of the line. The inductive behavior of the line can be characterized by $\zeta = \frac{R_{line}}{2}\sqrt{\frac{C_{line}}{L_{line}}}$, the damping factor of a line [5]. As described in [5], when $\zeta < 1.0$, the inductive behavior of a line cannot be ignored. As shown in Fig. 3, the damping factor decreases as the line tapering factor increases, making the line behave more inductively. For $\zeta > 1.0$ (the dotted lines), the damping factor does not consider the inductive behavior of the line since the line is underdamped. The inductive effect of a line with $\zeta > 1.0$ is negligible.

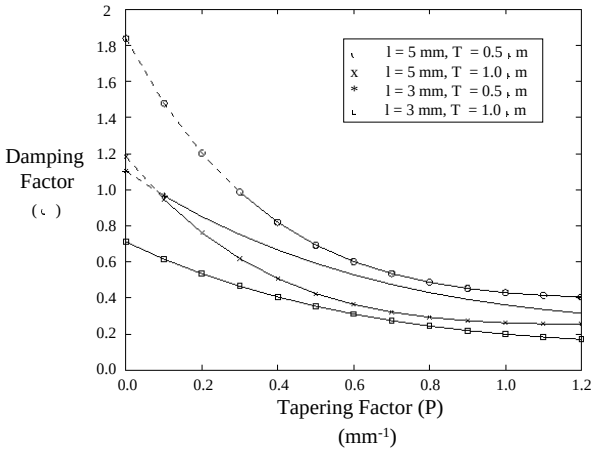

Figure 3: Interconnect damping factor as a function of the tapering factor for different line parameters

The line inductance shields part of the line capacitance and decreases the equivalent output resistance of the gate that drives the line. The signal propagation delay decreases as the inductive behavior of the line becomes more pronounced [11]. This effect makes line tapering more attractive in long RLC lines.

Another criterion to optimize the interconnect width for minimum propagation delay is uniform wire sizing. A minimum width coplanar interconnect line is illustrated in Fig. 4 for two sizing criteria.

A uniform wire size assumes a constant interconnect width along the line length. As shown in [7] for an RC line, optimum wire tapering with repeater insertion outperforms uniform wire sizing with repeater insertion by 3.5%.

Exponential wire tapering outperforms uniform wire sizing as discussed in section 2. As with wire tapering, uniform wire sizing decreases the line resistance, making the inductive behavior greater; however, the superlinear increase in the line capacitance limits the effect of the line inductance on reducing the signal propagation delay. Wire tapering, however, produces a smaller delay than the delay achieved from uniform wire sizing. Optimum wire tapering produces a greater delay reduction in RLC lines than in RC lines as the inductive behavior of the line further decreases the delay. The line inductance makes tapering more efficient than uniform wire sizing in RLC lines.

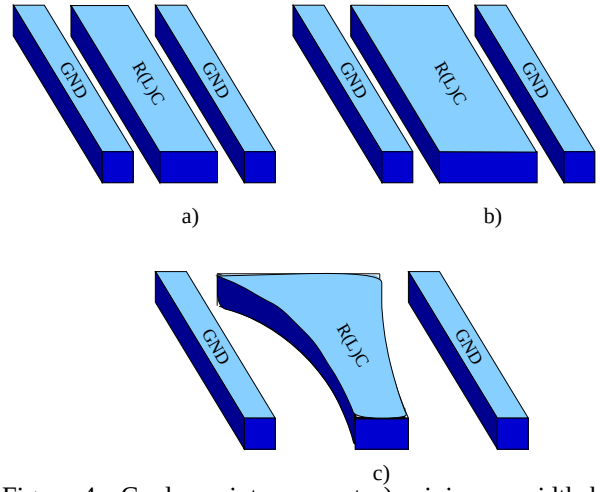

Figure 4: Coplanar interconnect a) minimum width b) uniform sizing c) exponential tapering

For an RLC line, tapering not only reduces the propagation delay, but also decreases the total power dissipation as compared to uniform wire sizing. An increase in the inductive behavior of the line reduces the signal transition time at the load, reducing the short-circuit current and, consequently, the total transient power dissipation [12, 15]. Simulation results are presented in section 5 that illustrate the efficiency of exponential wire tapering on both the propagation delay and power dissipation of RLC lines.

5 Simulation Results

In order to determine the optimum tapering factor, the line impedance parameters (R_{line}, L_{line}, and C_{line}) are expressed in terms of the design parameters q and p. Closed form expressions for the line parameters are provided in the Appendix.

A 0.24 μm CMOS technology is used to demonstrate the efficiency of tapering an RLC line. A 5 mm long interconnect line with $T = 0.5\,\mu$m, $W_{min} = 0.5\,\mu$m, $W_{max} = 20\,\mu$m, and $S_{min} = 1.0\,\mu$m is considered as an example. A long interconnect driven by a CMOS inverter is modeled by twenty RLC sections. The line is shielded by two ground lines with a $1.0\,\mu$m width. A CMOS inverter is the load.

As listed in Table 1, different circuits are considered. W_n and W_{nl} are the width of the NMOS transistor of the driving and load inverters, respectively. t_{r-In} is the transition time of the signal at the input of the driving inverter. From the discussion in section 3, q is chosen to minimize the power dissipation based on the minimum value of the line width W_{min}. The width of each section and corresponding line impedance parameters are described in the Appendix.

Table 1: Circuits parameters of example circuits

	W_n (μm)	W_{nl} (μm)	t_{r-In} (psec)	q (μm)	p (m^{-1})
Circuit1	15	5	50	0.5	550
Circuit2	20	1	50	0.5	600
Circuit3	15	15	20	1.0	400

The minimum delay is determined for both uniform wire sizing and exponential line tapering. As shown in Fig. 5, wire tapering outperforms uniform wire sizing for all of the circuits. For an RLC line, the reduction in the minimum delay is greater as compared to an RC line, making tapering more efficient in RLC lines. A 15% reduction in delay for an RLC line as compared to a reduction of 7% for an RC line is achieved when optimum tapering is used rather than uniform wire sizing.

In addition to a smaller propagation delay, the total transient power dissipation is lower. A tapered line with q equal to the minimum width reduces the total line capacitance, thereby decreasing the dynamic power (as compared to uniform wire sizing). Furthermore, the power dissipation is further decreased in an RLC line since the short-circuit power is lower. The reduction in power dissipation for several RC and RLC lines is shown in Fig. 6. A reduction in power dissipation of as much as 16% for an RLC line as compared to 11% for an RC line is achieved when optimum tapering is used rather than uniform wire sizing.

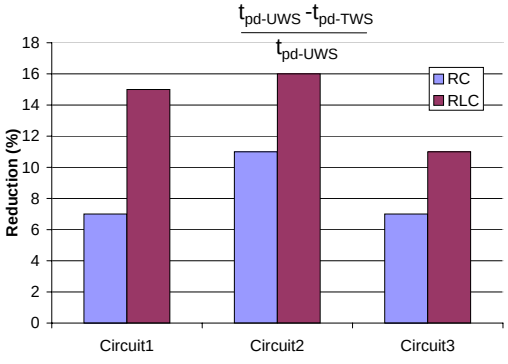

Figure 5: Reduction in propagation delay. UWS stands for Uniform Wire Sizing and TWS stands for Tapered Wire Sizing.

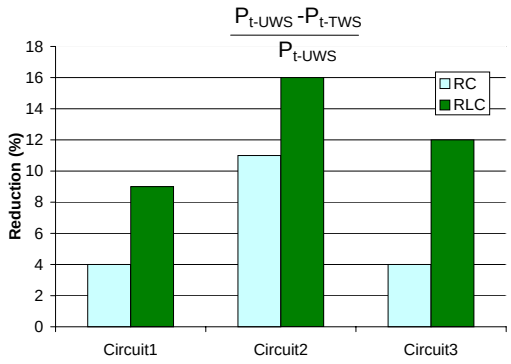

Figure 6: Reduction in total power dissipation

6 Conclusions

The optimum wire shape that produces the minimum signal propagation delay in a distributed RLC line is determined in this paper. It is shown that an exponentially tapered interconnect minimizes the time of flight of an LC line. The general form for the optimum shaping function of an RLC line is qe^{px}. The optimum wire width at the load end q and the optimum tapering factor p which achieve the minimum delay and low power are determined for the driver and load characteristics.

Optimum wire tapering as compared to uniform wire sizing is more efficient in RLC lines than in RC lines. The line inductance makes tapering more attractive in RLC lines since tapering produces a greater reduction in delay as compared to uniform wire sizing. A reduction in delay of 15% for an RLC line as compared to 7% for an RC line is achieved when optimum tapering is applied rather than uniform wire sizing.

With a minimum wire width at the far end and an optimum tapering factor, both the propagation delay and the power dissipation are reduced. The line inductance increases the savings in power in an optimally tapered line as compared to uniform wire sizing. A reduction in power dissipation of 16% for an RLC line as compared to 11% for an RC line is achieved when optimum tapering is applied rather than uniform wire sizing. Summarizing, tapering improves both the speed and power characteristics of an RLC line.

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Appendix : Impedance Parameters of Tapered RLC Interconnect

Practically, implementing a continuously shaped line is not precisely possible. However, dividing the line into sections of length $l_1 = \frac{l}{N}$, where N is the number of sections, effectively approximates a continuous shape. As shown in Fig. 7, the width of the line sections increases exponentially as the section approaches the near end, producing the optimum shape. Given the geometric dimensions of the line and shield, the line impedance parameters are expressed as functions of the tapering parameters, q and p.

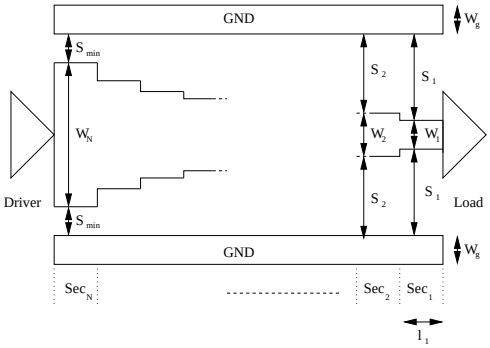

Figure 7: Coplanar tapered line

Expressing the line inductance in terms of the dimensions of the wire structure requires that the current return path be determined. In the coplanar structure shown in Fig. 7, the return path is assumed to be in the adjacent ground lines. This structure is common in global interconnects such as clock networks or data busses [16].

For a small number of line sections N, the section length is much larger than the other physical dimensions (such as the section width W_i, the separation between the section and the ground S_i, and the line thickness T). Tapering is more effective in long (global) lines (*e.g.*, $l > 1000\ \mu$m) as the line inductance and resistance are significant. These lines are divided into several sections (*e.g.*, $N < 20$), making the ratio between the section length and the other dimensions large (*e.g.*, $\frac{l_1}{W_i,S_i,T} > 100$). Neglecting skin and proximity effects and for $l_1 \gg S_i, W_i$, and T, the total line inductance is

$$L_{line}(q,p) = L_0\Big[N\left(A + \frac{3}{2}B(q,p)\right) + \frac{0.22}{l_1}\sum_{i=1}^{N}\frac{1}{W_i(q,p)} - ln\left(\prod_{i=1}^{N}(qe^{(i-1)pl_1} + T)\right)\Big], \qquad \text{(A.1)}$$

where

$$\begin{aligned} L_0 &= \frac{\mu_0 l_1}{2\pi}, \\ A &= 0.8637 - 0.5ln(W_g + T) + \frac{0.11}{(W_g + 3T)}, \\ B(q,p) &= lnSW_g(q,p) - \frac{SW_g(q,p)}{l_1}, \\ SW_g(q,p) &= 2S_{min} + W_g + qe^{(N-1)pl_1}. \end{aligned}$$

The width of each line section is

$$W_i(q,p) = \begin{cases} W_{i-1}e^{pl_1} & \text{for i} > 1\ , \\ q & \text{for i = 1}\ . \end{cases} \qquad \text{(A.2)}$$

The inductance of an exponentially tapered line is determined from (A.1) and compared with the inductance extracted by the field solver FastHenry [17]. The error between the two solutions is less than 0.78% for a tapering factor ranging from 0 to 800 m^{-1}.

The total line resistance is

$$R_{line}(q,p) = R_D l_1 \sum_{i=1}^{N} \frac{1}{W_i(q,p)}, \qquad \text{(A.3)}$$

where R_D is the line resistance per square. The total line capacitance is

$$C_{line}(q,p) = l_1 \sum_{i=1}^{N} C_{Seci}, \qquad \text{(A.4)}$$

where C_{Seci} is the capacitance of each section per unit length. A closed form expression for C_{Seci} in terms of $W_i(q,p)$ and $S_i(q,p) = S_{min} + \frac{(W_N - W_i(q,p))}{2}$ is obtained from [14].

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