Design Methodologies for On-Chip Inductive Interconnect

by

Magdy A. El-Moursy

Submitted in Partial Fulfillment
of the
Requirements for the Degree
Doctor of Philosophy

Supervised by
Professor Eby G. Friedman

Department of Electrical and Computer Engineering
School of Engineering and Applied Sciences
The College

University of Rochester
Rochester, New York

2004

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Dedication

This work is dedicated to my parents: Professor Dr. Naima A. Ahmed and Professor Dr. Ali A. El-Moursy.

Curriculum Vitae

The author was born in Cairo, Egypt in 1974. He attended the school of engineering, Department of Electronics and Communications from 1991 to 1996 where he received the B.S. degree in electronics and communications engineering (with honors) and the Master's degree in computer networks from Cairo University, Cairo, Egypt, in 1996 and 2000, respectively, and the Master's degree in electrical engineering from University of Rochester, Rochester, NY, USA, in 2002. He is a Ph.D. candidate in the area of high-performance VLSI/IC design at the University of Rochester, Rochester, NY, USA. In summer of 2003, he was with STMicroelectronics, Advanced System Technology, San Diego, CA, USA.

His research interest is in interconnect design and related circuit level issues in high performance VLSI circuits, clock distribution network design, and low power design. He is the author of about 20 papers and two book chapters in the fields of high speed and low power CMOS design techniques and high speed interconnect.

Acknowledgments

I would like to express my deep gratefulness and thanks to my supervisor Professor Eby G. Friedman who gave me a lot of his time, concern, and support both technically and socially. Without him, my research was not going to appear in this professional style and form. His advice was always giving me a light to follow the correct way. I will always remember his help and support, which made my Ph.D. study really an interesting and joyful experience which I will never forget.

My thanks to my colleagues, Dr. Volkan Krusun, Dr. Dimitrios Velenis, and Boris Andreev, with whom I enjoyed my research. Special thanks are dedicated to Dr. Andrey V. Mezhiba for the useful discussions, which helped me a lot. I would also like to thank my brother, Ali A. El-Moursy, who is a graduate student in University of Rochester. Ali shared with me all the good and bad moments in my study and life in Rochester.

I would like also to thank everyone in the Electrical and Computer Engineering Department at University of Rochester the secretary, the administration, and the professors. My special thanks to Professor David A. Albonesi, Professor Martin Margala, Professor Wendi Heinzelman, and Professor Robert C. Waag from whom I have learned a lot and Professor Sandhya Dwarkadas for serving on my proposal and defense committees.

At the end I would like to thank RuthAnn Williams for her professional help to finish all the paper work very accurately and in time. She adds nice spirit to the lab.

Abstract

With the decrease in feature size of CMOS integrated circuits, interconnect design has become an important issue in high speed, high complexity integrated circuits (IC). Different design methodologies have been proposed to improve circuit performance. Wire sizing, driver sizing, and wire shaping are common techniques to enhance circuit performance.

With increasing signal frequencies and the corresponding decrease in signal transition times, the interconnect impedance can behave inductively. Different design methodologies under an inductive environment are described in this dissertation. Including line inductance in the design process can enhance both the delay and power as well as improve the accuracy of the overall design process.

Line inductance introduces new tradeoffs in interconnect and driver sizing to decrease the circuit delay. An accurate solution for the optimum line width is described that minimizes the total transient power dissipated by a CMOS circuit. Furthermore, interconnect inductance introduces a shielding

effect which decreases the effective capacitance seen by the driver of a circuit, reducing the gate delay. Ignoring the line inductance overestimates the circuit delay, inefficiently oversizing the circuit driver. Considering line inductance in the design process also saves gate area, reducing the dynamic power dissipation.

An alternative technique to reduce the propagation delay in long interconnects is non-uniform wire sizing or wire shaping. In this dissertation, the optimum wire shape for the minimum signal propagation delay across an *RLC* line is shown to have a general exponential form. The line inductance makes exponential tapering more attractive in *RLC* lines than in *RC* lines. Wire tapering can reduce both the propagation delay and the power dissipation. This technique is used to size the interconnect lines within an H-tree clock distribution network. Exponentially tapered interconnect is shown to reduce the dynamic power dissipation while preserving the signal characteristics within clock distribution networks. Furthermore, the inductive behavior of the interconnects is reduced, decreasing the inductive noise.

On-chip inductance should be included in the design process in high frequency circuits. By including the on-chip inductance, the efficiency of different circuit design techniques such as wire sizing, driver sizing, and line tapering can be greatly enhanced.

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Chapter 1

Introduction

On-chip interconnects are now the primary bottleneck in the flow of signals through high complexity, high speed integrated circuits (ICs). Operating an IC at high frequency while dissipating low power is the primary objective for many modern circuit applications. The frequency at which ICs operate increases each year. In order to satisfy these performance objectives, the feature size of CMOS circuits is decreased for each advanced generation of technology. The reduction in feature size reduces the delay of the active devices. The effect on the delay due to the passive interconnects, however, has increased rapidly as described in the National Technology Roadmap [1].

Low power dissipation is another increasingly important design objective in current (and future) ICs. With shrinking feature size, the number of wires grows exponentially [1, 2]. The interconnect capacitance often dominates the total gate load [3]. On-chip interconnects therefore dissipate a large portion of the total power dissipation. Long interconnects that distribute clock signals and power can dissipate up to 40% to 50% of the total power of an IC [4]. Additional interconnect layers may enhance circuit speed while increasing the power dissipation. Interconnect design has, therefore, become a dominant issue in high speed ICs. Some insight into the complexity of modeling multilayer interconnects at high frequencies is presented in this chapter.

Interconnect wires can be classified into two categories, local wires and global wires. Local wires are those interconnects within logic units that connect the active devices. The delay of the local wires decreases with feature size since the distances among the devices decreases. Global wires are those interconnects that connect different logic units (*e.g.,* busses) or distribute signals across the die (*e.g.,* clock distribution networks). As shown in Fig. 1.1, the delay of local wires decreases while the delay of global wires increases with advancing technology nodes [4]. Despite the reduction in feature size, the die size has tended to increase. The die size has historically doubled every ten years, as shown in Fig. 1.2. The length of the global wires does not scale with technology, while the cross section decreases. The reduction in cross section increases the line resistance and, consequently, the delay required for a signal to propagate along a line. The increase in die size further increases the length of the global lines [6, 7] which further increases the delay. Special attention should therefore be placed on the global lines, since these lines can limit the overall speed of a circuit [6]-[15].

In order to cope with these trends in advanced technologies, different design methodologies have been developed to decrease the time required for a signal to propagate through a long line. In section 1.1, different models for on-chip interconnect are described. The increasing importance of considering line inductance in the interconnect model is discussed in section 1.2.

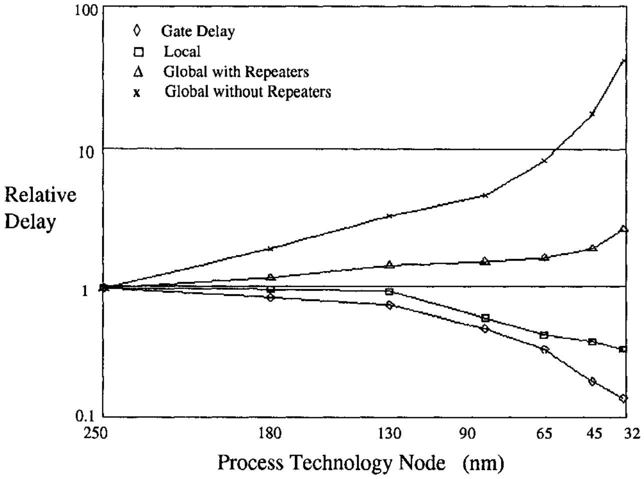


Figure 1.1: Relative delay for local and global wiring versus feature size [4]

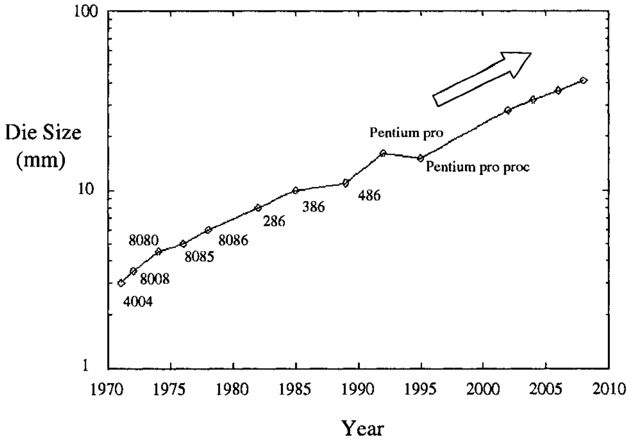


Figure 1.2: Die size for different generations of Intel microprocessors [5]

1.1 Interconnect Modeling

Modeling on-chip interconnect is important to determine the signal characteristics of a line. Accurate modeling enhances both the design and analysis processes. Local lines can often be modeled as a single lumped capacitor, as shown in Fig. 1.3a. If the line capacitance is much smaller than the load capacitance, local lines can be neglected in the delay analysis. Modeling local interconnect by a capacitive load becomes more important as the line capacitance becomes comparable to the load capacitance. Signal propagation through these lines is negligible as compared to the gate delay [16]. Since these lines are short, the resistance is typically negligible. The contribution of the line resistance to the degradation in the signal propagation characteristics is therefore not significant.

The line resistance impedes the signal propagation in long lines. The delay through these lines can be comparable to or greater than the gate delay. Modeling a global line as a lumped capacitor is often highly inaccurate. Different models have been proposed to model *RC* lines. The simplest model is a lumped *RC* model as shown in Fig. 1.3b. In order to capture the distributed nature of the line impedance, *RC* lines are often divided into sections of distributed impedances [17]-[19]. Each section is modeled as an equivalent *RC* circuit. The T and Π circuits, shown in Figs. 1.4a and 1.4b, respectively, are widely used in modeling long interconnects. The accuracy of the model depends upon the number of sections used to model the interconnect. An *RC* model is adequate at low to medium frequencies (up to a few hundred MHz). However, at high frequencies (on the order of a GHz), the *RC* model is inadequate to accurately characterize the signal. An *RLC* model is necessary to accurately characterize these interconnects.

Global lines are usually wide, exhibiting low resistance. With the reduction in line resistance and the increase in clock frequencies, the line inductance has begun to affect the signal propagation characteristics [20]. The inductance should therefore also be considered in the interconnect model. A first order approximation of an inductive interconnect is shown in Fig. 1.3c. The T and

Π equivalent distributed models for an *RLC* line are shown in Figs. 1.4c and 1.4d, respectively [21, 22].

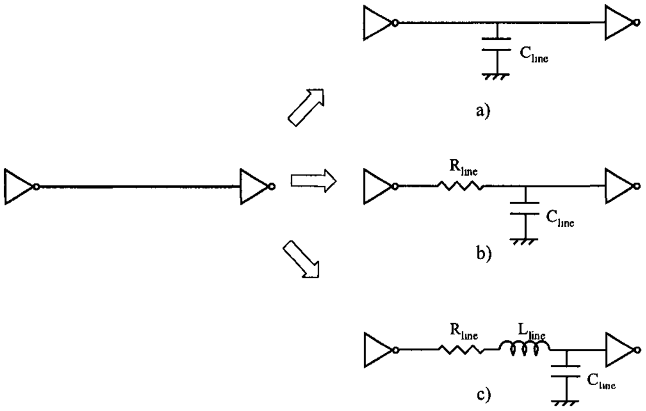


Figure 1.3: Different lumped interconnect models a) *C* model b) *RC* model c) *RLC* model

1.2 Importance of On-Chip Inductance

Many studies have been made to determine the conditions at which the line inductance should be considered in an interconnect model [23]-[25]. The work described in [20] determines the limits on the line length and transition time at which the line inductance should be considered. As the equivalent output resistance of the gate that drives the interconnect decreases, the limits presented in [20] become more accurate. The lower limit on the line length

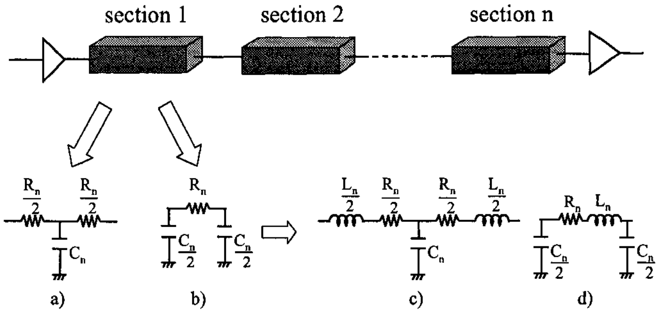


Figure 1.4: Distributed model for an interconnect a) RC T model b) RC Π model c) RLC T model d) RLC Π model

beyond which the line inductance should be considered is shown in Fig. 1.5 for different line impedance parameters (L is the inductance and C is the capacitance per unit length, respectively). Increasing signal frequencies typically require faster signal transition times. As the signal transition time decreases, the lower limit on the line length also decreases, making shorter on-chip interconnects behave inductively. Medium length lines which do not behave inductively at low frequency, behave inductively as the frequency increases.

Alternatively, the number of long interconnects has increased rapidly [26]. For example, an IC today may have only 10,000 to 20,000 global nets. This number, however, is expected to grow to more than 100,000 [27]. Considering the line inductance is, therefore, becoming more crucial in high speed, high complexity integrated circuits [28]-[40].

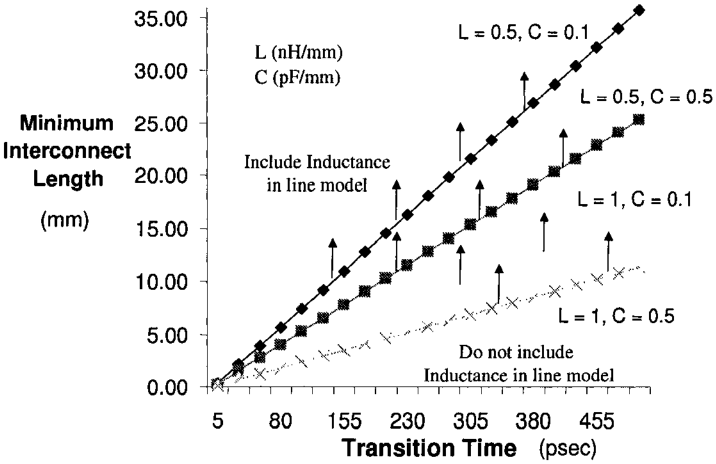


Figure 1.5: Lower limit of interconnect length above which the inductance should be considered in the line model

Another factor which increases the importance of line inductance is the introduction of new materials. New metal and dielectric materials have been introduced to reduce interconnect delay. Low-k dielectrics can decrease the line capacitance to half the capacitance of SiO_2. Furthermore, replacing aluminum lines with copper can also reduce the line resistance by a factor of two to three. These new materials increase the importance of considering the line inductance. As described in [20], the damping factor ζ can be used to characterize the significance of the inductance. For $\zeta < 1$, the line is underdamped, causing ringing in the signal. As shown in Fig. 1.6, when advanced materials are used, the damping factor decreases, increasing the importance of considering the line inductance.

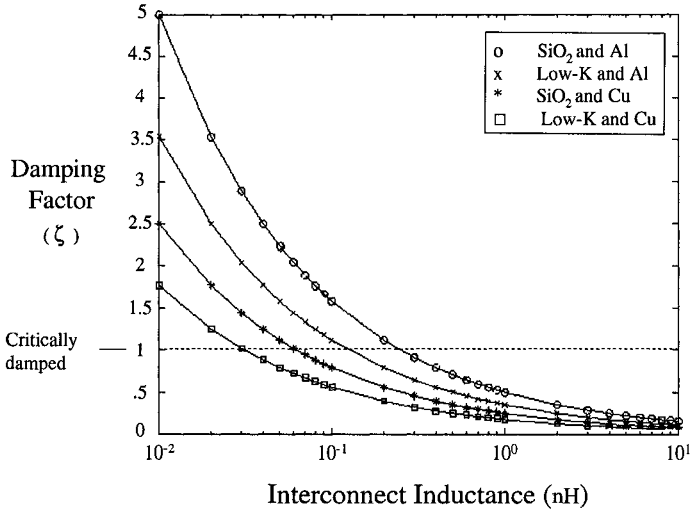


Figure 1.6: Damping factor as a function of the line inductance for different dielectric and metal materials

Different techniques to drive long interconnects are reviewed in Chapter 2. In order to drive global interconnects, many design methodologies have been proposed. Different design techniques have been developed to reduce the propagation delay along long resistive line. These techniques ignore the line inductance, which may lead to area and/or power inefficient circuits. In this chapter, efficient techniques to drive global RC interconnects are reviewed.

In Chapter 3, different aspects regarding the complexity of extracting circuit parameters at high frequencies are discussed. On-chip inductance extraction and analysis are becoming more critical at higher frequencies and smaller feature sizes. Extracting on-chip inductance in large circuits is a complicated process. An overview of inductance extraction importance and difficulties is presented in this chapter. Furthermore, the most widely used techniques to simplify the extraction process are also summarized. A comparison between the most efficient techniques is provided.

Resistive power dissipation in CMOS circuits is characterized for both RC and RLC lines in Chapter 4. Interconnect resistance dissipates a portion of the total transient power in CMOS circuits. Conduction losses increase with larger interconnect resistance. It is shown in this chapter that these losses do not add to the total power dissipation of a CMOS circuit through I^2R losses. Interconnect resistance can, however, increase the short-circuit power of both the driver and load gates. The effects of interconnect line resistance on the primary components of the transient power dissipation are described in both RC and RLC lines.

In Chapter 5, power characteristics of an inductive interconnect are described. The width of an interconnect line affects the total power consumed by a circuit. The effect of wire sizing on the power characteristics of an inductive interconnect line is presented in this chapter. The matching condition between the driver and the load affects the power consumption since the short-circuit power dissipation may decrease and the dynamic power will increase with wider lines. A tradeoff therefore exists between short-circuit and dynamic power in inductive interconnects. The power characteristics of inductive interconnects therefore may have a great influence on wire sizing optimization techniques. An analytic solution of the transition time of a signal propagating along an inductive interconnect is presented. The solution is useful in wire sizing synthesis techniques to decrease the overall power dissipation. The optimum line width that minimizes the total transient power dissipation is determined. An analytic solution for the optimum width is presented. Considering the driver size in the design process, the optimum wire and driver size that minimizes the total transient power is also determined.

For long lines, repeaters are usually used to drive the interconnect. Power and delay characteristics of a long inductive interconnect driven by a repeater system are presented in Chapter 6. Repeaters are often used to drive high impedance interconnects. These lines have become highly inductive and can affect signal behavior in long interconnects. The line inductance should therefore be considered in determining the optimum number and size of the repeaters driving a line. The optimum repeater system uses uniform repeater insertion in order to achieve the minimum propagation delay. A tradeoff exists, however, between the transient power dissipation and the minimum propagation delay in sizing long interconnects driven by the optimum repeater system. Optimizing the line width to achieve the minimum power delay product, however, can satisfy current high speed, low power design objectives. The Power-Delay-Area-Product criterion is introduced as an efficient technique to size the interconnect within a repeater system.

In Chapter 7, the shielding effect of line inductance is introduced. Interconnect inductance introduces a shielding effect which decreases the effective capacitance seen by the driver of a circuit, reducing the gate delay. A model of the effective capacitance of an *RLC* load driven by a CMOS inverter is presented. The interconnect inductance decreases the gate delay and increases the time required for the signal to propagate across an interconnect, reducing the overall delay to drive an *RLC* load. Ignoring the line inductance overestimates the circuit delay, inefficiently oversizing the circuit driver. Considering line inductance in the design process saves gate area, reducing dynamic power dissipation. An accurate model for a CMOS inverter and an *RLC* load is used to characterize the propagation delay.

The optimum interconnect shape that minimizes the signal propagation delay along *RLC* lines is determined in Chapter 8. The optimum wire shape to produce the minimum signal propagation delay across an *RLC* line is shown to have a general exponential form. The line inductance makes exponential tapering more attractive for *RLC* lines than for *RC* lines. For *RLC* lines, optimum wire tapering achieves a greater reduction in the signal propagation delay as compared to uniform wire sizing. Wire tapering can reduce both the propagation delay and power dissipation. For *RLC* lines, exponential tapering outperforms uniform repeater insertion. As technology advances, wire tapering becomes more effective than repeater insertion, since a greater reduction in the propagation delay is achieved. Wire tapering can also improve signal integrity by reducing the inductive noise of the interconnect lines. Wire tapering reduces the effect of impedance mismatch in digital circuits.

In Chapter 9, the optimum tapered structure for an *RLC* interconnect to minimize transient power dissipation of a circuit is determined. An analytic solution to determine the optimum tapered structure is provided in this chapter. Wire tapering can reduce the power dissipation of a circuit. Wire tapering is more efficient than uniform wire sizing in reducing the transient power dissipation. Optimum wire tapering can reduce the power dissipation as compared to uniform wire sizing.

In Chapter 10, a practical implementation for the optimum interconnect shaping is applied to the H-tree clock distribution networks. Exponentially tapered interconnects can reduce the dynamic power dissipation of clock distribution networks. A criterion for sizing H-tree clock networks is proposed. The technique reduces the power dissipated for an example clock network while preserving the signal transition times and propagation delays. Furthermore, the inductive behavior of the interconnects is reduced, decreasing the inductive noise. Exponentially tapered interconnects decrease the difference between the overshoots in the signal at the input of a tree. As compared to a uniform tree with the same area overhead, overshoots in the signal waveform at the source of the tree are reduced.

The dissertation is concluded in Chapter 11. In Chapter 12, other aspects which should be considered when developing design methodologies in the future are discussed.

Chapter 2

Design Methodologies to Drive RC Interconnects

2.1 Introduction

As interconnect has become a dominant issue in high speed ICs, different design methodologies have been developed to improve the performance of long interconnects. These methodologies have historically concentrated on the distributed resistance of a long line. The most effective techniques used to drive long RC interconnect are discussed in the following sections. In section 2.2, wire sizing is presented as an effective technique to increase circuit speed. Uniform repeater insertion is another effective technique as described in section 2.3. In section 2.4, optimum wire shaping for minimum signal propagation delay is discussed.

2.2 Wire Sizing

Interconnect widening decreases the interconnect resistance while increasing the capacitance. Many algorithms have been proposed to determine the optimum wire size that minimizes a target cost function. Some of these algorithms address reliability issues by reducing clock skew. Most of the previous work concentrate on minimizing delay [41]-[46]. The results described in [47]-[51] consider simultaneous driver and wire sizing based on the Elmore delay model with simple capacitance, resistance, and power models. As the inductance becomes important, specific algorithms have been enhanced that consider RLC impedance models [52]-[55].

Previous studies in wire and driver sizing have not considered changes in the signal characteristics accompanied with changes in the characteristics of the line impedance. The interconnect impedance characteristics are more sensitive to the wire size in long, inductive interconnects. The work described in [48, 51] considers power dissipation while ignoring the inductive behavior of the interconnect and, therefore, the effect of line inductance on the power characteristics. In Chapter 5, the power characteristics of an inductive interconnect are described. Changes in the matching characteristics are discussed in terms of sizing the inductive interconnect for minimum power and delay.

2.3 Repeater Insertion

Uniform repeater insertion is an effective technique for driving long interconnects. The objective of a uniform repeater insertion system is to minimize the time for a signal to propagate through a long interconnect. Based on a distributed *RC* interconnect model, a repeater insertion technique to minimize signal propagation delay is introduced in [56]. Uniform repeater insertion techniques divide the interconnect into equal sections, employing equal size repeaters to drive each section as shown in Fig. 2.1. Bakoglu and Meindl developed closed form expressions for the optimum number and size of the repeaters to achieve the minimum signal propagation delay in an *RC* interconnect [56]. A uniform repeater structure decreases the total delay as compared to a tapered buffer structure when driving long resistive interconnects while buffer tapering is more efficient for driving large capacitive loads [57]. Adler and Friedman developed a timing model of a CMOS inverter driving an *RC* load [58, 59]. The authors used this model to enhance the repeater insertion process for *RC* interconnects. Alpert considered the interconnect width as a design parameter [60]. He showed that, for *RC* lines, repeater insertion outperforms wire sizing. As shown in Chapter 6, this behavior is not the case for an *RLC* line. The minimum signal propagation delay always decreases with line width for *RLC* lines if a repeater system is used.

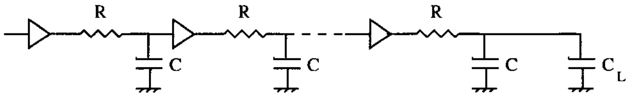


Figure 2.1: Uniform repeater system driving a distributed *RC* interconnect

The delay can be greatly affected by the line inductance, particularly for low resistance materials and fast signal transitions. Ismail and Friedman extended previous research in repeater insertion by considering the line inductance [61]. The authors showed that on-chip inductance can minimize the speed, area, and power of the repeater insertion process as compared to an *RC* line model. Banerjee and Mehrotra developed an analytic delay model and methodology for inserting repeaters into distributed *RLC* interconnect which demonstrated the importance of including line inductance as technologies advance [62]-[65].

With increasing demands for low power ICs, different strategies have been developed to minimize power in optimizing the repeater insertion process. Power dissipation and area have been considered in previous work. The line inductance, however, has yet to be considered in the optimization process of sizing a wire driven by a repeater system. Tradeoffs in repeater systems driving inductive interconnect are described in Chapter 6.

2.4 Interconnect Shaping

Another technique to reduce the signal propagation delay is to shape the interconnect line. Interconnect shaping changes the interconnect width from the driver to the load as shown in Fig. 2.2. As described in [66, 67], the optimum interconnect shape which minimizes the signal propagation delay in an *RC* interconnect is an exponential function. Different extensions to this work have been applied to consider other circuit parameters such as fringing capacitance [68]-[83].

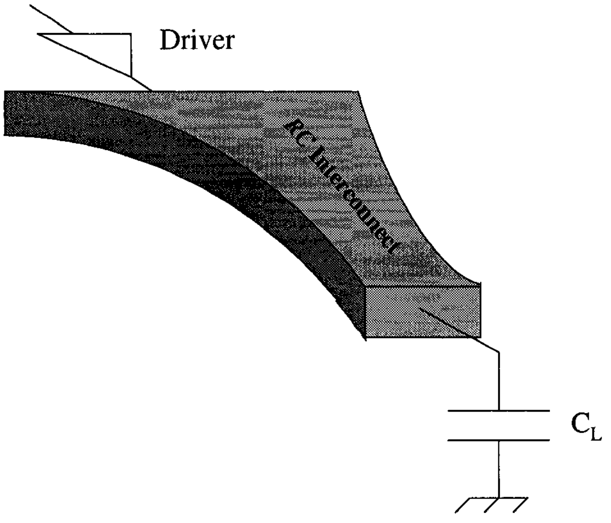


Figure 2.2: Tapered *RC* interconnect

The research described in [60] shows that wire tapering improves the speed by only 3.5% as compared to uniform wire sizing if an optimum repeater system is used to minimize the propagation delay of an *RC* line. The inductance, however, has not been considered in the line model described in [60]. The inserted repeaters increase the dynamic power due to the additional input capacitance of the repeaters. In Chapter 8, the optimum shape of an *RLC* line that minimizes the delay is determined.

Chapter 3

Inductance Extraction

3.1 Introduction

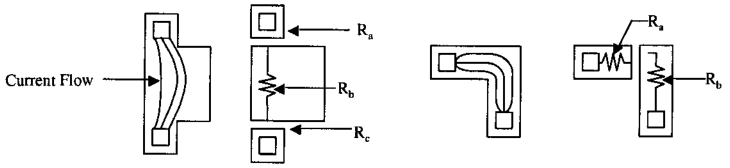
In order to consider line inductance in the design process, an accurate estimate of the line inductance needs to be determined. Determining the inductance of an interconnect surrounded by a complicated metal structure is not an easy process. Inductance extraction is the process of computing the complex frequency-dependent impedance matrix of a multi-terminal conductor, such as an electrical interconnect, under the magneto-quasistatic approximation [84].

Inductance extraction is significantly more difficult than either resistance and capacitance extraction. If skin and proximity effects are neglected, the line resistance is independent of the geometric structure of the surrounding interconnects [85]. The resistance depends only on how current flows through the interconnect line. As shown in Fig. 3.1, the interconnect capacitance is typically highly localized. The line capacitance depends on the geometric structure of the interconnect line and the adjacent lines. The electric field lines terminate at the nearest metal surface, binding the capacitive coupling to the adjacent metal structure.

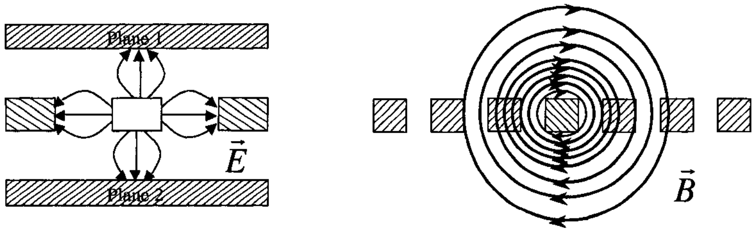
Unlike electric field lines, magnetic field lines extend to infinity, making the mutual inductive coupling with distant lines significant and potentially important in determining the line inductance. Inductance calculations require determining the current return path which is difficult in non-systematic and complicated structures [86].

At high frequencies, non-uniform current distribution flows through the interconnect cross section, causing a change in the conductor inductance due to proximity and skin effects [87]. Also, increasing circuit size requires considerable time to analyze and determine the inductance of each conductor in a circuit.

Different techniques have been developed to simplify the extraction process [88]-[113]. Most of these techniques are based on the partial element equivalent circuit (PEEC) to create an inductance matrix for a target net-



resistance extraction



capacitance extraction

inductance extraction

Figure 3.1: Example of electric and magnetic field lines to illustrate the difference among resistive, capacitive, and inductive extraction

work. This matrix is usually dense which requires sparsification to accelerate the extraction process. The most efficient sparsification approaches can be partitioned into four techniques; shell technique, hierarchical technique, halo technique, and K Matrix technique. Each of these techniques are briefly summarized in the following sections.

3.2 Shell Technique

This technique was first proposed by Krauter and Pileggi [89]. The authors assume that all of the current return paths are at a finite and constant radius r_0 from the origin as shown in Fig. 3.2. No inductive coupling is assumed outside of this radius. The inductance values of the segments within the radius are shifted to account for those entries that have been dropped as a result of truncation. This shift-truncate method can guarantee that positive definite sparse approximations of the original matrix are always produced. An extension of this technique is an ellipsoid shell, which is more suitable for conductor filament structures [90]. The primary difficulty with this technique is determining the appropriate radius r_0.

3.3 Hierarchical Technique

The hierarchical technique was first proposed by Beattie *et al.* [91]. Two auxiliary nodes are introduced to model the coupling between two groups of conductors by a single value. The new global circuit node variables represent the averaged source and potential values over an entire group of conductors

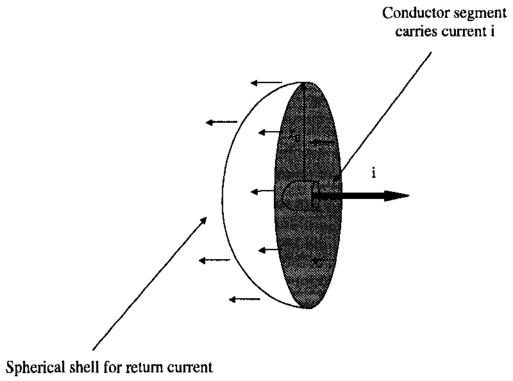

Conductor segment
carries current i
i
Spherical shell for return current

Figure 3.2: Spherical shell of return current i at a radius r_0 [89]

as shown in Fig. 3.3

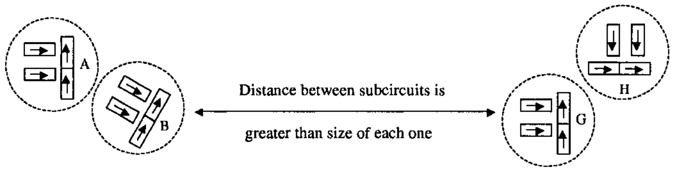

A
B
Distance between subcircuits is
greater than size of each one
G
H

Figure 3.3: Example system: A,B- aggressor groups; G,H- victim groups [91]

As an example, groups A and B are considered the aggressor groups and G and H are the victim groups. To calculate the flux induced on a specific conductor in group G, (3.1) and (3.2) are used. Without calculating the flux induced from each conductor element in A and B, the flux can be calculated in a hierarchical fashion. This approach avoids calculating the flux induced from each conductor in the system, but adds an overhead to the simulation runtime and memory.

$$\phi_{GH,A} = \sum_{i\in A} [\bigcup_{j\in GH}] * I_{Ai}, \tag{3.1}$$

$$\phi_{Gj,AB} = \phi_{Gj,AB} * [\sum_{i\in AB} L_{ji} / \sum_{i\in AB} [\bigcup_{j\in G} L_{ji}] * I_{Ai}]. \tag{3.2}$$

3.4 Halo Technique

Another approach for limiting the inductive interaction was proposed by Shepared and Tian [88]. This approach introduces return-limited inductances for sparsification and the use of "halos" to limit the number of mutual inductances. The technique separately performs inductance modeling of the signal and power/ground lines. The technique assumes a halo region surrounds the ground lines as shown in Fig. 3.4.

No mutual inductance should be considered between two conductors separated by a halo region. This approach exploits the power and ground distri-

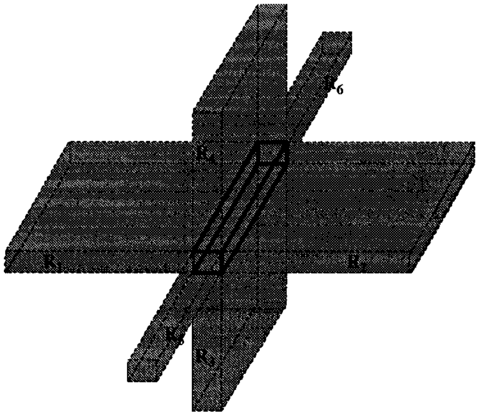


Figure 3.4: The halo of a target segment consisting of six semi-infinite regions [88]

bution networks to localize the inductive coupling.

3.5 K Matrix Technique

The authors in [92] noticed the relation between the inductance and capacitance of a transmission line represented by

$$[L_{Loop}] = \mu_0 \in_0 [C_0]^{-1}. \tag{3.3}$$

For a sparse capacitance matrix, Devgan, Ji, and Dai expected that if the inductance matrix is dense, the inverse matrix should be sparse. They proposed a new circuit matrix,

$$[K] = [L]^{-1}, \tag{3.4}$$

where K is the inverse of the partial inductance matrix. The K matrix has locality and sparsity normally associated with a capacitance matrix. A simulator called KSim has also been developed [93]. The simulator is used to directly analyze the RKC circuit rather than the RLC equivalent circuit by inserting the transient model of K into SPICE. This technique requires the partial inductance matrix to be inverted and a special simulator to analyze the circuit.

3.6 Comparison between Different Inductance Extraction Techniques

In this subsection, some observations and comments are provided that describe the strengths and weaknesses of each technique. The primary difficulty with the shell technique is determining the radius of the shell [95]. If the radius is too large, the solution may be inefficient as the inductance matrix will be quite large. Alternatively, if the radius is too small, the solution may be inaccurate because some important elements may have been neglected. The shell technique includes any inductance within a certain geometric distance from the origin whether the included inductance is significant or not. Many mutual inductances may be included which have no significant effect on the signal behavior.

The halo technique is more efficient. By assuming the current return path is in the nearest ground lines, the technique exploits the shielding effect of the power and ground traces. This technique can be highly inaccurate and strongly depends on the nature of the geometric structures. Three circuits are used to compare the two techniques. The number of nonzero elements in the inductance matrix is listed in Table 3.1.

Table 3.1: Number of nonzero elements in the inductance matrix

	Shell radius			
Circuit	50 μm	25 μm	10 μm	Halo Technique
1	3297	1297	465	132
2	3075	1427	859	178
3	6103	2513	681	597

The accuracy of the shell technique does not achieve that of the halo technique until the shell radius reaches 50 μm, which greatly increases the number of elements included in the matrix, thereby requiring larger memory and CPU time.

One of the most promising techniques is the K matrix method. Since the K matrix is sparse, no additional steps are required to determine which inductance should be considered. To compare the K matrix with the shell technique, the CPU time and memory required for both techniques are listed in Table 3.2. If the special simulator, which considers the K element rather than the L element, becomes more popular, this technique has significant potential.

Table 3.2: CPU time and memory usage for different inductance extraction methods

Method	CPU time (s)	Memory (MB)
Full L Matrix	734	20
Shell method	144	6
K matrix method	17	3

The work described in [94] is a table based inductance extraction method which considers the common structure of the N conductors in the metal layers of an IC. Techniques such as hierarchical and table based techniques are not widely used. The hierarchical technique requires significant overhead in both CPU time and memory, and is therefore unacceptable in large circuits. Table based techniques are not applicable to any structure. Only symmetric structures can be evaluated, making these approaches not generally useful.

Different design methodologies to drive long, inductive interconnect are discussed in following chapters. At high frequencies, long interconnects should be treated as lossy transmission lines. Transmission line properties affect the signal characteristics and change the nature of the circuit design methodologies. In the following chapters, different design methodologies are reevaluated assuming an inductive environment.

Chapter 4

Resistive Power in CMOS Circuits

4.1 Introduction

Power dissipation has become a primary design constraint in modern CMOS integrated circuits. Several methods have been introduced to estimate the transient power dissipation where the circuit load is modeled as a single lumped capacitor [114]-[120]. This interconnect model, however, neglects interconnect resistance and inductance. As the feature size is scaled, the effects of interconnect resistance and, more recently, inductance have increased.

Various components of power dissipation have been studied for different line models [121]-[125]. As the resistance of the interconnect has become significant, a portion of the total transient power dissipation is consumed as conduction loss within the line. The results described in [124] show that conduction losses can reach 54% of the total transient power dissipation. A closed form expression for the resistive power dissipation of a CMOS inverter driving a resistive-capacitive load is presented in [121]. Confusion, however, exists as to whether and how to consider resistive I^2R power losses within the interconnect line. Conduction losses have been incorrectly represented as an additional transient power component [121, 126]. It is shown here that this conclusion is incorrect. Conduction losses do not add to the total transient power dissipation of a CMOS circuit. Regardless of the magnitude of the line resistance, the conduction loss does not change the total transient power dissipation of a CMOS circuit. This conclusion is applicable to any interconnect line whether modeled as a resistive-capacitive line or as a lossy RLC transmission line.

The effects of interconnect line resistance on the primary components of the transient power dissipation are described in section 4.2. In section 4.3, some simulation results are provided. The chapter is concluded in section 4.4.

4.2 Effect of Interconnect Resistance on the Transient Power Dissipation

The effect of interconnect resistance on the transient power dissipation is discussed in this section. Transient power dissipation has two primary components, dynamic and short-circuit power. It is shown in subsection 4.2.1

that conduction losses within the interconnect line are already included in the dynamic power dissipation of a circuit. Furthermore, increasing the line resistance may reduce the dynamic power dissipation of the line driver under specific conditions. Greater line resistance can also increase the short-circuit power dissipation of the driver and the load gate. These topics are described in subsection 4.2.2.

4.2.1 Conduction Losses in Resistive Interconnect

To determine the process in which conduction losses are included in the transient power dissipation, the $C{V_{dd}}^2 f$ dynamic power dissipation of an inverter driving a capacitive load is first considered, where short-circuit power is neglected. In order to properly evaluate the circuit, the PMOS and NMOS transistors are replaced with an equivalent variable resistance R_p and R_n, respectively.

To charge the load, an energy e drawn from the power supply is

$$e = \int_0^{T/2} V_{dd}\, I \, dt = V_{dd}\, Q, \tag{4.1}$$

where I is the charging current and Q is the charge placed on the load capacitor, where $Q = C_{load} V_{dd}$ [127]. The energy drawn from the supply is $C_{load} {V_{dd}}^2$ and the dynamic power dissipation is $C_{load} {V_{dd}}^2 f$, where $f = 1/T$ is the switching frequency.

As the load capacitor is charged from 0 to V_{dd}, the energy stored in the capacitor is $\frac{1}{2}C_{load}{V_{dd}}^2$. From conservation of energy, the remaining half of the energy is dissipated in R_p. During the period the load is discharged, the energy stored in C_{load} is dissipated in R_n. Note that the dynamic power dissipation does not depend upon the magnitude of R_p and R_n (which are dependent upon the size of the driver transistors). Note also that the power is dissipated in the resistors, R_p and R_n.

If a line resistance is included in the interconnect model, the equivalent circuit for both switching polarities is shown in Figs. 4.1a and 4.1b. The total resistances are

$$R_{eqp} = R_p + R_{line}\,, \tag{4.2}$$

$$R_{eqn} = R_n + R_{line}\,. \tag{4.3}$$

The power supply charges the load capacitance C_{load} to the supply voltage V_{dd}. The amount of charge Q drawn from the source is

$$\text{Charge}\,(Q) = \text{Capacitance}\,(C_{load}) \bullet \text{Voltage across capacitance}\,(V_{dd}). \tag{4.4}$$

The energy drawn from the source is the same as (4.1),

$$\text{Energy}\,(e) = \text{Voltage supply}\,(V_{dd}) \cdot \text{Charge}\,(Q). \tag{4.5}$$

The capacitive-resistive line, therefore, dissipates the same dynamic power $C_{load}{V_{dd}}^2 f$ as a capacitive line.

When the voltage across the load capacitor reaches the supply voltage V_{dd}, the energy stored in the load capacitor is independent of the resistance, current, or time. The energy stored in the load capacitor is half the energy drawn from the supply and is

$$E_c = \frac{1}{2} C_{load} {V_{dd}}^2. \tag{4.6}$$

From conservation of energy, the energy dissipated in the equivalent resistance R_{eqp} is the remaining half and is

$$E_{R_{eqp}} = \frac{1}{2} C_{load} {V_{dd}}^2. \tag{4.7}$$

During the discharge phase, the charge on the capacitor is moved to ground. Regardless of the resistance, current, and time, the energy dissipated in R_{eqn} is

$$E_{R_{eqn}} = \frac{1}{2} C_{load} {V_{dd}}^2. \tag{4.8}$$

The total dynamic power dissipation is twice the energy dissipated in one of the resistances $\frac{1}{2} C_{load} {V_{dd}}^2$ per clock period, leading to

$$P_{Dynamic} = C_{load}{V_{dd}}^2 f. \tag{4.9}$$

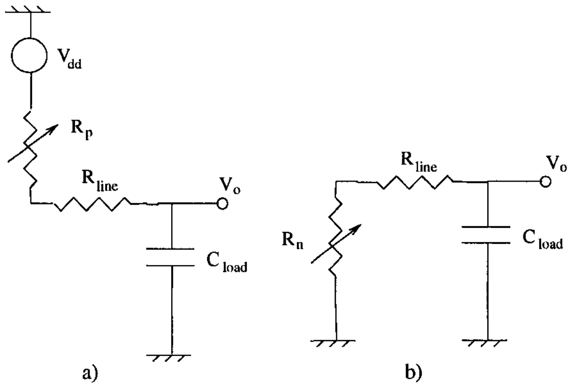


Figure 4.1: Equivalent circuit model including line resistance during a) charging, b) discharging

The conduction losses are, therefore, included in the dynamic power component and should not be considered separately [128]. In both of the capacitive and capacitive-resistive interconnect models, the power is dissipated in the resistances. In a simple capacitive interconnect model, the dynamic power is dissipated in the transistors. In a capacitive-resistive interconnect model, the dynamic power is divided between the interconnect resistance and the transistors, but the sum remains $C_{load}{V_{dd}}^2 f$.

Once the voltage across the load capacitor reaches the supply voltage, the dynamic power does not change with the line resistance. The interconnect resistance reduces the charging (discharging) currents, increasing the time required to charge (discharge) the load.

A second observation can be noted. The interconnect resistance can actually reduce the dynamic power dissipation. If the final voltage V_{final} across the load capacitor does not reach the supply voltage (*i.e.*, 90% of V_{dd}) due to the interconnect resistance, while the circuit continues to function properly, the dynamic power dissipation of the driver decreases with increasing line resistance. The energy drawn from the power supply, therefore, decreases with increasing line resistance. The difference in energy ΔE between these two cases is proportional to the difference between the square of the final voltage at the load and the supply voltage,

$$\Delta E = C_{load}\,({V_{dd}}^2 - {V_{final}}^2). \tag{4.10}$$

The energy drawn from the source is divided equally, each half is dissipated in one of the two switching resistances. Although an increase in the interconnect resistance may cause a reduction in the dynamic power dissipation, a degradation in the signal increases the sensitivity of the signal to noise. An increase in the signal transition time with greater line resistance increases the short-circuit power within the load gate as well as the signal delay along the line. Furthermore, increasing the line resistance will likely increase the short-circuit power dissipated by the driver as discussed in subsection 4.2.2.

4.2.2 Effect of Line Resistance on Short-Circuit Power within the Driver Gate

The line resistance can increase the short-circuit current within the line driver. The short-circuit power P_{sc} depends upon the period during which both of the driver transistors are simultaneously on and the value of the short-circuit current I_{sc},

$$P_{sc} = V_{dd} f \int I_{sc}\, dt. \tag{4.11}$$

The period during which both of the driver transistors are simultaneously on depends upon the input signal transition time and is independent of the load at the output of the gate. The short-circuit power changes with the load characteristics due to the change in the voltage drop across the driving transistors which changes the short-circuit current.

In Fig. 4.2, different current components are shown for an input signal transitioning from high to low. The short-circuit current is illustrated in the equivalent circuit shown in Fig. 4.2. The source current is divided into two components, the charging current $I_{charging}$ and the short-circuit current I_{sc}. For increasing line resistance, the charging (and discharging) current decreases. A more highly resistive line increases the portion of the source current that flows through the NMOS transistor to ground, thereby increasing the short-circuit current and, consequently, the short-circuit power dissipated within the driver gate. An increase in short-circuit power is due to a limited increase in the short-circuit current with higher load resistance as demonstrated in section 4.3.

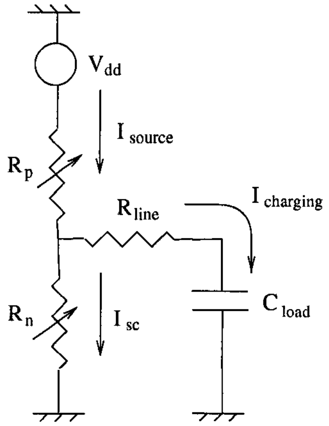


Figure 4.2: Equivalent circuit including short-circuit current for an input signal transitioning from high-to-low

The interconnect inductance of a lossy *RLC* interconnect is a lossless element, and, therefore, does not contribute to the transient power dissipation of a line. As described in [123], the dynamic power dissipated by a lossless transmission line equals the dynamic power dissipated by the total line capacitance. As described in subsection 4.2.1, the dynamic power of a lossy transmission line equals the dynamic power of a lossless line with the same line capacitance. Similar to the previous discussion, the resistance of a lossy transmission line may also increase the short-circuit power dissipation of both the driver and the load as presented in section 4.3.

4.3 Simulation Results

To verify the observations presented in section 4.2, a CMOS inverter driving either a capacitive-resistive line or a lossy transmission line has been investigated. A 0.24 μm CMOS inverter is loaded by a lumped RC impedance with an equivalent line capacitance of $C_{INT} = 50fF$, and an equivalent line resistance is varied from 0.25 Ω to 20 KΩ. The magnitude of each of the power components is determined by SPICE and listed in Table 4.1.

As the line resistance increases, the conduction loss also becomes larger but does not increase the total transient power dissipation. Any increase in the total transient power is due to an increase in the short-circuit power. For all values of load resistance the dynamic power dissipation is 15.62 μW. The ratio of the conduction loss to the total power dissipation increases from 0.02% to about 40% for an increase in load resistance from 0.25 Ω to 20 KΩ. More power is dissipated in the load resistance as compared to the power dissipated in the charging (or discharging) transistor.

Table 4.1: Power components for resistive-capacitive line

Line Resistance (Ω)	Power (μW)				Ratio of Conduction Loss to the Total (%)
	Short-circuit	Total	Dynamic	Conduction Loss	
0.25	18.66	34.28	15.62	0.0038	0.01
2.5	18.66	34.28	15.62	0.0381	0.11
25	18.76	34.38	15.62	0.3759	1.09
250	19.52	35.14	15.62	3.36	9.29
2500	21.79	37.41	15.62	12.24	32.74
20000	22.71	38.33	15.62	15.21	39.69

For a resistive-capacitive load, the short-circuit current for interconnect line resistances R_{INT} = 0.25 Ω, 250 Ω, and 20 $K\Omega$ is shown in Fig. 4.3. As shown in the figure, the short-circuit current increases as the load resistance increases. The maximum short-circuit current increases by around 33% for about a five order of magnitude increase in the line resistance. The increase in short-circuit and total power dissipation is about 21% and 12%, respectively.

The lossy transmission line is modeled by adding a lumped inductance of $10\,nH$ in series with the line resistance. The same power components are listed in Table 4.2. Since the inductance is a lossless element, the dynamic

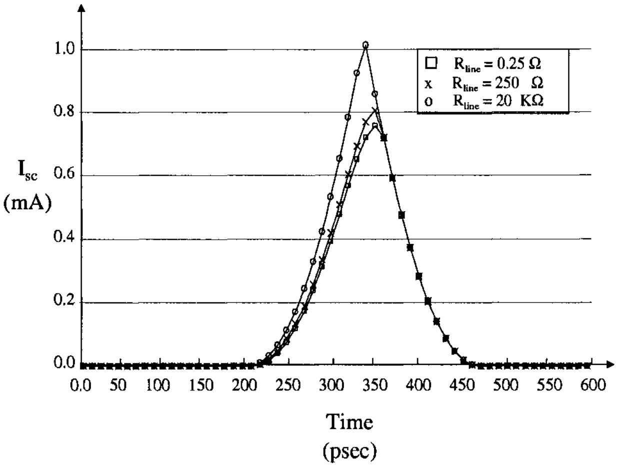


Figure 4.3: Short-circuit current waveform for different load resistances of a resistive-capacitive load

power remains the same. For a lossy transmission line, the short-circuit current for interconnect line resistances R_{INT} = 0.25 Ω, 250 Ω, and 20 $K\Omega$ is shown in Fig. 4.4. The load resistance has the same effect on the short-circuit current and, consequently, on the short-circuit power. Note from the data listed in Table 4.2 that the addition of a resistance in the lossy transmission line also does not change the total transient power other than producing a small increase in short-circuit power.

Table 4.2: Power components for lossy transmission line

Line Resistance (Ω)	Power (μW)				Ratio of Conduction Loss to the Total (%)
	Short-circuit	Total	Dynamic	Conduction Loss	
0.25	19.57	35.19	15.62	0.0067	0.02
2.5	19.55	35.17	15.62	0.0649	0.18
25	19.62	35.24	15.62	0.6016	1.71
250	20.17	35.79	15.62	4.08	11.41
2500	21.89	37.51	15.62	12.48	33.29
20000	22.71	38.33	15.62	15.22	39.71

4.4 Conclusions

The effects of interconnect line resistance on the total transient power dissipation of CMOS circuits are discussed in this chapter. As the line resistance is increased, the conduction loss becomes a larger portion of the total transient power dissipation. The conduction loss of an interconnect line should, therefore, not be considered separately in estimating the total transient power dissipation. Conduction losses are *included as part of the dynamic power dissipation.* The magnitude of the dynamic power dissipation of a circuit is

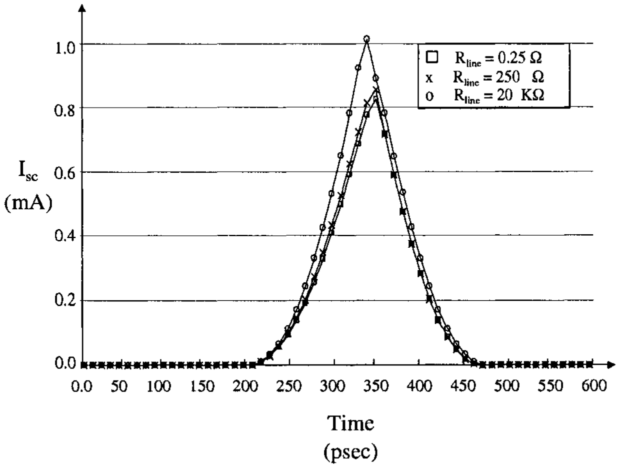


Figure 4.4: Short-circuit current waveform for different load resistances of a lossy transmission line

independent of the resistance of the interconnect line. A small increase in the short-circuit power dissipation within the driver gate occurs with a several orders of magnitude increase in the interconnect resistance. The increase in short-circuit and total power dissipation, for a five times magnitude increase in the load resistance, is about 21% and 12%, respectively. The line resistance has the same effect on the conduction loss of an interconnect line whether the line is modeled as a resistive-capacitive line or as a lossy transmission line.

Chapter 5

Wire Sizing for Inductive Interconnects

5.1 Introduction

With the decrease in feature size of CMOS integrated circuits, interconnect design has become an important issue in high speed, high complexity integrated circuits (IC). With increasing signal frequencies and the corresponding decrease in signal transition times, the interconnect impedance can behave inductively [20], increasing the on-chip noise. Furthermore, considering inductance within the design process increases the computational complexity of IC synthesis and analysis tools. However, inductive behavior can also be exploited. As shown in [129], a properly designed inductive line can reduce the total power dissipation of high speed clock distribution networks. Furthermore, on-chip inductance may affect certain design techniques such as repeater insertion [61, 130]. Clock distribution networks can dissipate a large portion of the total power dissipated within a synchronous IC, ranging from 25% to as high as 70% [131]-[133]. The technique proposed here can be used to reduce the overall power being dissipated by long nets such as a high speed clock distribution network.

On-chip interconnect now dominates the circuit delay and power dissipation characteristics of high performance ICs. Interconnect design has, therefore, become an important issue in the IC design process. Many algorithms have been proposed to determine the optimum wire size that minimizes a target cost function. Some of these algorithms address reliability issues by reducing clock skew. Most of the previous work concentrate on minimizing delay [41]-[47]. Simultaneous driver and wire sizing is presented in [47]-[51] as an efficient technique to design an optimum interconnect network with minimum propagation delay.

The work described in [48, 51] considers power dissipation as a cost function in the delay optimization process. The power minimization criterion used in these previous techniques [48, 51] minimizes the interconnect and gate area in order to reduce the capacitance of both the passive interconnects and active gates, thereby reducing dynamic power. The dynamic power dissipated in the load capacitance represents a large portion of the total transient power dissipated in a digital circuit. As shown in [129], however, the short-circuit power of some digital circuits may exceed the dynamic power. As described in [129], on-chip inductance can improve circuit speed while reducing the short-circuit power dissipation. Wire sizing can increase the inductive behavior of the signal, possibly lowering the total power dissipated by a circuit. The interconnect inductance should, therefore, be included in the power minimization process.

Buffers and repeaters are widely used in interconnect networks (*e.g.,* clock distribution networks) for different design objectives (*e.g.,* reducing delay or clock skew). Wider wires are used in [129] to reduce power dissipation while neglecting the effect of the line driver on the signal characteristics. It is shown in this chapter that this technique may, in certain cases, actually increase power dissipation. The width of the interconnect also affects other impedance parameters which can change the signal characteristics, leading to non-optimal circuits.

As interconnect inductance becomes important, specific wire sizing optimization algorithms have been enhanced that consider RLC impedance models [52]-[55]. Previous studies in wire and driver sizing do not consider changes in the signal characteristics accompanied with a change in the line impedance characteristics. The interconnect impedance characteristics are more sensitive to wire size in long, inductive interconnects. The research described in [53] considers line inductance, however, the optimization criteria minimize delay using an unrealistic inductance model and do not consider power dissipation. The work described in [134]-[136] considers dynamic power dissipation while ignoring the short-circuit power of the load gate. The work described in [48, 51] considers power dissipation while ignoring the inductive behavior of the interconnect and, therefore, the effect of line inductance on the power characteristics.

In this chapter, the power characteristics of an inductive interconnect are presented. No repeaters are assumed along the line. Repeaters can be used to reduce the signal propagation delay. Inserting repeaters, however, is not always practical. Furthermore, repeaters dissipate power and increase the area of the circuit. The power characteristics of a long, inductive interconnect driven by a repeater system are described in [137]-[139]. In this chapter, the effect of sizing an inductive interconnect on the signal characteristics is described. It is shown that the signal characteristics of an inductive interconnect line are sensitive to changes in the line width. As the short-circuit power depends directly on the signal transition time, the effect of sizing an inductive interconnect line on the signal transition time is discussed.

An analytic solution for the transition time at the far end of a long inductive interconnect is provided. These results are used to determine an analytic solution for the width of an inductive interconnect line that minimizes the total transient power dissipation. A tradeoff between short-circuit and dynamic power in inductive interconnect is introduced.

The line driver has a significant effect on the signal and power dissipation characteristics. It is shown in this chapter that simultaneous sizing of the driver and the line is important to minimize the total power dissipation. An analytic solution for the simultaneous driver and wire sizing problem that minimizes the total transient power dissipation assuming an RLC line is presented. The chapter is organized as follows. In section 5.2, the transient power characteristics of an inductive interconnect line are discussed and a power optimization criterion is formulated. The signal behavior at the far end of an inductive line is described in section 5.3. The effect of line material and length on the signal characteristics of an inductive line is discussed in section 5.4. In section 5.5, circuit simulations are used to demonstrate the accuracy of the analytic solutions for the transition time and the optimum line width. Additional results are provided that compare the power of an optimally sized line for different interconnect materials and lengths. Some conclusions are discussed in section 5.6.

5.2 Transient Power Characterization

The transient power characteristics of inductive interconnect are discussed in this section. The research described in [129] uses the concept of wire sizing to reduce the total transient power dissipated by a clock distribution network, but does not provide an analytic solution to determine the optimum interconnect width. The change in circuit behavior that occurs when the width of the line is increased is also ignored in [129]. The matching response between the line and the driver plays an important role in the transient power dissipation as discussed in section 5.3. In [129], the driver size is also not considered as a design variable.

Issues that affect wire sizing are discussed in this section. The effects of wire sizing on the line impedance characteristics are discussed in subsection 5.2.1. In subsection 5.2.2, the tradeoff between dynamic and short-circuit power dissipation in inductive interconnect is described. Transient power optimization criteria are presented in subsection 5.2.3.

5.2.1 Effect of Wire Sizing on Interconnect Line Impedance Characteristics

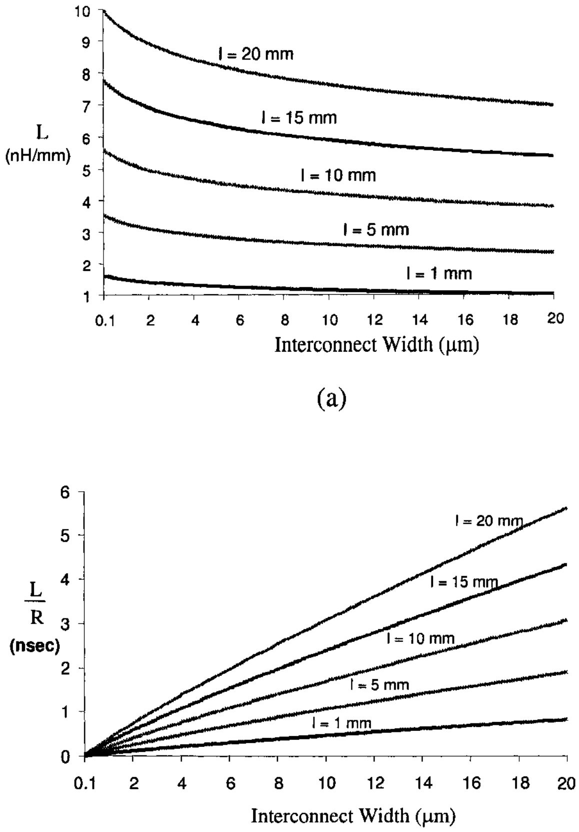
Neglecting the dielectric losses of the line, a lossy transmission line can be represented by the line resistance R, inductance L, and capacitance C, all per unit length. R is expressed in terms of the line dimensions,

$$R = \frac{\rho}{W_{INT} T}, \tag{5.1}$$

where ρ, T, and W_{INT} are the line resistivity, thickness, and width, respectively. C is expressed in terms of the line dimensions for different line structures in [140]. Note that C increases with the line width, which increases the dynamic power P_{1d}.

An expression for the line inductance requires information characterizing the current return paths. For an interconnect shielded by two ground lines, a closed form expression for the line inductance in terms of the line dimensions and the separation between the line and the ground lines is obtained from [103]. This shielded structure is commonly used in high speed clock distribution networks [100, 141] and many global interconnects. For a fixed separation between the signal and shield line, the total line inductance primarily depends on the self-inductance of the line. The line self-inductance decreases monotonically with increasing line width. The line inductance decreases with increasing line width, as shown in Fig. 5.1a.

The ratio L/R characterizes the significance of the line inductance [61]. For different line lengths, this ratio increases with wider lines as shown in Fig. 5.1b. The reduction in line resistance is greater than the reduction in line inductance. An increase in the ratio L/R and the interconnect capacitance



(a)

(b)

Figure 5.1: Inductive interconnect characteristics versus width for different lengths (a) self-inductance, (b) inductive time constant

affects the transition time as described in section 5.3.

Not only the line dimensions but also the switching frequency increase the importance of considering the line inductance. A higher clock frequency typically implies shorter signal transition times. Shorter transition times increase the number of on-chip interconnects that behave inductively. As shown in [20], for line lengths $l > \frac{t_r}{\sqrt{LC}}$ where t_r is the signal transition time, the inductance of the line should be considered in the interconnect model.

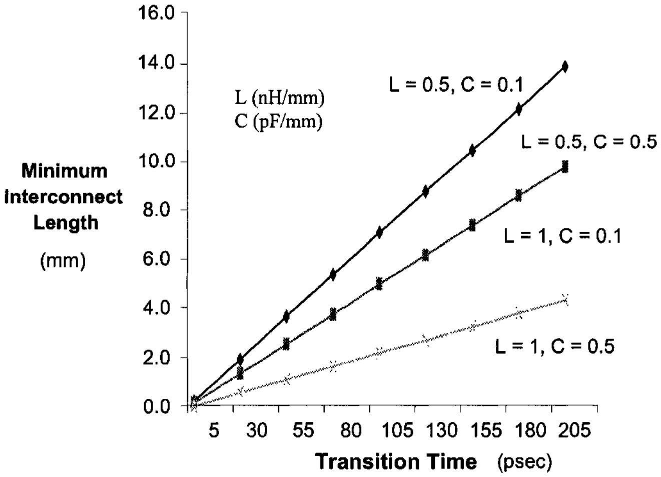


Figure 5.2: Lower limit on the interconnect length above which the line inductance should be considered

The limit on the interconnect length that produces inductive behavior is shown in Fig. 5.2. If the interconnect is longer than this limit, the line inductance should be considered in the line model [20]. For shorter signal transition times, the limit decreases for any value of line capacitance and inductance per unit length (as shown in Fig. 5.2). This characteristic increases the number of interconnect lines which behave inductively and increases the importance of line inductance to accurately characterize the signal behavior.

5.2.2 Transient Power of Inductive Lines

The power dissipation is affected by a change in line width as described in this subsection. A tradeoff exists between dynamic and short-circuit power in sizing inductive interconnect. The dependence of the power dissipation on the interconnect width is illustrated in Fig. 5.3 [142]-[146]. As the line inductance-to-resistance ratio increases, the short-circuit power decreases with wider interconnect. If the interconnect exceeds a certain width, the short-circuit power increases. The dynamic power increases with line width as the line capacitance increases. As shown in Fig. 5.3, an optimum interconnect width at which the total transient power is a minimum exists for overdriven lines. This tradeoff does not occur if the line is underdriven, as described in section 5.3.

For the circuit shown in Fig. 5.4, a long interconnect line between two CMOS inverters can be modeled as a lossy transmission line. A change in the line width primarily affects the dynamic power P_{1d} of Inv_1, and the short-circuit power P_{2sc} of Inv_2. The dynamic power of Inv_2 depends on the load capacitance, and is not affected by the wire size. The change in the short-circuit power of Inv_1 is negligible, assuming a fixed signal transition time

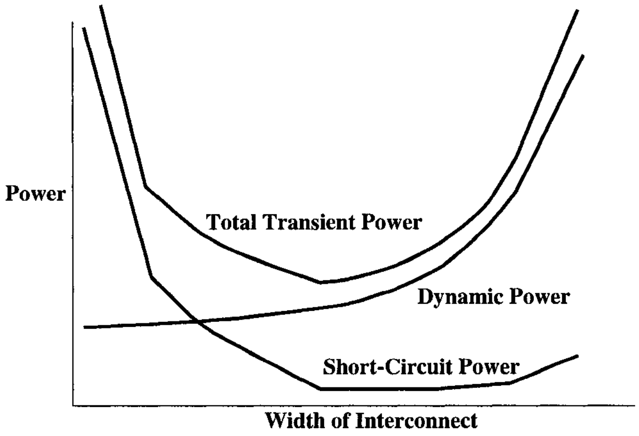


Figure 5.3: Dynamic, short-circuit, and total transient power as a function of the interconnect line width

at the input of Inv_1. For a large driver driving a long line (large capacitive load), the short-circuit power of the driver is only about 2% of the total power dissipation of the driver. For a change in the line width from 0.1 μm to 20 μm, the dynamic power of the driver increases by 400%, while the reduction in short-circuit power is less than 10%.

P_{1d} can be described as $P_{1d} = f\, V_{dd}^2\, C_1$, where f is the operating frequency, C_1 is the total capacitance driven by Inv_1, and V_{dd} is the supply voltage. The dynamic power dissipated by a lossy transmission line equals the dynamic power dissipated by the total capacitance of the line [128]. The short-circuit power dissipated within the load gate P_{2sc} is directly proportional to the input signal transition time, which is the signal transition time at the far end of an interconnect line. Regardless of the load characteristics, P_{2sc} can be represented as

$$P_{2sc} = G(V_{dd}, V_t, K, C_L)\ \tau_0\ f, \tag{5.2}$$

where τ_0 is the transition time of the input signal at the load gate, and $G(V_{dd}, V_t, K, C_L)$ is a function of V_{dd}, threshold voltage V_t, transconductance K of the load gate, and capacitive load C_L. Different techniques have been developed to characterize G under different load models. The general form of (5.2) is valid whether the load is modeled as a capacitive load [120], a lossless transmission line [123], or a lossy transmission line [125]. G is also a function of τ_0; however, the dependence of G on τ_0 is small.

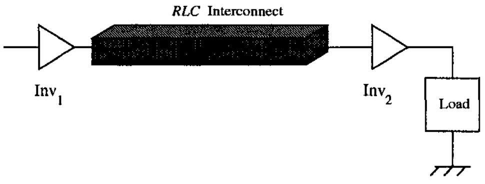


Figure 5.4: CMOS gates connected by an *RLC* interconnect line

Only C_1 and τ_0 are affected by a change in the line width. Changing the line width has a significant effect on the transition time as described in section 5.3.

5.2.3 Transient Power Optimization Criteria

Criteria for optimizing the interconnect width to minimize the transient power dissipation is presented in this subsection. The tradeoff between the primary transient power dissipation components (short-circuit and dynamic) suggests an optimum line width at which the total transient power dissipation is minimum.

Previous research in wire sizing has not considered the change in short-circuit power with a change in the line width. The short-circuit power has not been considered as a part of the optimization process. A change in the line impedance characteristics affects the power dissipation of the circuit (specifically, the short-circuit power). Ignoring the interconnect matching characteristics between the driver and load may therefore lead to a non-optimal solution (dissipating excessive power).

The effective output impedance of the driver also plays an important role in the matching response and total transient power dissipation. Two complementary effects occur. As the driver size increases, the transition time of the output signal decreases and, consequently, the short-circuit power dissipated by the load gate decreases. Simultaneously, the input capacitance of the driver gate increases since a larger inverter is used to drive the load, increasing the power required to charge the gate capacitance. The total transient power can be expressed in terms of two design parameters, the interconnect width and the driver size.

For an inverter driving N gates, as shown in Fig. 5.5, the total transient power dissipation $P_{tdrive}(W_{INT}, W_n)$ is a function of the line width W_{INT} and the NMOS transistor width W_n which represents the driver size (assuming a symmetric CMOS inverter as the driver),

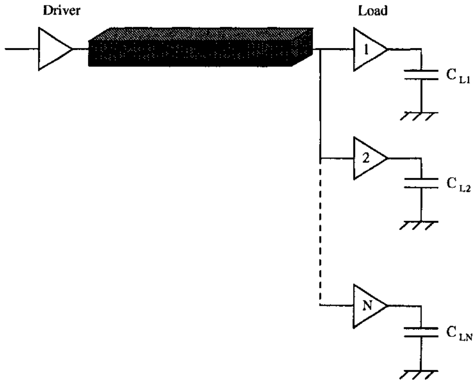


Figure 5.5: Inverter driving N logic gates

$$P_{tdrive}(W_{INT}, W_n) = P_{1d}(W_{INT}) + N\, P_{2sc}(W_{INT}, W_n) + P_{driver}(W_n), \quad (5.3)$$

where $P_{driver}(W_n)$ is the dynamic power required to charge the gate capacitance of the driver.

$$P_{driver}(W_n) = f\, V_{dd}{}^2\, C_{driver} W_n, \tag{5.4}$$

$$C_{driver} = \alpha(1 + \frac{\mu_n}{\mu_p}) L_n C_{ox}, \tag{5.5}$$

where $\frac{\mu_n}{\mu_p}$ is the electron to hole mobility ratio, L_n is the feature size, C_{ox} is the gate oxide capacitance per unit area, and α is a constant characterizing the effective gate capacitance during different regions of operation.

The dynamic power of the driving inverter $P_{1d}(W_{INT})$ is a function of the interconnect width.

$$P_{1d}(W_{INT}) = f\, V_{dd}{}^2\, C_1(W_{INT}), \tag{5.6}$$

where

$$C_1(W_{INT}) = NC_{2g} + C_{INT}(W_{INT}), \tag{5.7}$$

C_{2g} is the gate capacitance of the load inverter, and $C_{INT}(W_{INT})$ is the total interconnect capacitance which is a function of the interconnect width.

To achieve the global minimum for the transient power dissipation, the wire and driver size are simultaneously determined. Differentiating (9.1) with respect to W_{INT} and W_n and equating each expression to zero, two nonlinear equations in W_{INT} and W_n are obtained,

$$\frac{\partial P_{tdrive}}{\partial W_{INT}} = fV_{dd}^2 \frac{\partial C_{INT}}{\partial W_{INT}} + \frac{NfG}{0.8}\left(\frac{\partial t_{10\%}}{\partial W_{INT}} - \frac{\partial t_{90\%}}{\partial W_{INT}}\right) = 0, \tag{5.8}$$

$$\frac{\partial P_{tdrive}}{\partial W_n} = \frac{NfG}{0.8}\left(\frac{\partial t_{10\%}}{\partial W_n} - \frac{\partial t_{90\%}}{\partial W_n}\right) + \alpha(1 + \frac{\mu_n}{\mu_p})L_n C_{ox} = 0, \tag{5.9}$$

where $\frac{\partial t_{10\%}}{\partial W_{INT}}$, $\frac{\partial t_{90\%}}{\partial W_{INT}}$, $\frac{\partial t_{10\%}}{\partial W_n}$, and $\frac{\partial t_{90\%}}{\partial W_n}$ are described in Appendix A and $\frac{\partial C_{INT}}{\partial W_{INT}}$ is obtained from [140].

Numerical techniques are used to solve these two expressions. The two equations are solved simultaneously to determine the optimum solution. Using specific technology parameters, an analytic solution is compared to simulation results in subsection 5.5.2. In section 5.3, a change in the interconnect impedance characteristics, which directly affects the short-circuit power, is described.

5.3 Transition Time for a Signal at the Far End of an *RLC* Interconnect Line

From subsection 5.2.2, the short-circuit power is linearly dependent upon the input signal transition time. The effect of the wire size on the line impedance matching characteristics and the transition time is described in this section.

Wire sizing techniques to date have not considered the line matching characteristics as the line width changes. For inductive interconnect, the matching response plays an important role in the signal characteristics. It is shown in this section that, for an underdriven line, the transition time increases as the line becomes wider. An analytic solution of the signal transition time at the far end of an interconnect line is presented in subsection 5.3.1. The effect of wire sizing on the line matching characteristics and transition time is described in subsection 5.3.2.

5.3.1 Analytic Solution for the Transition Time

An analytic solution for the signal transition time at the far end of an inductive interconnect line is presented. The signal is assumed in this solution to behave as a ramp signal as the signal transitions from high-to-low. After the PMOS transistor of the driving inverter turns off, an expression for the signal at the far end of the line is

$$V(t) = V_c(\tau_{pOFF})\, e^{-\alpha_n (t-\tau_{pOFF})}, \tag{5.10}$$

where τ_{pOFF} is the time at which the PMOS transistor of the driver turns off, and α_n is a constant that depends upon R, C, L, and the transistor characteristics of the driver such as the transconductance, mobility, and threshold voltage. $V_c(\tau_{pOFF})$ is the voltage across the load capacitance at τ_{pOFF}. A derivation of this relation is presented in Appendix A. The transition time is expressed by $\tau_0 = \frac{t_{10\%} - t_{90\%}}{0.8}$, where $t_{10\%}$ and $t_{90\%}$ are the times at which the signal reaches 10% and 90% of the final value, respectively.

The transition time based on this analytic solution is shown in Fig. 5.6. The change in the matching condition between the driver and the load which leads to this shape is described in subsection 5.4. As the line width increases, the signal transition time decreases until a minimum transition time is reached. The signal transition time increases after exceeding a certain line width. The transition time based on this analytic solution is compared to SPICE in subsection 5.5.1.

5.3.2 Dependence of Line Characteristics on Interconnect Width

Increasing the inductance-to-resistance ratio of the line by widening the line changes the matching characteristics. For line widths at which the line inductance dominates the line resistance, the matching condition plays an important role in the signal characteristics. For an inductive environment, the matching condition between the driver and the load affects both the power

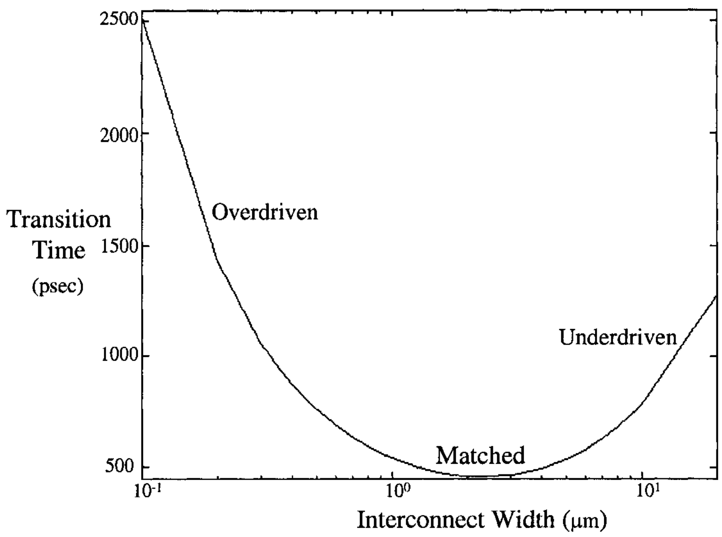


Figure 5.6: Transition time as a function of interconnect width for different impedance matching conditions. Note the minimum transition time at the ideally matched condition.

and speed characteristics as shown in section 5.5.

To better understand the signal behavior in terms of the interconnect width, an equivalent circuit of an inverter driving an inductive interconnect line is shown in Fig. 5.7a. The characteristic impedance of a lossy line can be described by the well known formula, $Z_{lossy} = \sqrt{\frac{R+jwL}{jwC}}$. Different approximations have been made to estimate Z_{lossy} in terms of the per unit length parameters [147]-[149]. A general form of Z_{lossy} is $Z_0 + g\,R$ where g is a constant which depends on the line parameters. At the end of the high-to-low

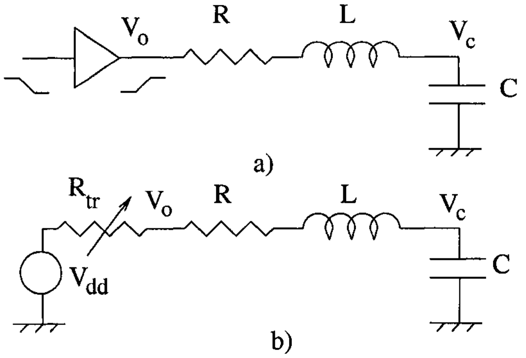


Figure 5.7: An inverter driving an RLC interconnect line (a) circuit diagram (b) equivalent circuit of inverter at the end of the high-to-low input transition

input transition, the NMOS transistor is off. With the input low, the inverter can be modeled as an ideal voltage source with a variable output resistance R_{tr} as shown in Fig. 5.7b.

At small interconnect widths, the characteristic line impedance is large as compared to the equivalent output resistance of the transistor. Thus, the line is overdriven (the underdamped condition). Z_{lossy} decreases with increasing line width. The line remains underdamped until Z_{lossy} equals R_{tr}. A further increase in the line width underdrives the line as Z_{lossy} becomes less than R_{tr} [150]. As the line width is increased, the line driving condition changes from overdriven to matched to underdriven.

Increasing the line width makes an overdriven line behave more induc-

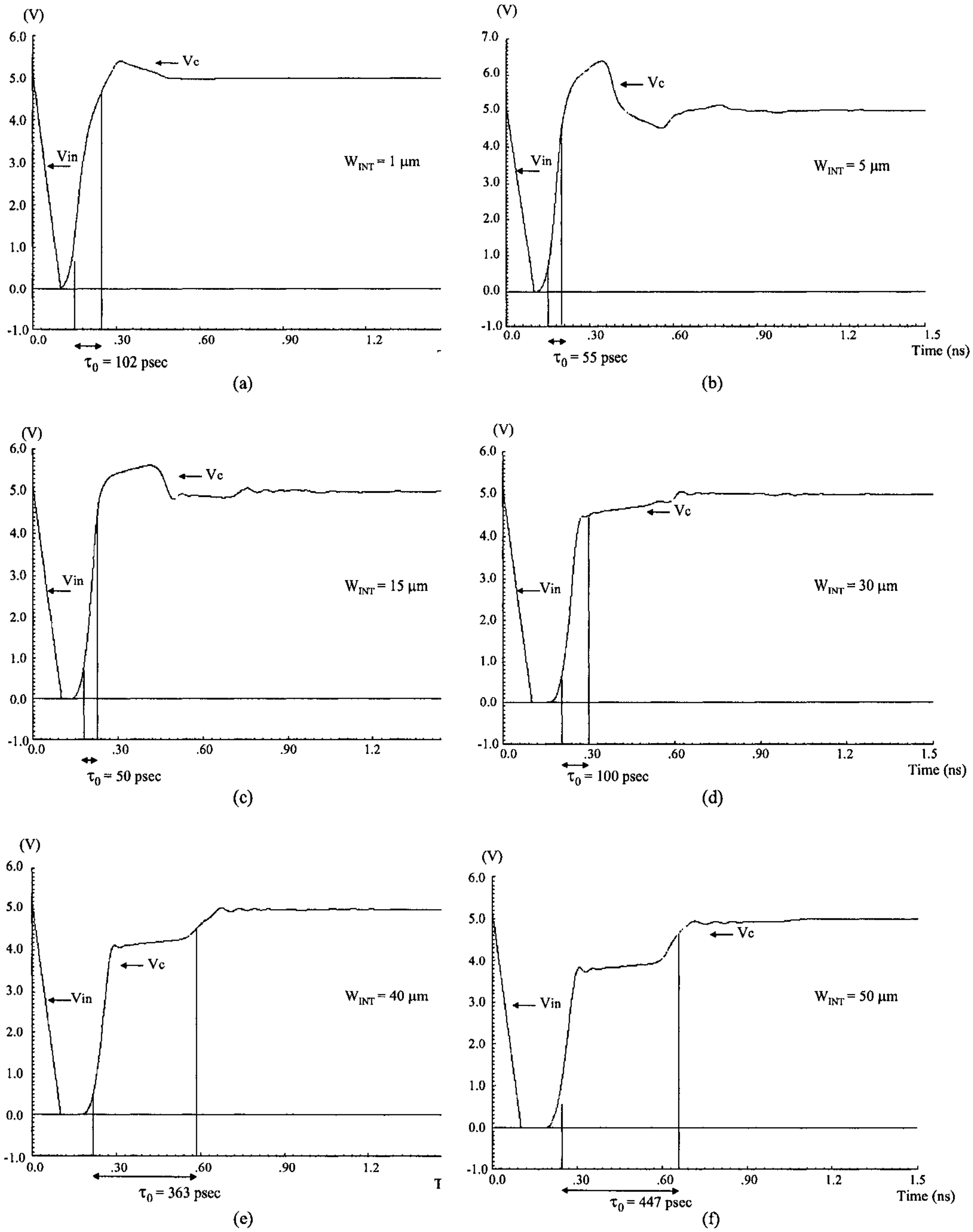


Figure 5.8: Output waveform at the far end of a long interconnect line driven by an inverter with different line widths (a) Resistive, (b) Overdriven (inductive), (c) Matched, (d) Underdriven (inductive), (e) Underdriven, (f) Underdriven

tively. The resistance decreases linearly with a linear increase in width while the inductance decreases sublinearly [103]. As described in [129], the line approaches a lossless condition, where the attenuation constant approaches zero at large line widths. This effect further reduces the signal transition time. As the line width increases, Z_{lossy} decreases until the line impedance matches the driver impedance. At this width, the transition time is minimum as shown in Fig. 5.6. A further increase in the width underdrives the line. At these widths, the capacitance begins to dominate the line impedance. With wider lines, the line becomes highly capacitive which increases the transition time, thereby increasing the short-circuit power dissipated in the load gate. For an overdriven line, the short-circuit power dissipation changes with line width as shown in Fig. 5.3. For an underdriven line, however, an increase in the line width increases the short-circuit power. If the line is underdriven, the line should be as thin as possible to minimize the total transient power by decreasing both the dynamic and the short-circuit power.

A CMOS inverter driving a capacitive load of 250 fF through a 5 mm long interconnect line is chosen to demonstrate the signal behavior. Twenty RLC distributed impedance elements are used to model the interconnect line. The input signal V_{in} is a ramp signal with a 100 psec transition time. The signal V_c across the load capacitance is illustrated by the waveforms depicted in Fig. 5.8. In Fig. 5.8a, the line is thin. The line inductance does not affect the signal waveform as the resistance dominates. As the line width increases, overshoots and undershoots appear in the waveform. As shown in Fig. 5.8b, the line inductance affects the signal characteristics and the signal transition time decreases (the overdriven condition). A further increase in the width matches the load with the driver and the overshoots disappear (see Fig. 5.8c). The signal transition time is minimum at this condition. As the wire is widened, some steps start to appear in the waveform (the underdriven condition) and the transition time increases (see Figs. 5.8d to 5.8f).

5.4 Signal Transition Time Characteristics

In this section, the signal characteristics at the far end of an inductive interconnect line for different line parameters are presented. The line parameters have an effect on the characteristics of the signal propagating along the line. Different interconnect lines with different line lengths and materials are discussed. The sensitivity of the signal characteristics to changes in the line width varies for different line lengths as described in subsection 5.4.1. In subsection 5.4.2, the effect of different line materials (and, therefore, resistivities) on the signal behavior is reviewed.

5.4.1 Effect of Interconnect Length

As the interconnect line becomes more inductive, the change in the line impedance characteristics becomes more significant with changing line width. Different interconnect line lengths are examined using Cadence SPICE. The lines are modeled by twenty distributed *RLC* impedance elements. The signal transition time at the far end of the line with a load capacitance of 250 fF is shown in Fig. 5.9. For a short line, the change in the signal transition time is less significant, as the line is not significantly inductive. As the interconnect becomes longer, increasing the inductive behavior, the signal characteristics become more sensitive to changes in the line width. This effect places additional emphasis on determining the optimum line width in longer lines that minimize the total transient power dissipation.

5.4.2 Effect of Interconnect Resistivity

Different interconnect line materials have different resistivities. An increase in the line inductance-to-resistance ratio associated with an increase in the width makes the signal characteristics more sensitive to the matching condition between the driver and the line. Simulations are used to examine

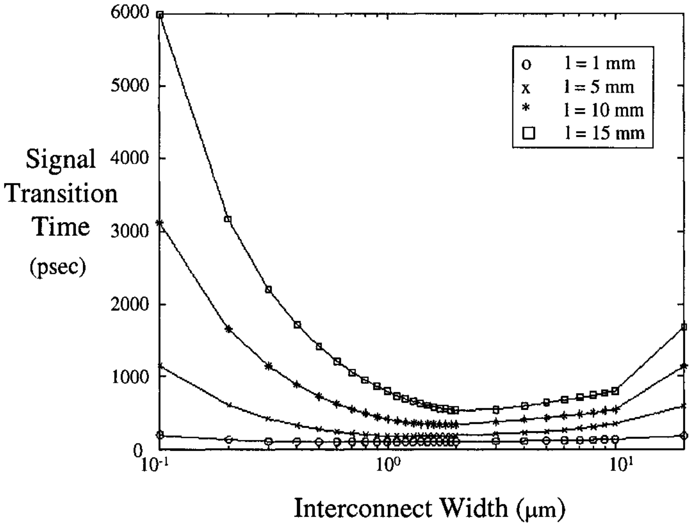


Figure 5.9: Signal transition time versus interconnect width for different line lengths

different interconnect lines with different line materials.

As shown in Fig. 5.10, for wider lines the line resistivity has no effect on the signal characteristics. After exceeding a specific line width (*e.g.*, 3 μm in the specified example), the signal transition time is the same for all line resistivities. For wide lines, the losses along the line are negligible, however, the signal transition time increases. This behavior shows that the increase in the transition time is caused by a change in the matching characteristics and is not due to signal degradation due to resistive losses. When the line inductance dominates the line resistance, the matching characteristics have a more significant effect on the signal behavior.

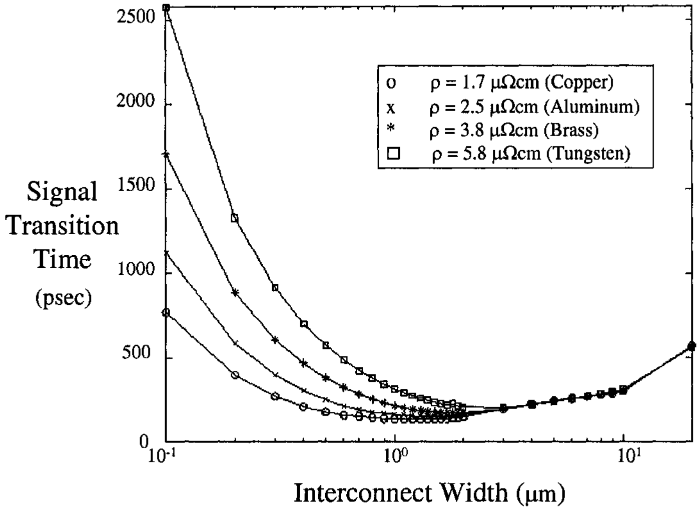


Figure 5.10: Signal transition time versus interconnect width for different materials (*i.e.*, resistivities)

5.5 Simulation Results

Some simulation results are presented in this section to verify the analytic expressions described in section 5.2. In subsection 5.5.1, the accuracy of the analytic solution for the signal transition time at the far end of an inductive interconnect is examined. The expression for the total transient power dissipation is evaluated in subsection 5.5.2. In subsection 5.5.3, the effects of interconnect resistivity and length on reducing power dissipation is verified.

5.5.1 Transition Time

The analytical solution presented in subsection 5.3.1 is compared with SPICE in this subsection. A 0.24 μm CMOS inverter with $W_n = 15\,\mu m$ and $W_p = 30\,\mu m$ is assumed. As listed in Table 5.1, the transition time is determined from (5.10) and compared with SPICE. The line width is varied from 0.1 μm to 20 μm. The maximum error in the analytic solution as compared to SPICE is less than 15% and typically is around 7%. The transition time based on this solution is compared to SPICE in Fig. 5.11.

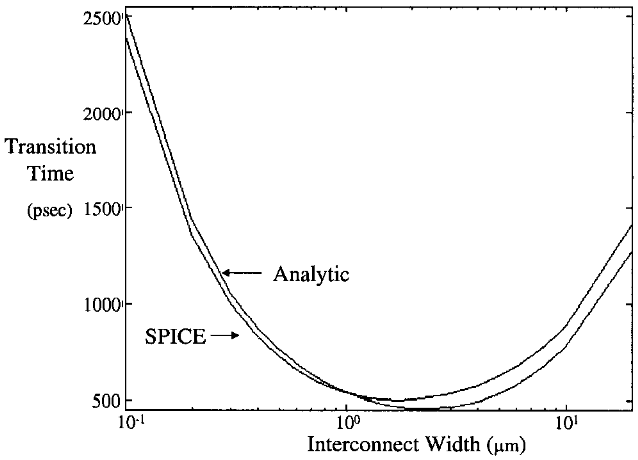


Figure 5.11: Analytic solution of the transition time as compared with SPICE for different line widths

Table 5.1: Simulation and analytic transition times of a signal at the far end of an inductive interconnect line

$W_{INT}(\mu m)$	R_t (Ω)	L_t (nH)	C_p (fF)	τ_0		Error (%)
				Spice	Analytic	
0.1	1250	9.62	628.10	2386.25	2510.71	5.22
0.2	625.00	9.53	652.02	1349.13	1431.80	6.13
0.3	416.67	9.45	670.56	999.88	1050.92	5.11
0.4	312.50	9.37	686.80	826.25	870.73	5.38
0.5	250.00	9.30	701.72	725.00	761.57	5.04
0.6	208.33	9.24	715.80	657.50	688.53	4.72
0.7	178.57	9.18	729.27	614.00	636.50	3.66
0.8	156.25	9.12	742.30	582.44	597.86	2.65
0.9	138.89	9.07	754.98	559.66	568.38	1.56
1	125.00	9.02	767.38	543.03	545.54	0.46
1.1	113.64	8.97	779.56	531.04	528.12	-0.55
1.2	104.17	8.92	791.55	521.84	513.78	-1.54
1.3	96.15	8.88	803.37	515.50	501.13	-2.79
1.4	89.29	8.83	815.06	511.04	490.85	-3.95
1.5	83.33	8.79	826.63	508.09	482.50	-5.04
1.6	78.13	8.75	838.10	506.38	475.75	-6.05
1.7	73.53	8.72	849.47	505.63	470.36	-6.97
1.8	69.44	8.68	860.76	505.69	466.11	-7.83
1.9	65.79	8.65	871.98	506.44	462.86	-8.61
2	62.50	8.61	883.13	507.73	460.45	-9.31
3	41.67	8.32	991.97	537.98	465.83	-13.41
4	31.25	8.10	1097.83	581.59	497.43	-14.47
5	25.00	7.92	1202.00	629.75	538.98	-14.41
6	20.83	7.76	1305.00	678.75	584.86	-13.83
7	17.86	7.63	1407.40	729.79	632.80	-13.29
8	15.63	7.51	1509.10	782.50	681.79	-12.87
9	13.89	7.41	1610.00	835.13	731.34	-12.43
10	12.50	7.31	1711.30	886.04	781.18	-11.83
20	6.25	6.67	2709.85	1411.56	1273.64	-9.77
Maximum Error						14.47
Average Error						7.2

5.5.2 Minimizing the Transient Power

The transient power components can be expressed in terms of the line width. A criterion for determining the interconnect width that minimizes the total transient power is applied in this subsection to a simple example circuit and compared with SPICE.

Using closed form expressions for the line impedance parameters in terms of the line width, the transition time $\tau_0(W_{INT}, W_n)$ as a function of W_n and W_{INT} is obtained. From (5.8) and (5.9), the short-circuit power of the load inverter $P_{2sc}(W_{INT}, W_n)$ can be expressed in terms of the design parameters to obtain an analytic solution for the optimum width so as to minimize power.

For a specific driver size, the total simulated power dissipation for $N = 1, 2, 5$, and 10 is shown in Fig. 5.12. As the number of load gates increases, the total short-circuit power dissipation over a practical range of interconnect widths increases. Determining the optimum width becomes more efficient, since the dynamic power can be traded off with the short-circuit power.

A comparison between the analytic solution and simulation is listed in Table 5.2. The number of load gates is provided in the first column. The effect of applying the optimization criterion on the signal propagation delay is also determined. The optimum interconnect width obtained from the analytic

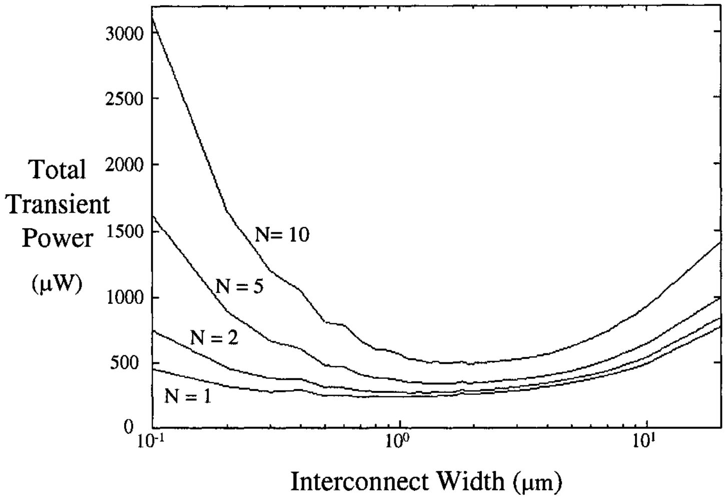


Figure 5.12: Total transient power dissipation for an inverter driving N logic gates as determined by SPICE

solution and simulation is listed in the second and third columns, respectively. A numerical method is used to solve (5.8). The error between the analytic solution and SPICE for the target range of values is less than 6%. The optimum width for minimum power is compared with the optimum width for minimum delay. The per cent increase in signal propagation delay, when the optimum width for minimum power is used, is listed in the last column of the table. The maximum per cent increase in the propagation delay is about 21%.

For N = 10, the total transient power dissipation of a symmetric driver is

Table 5.2: Simulation and analytic results of the optimum width with different loads

Number of Loads	$W_{INT_{optimum}} (\mu m)$		Error (%)	Increase in the delay
N	Analytic	SPICE		from minimum value (%)
1	0.51	0.50	+2.0	21.0
2	0.72	0.70	+2.0	10.8
5	1.06	1.00	+6.0	5.2
10	1.34	1.30	+3.1	4.2

shown in Fig. 5.13. Considering the driver size as a design variable, a different local minimum for the transient power dissipation exists for each driver size. Furthermore, for each line width, a minimum transient power dissipation also exists at a specific driver size. A global minimum for the transient power is obtained by simultaneously solving (5.8) and (5.9) to determine the optimum value for each design variable. For the example circuit shown in Fig. 5.5, the global minimum power of 942 μW is achieved at $W_{INT} = 2.8\,\mu m$ and $W_n = 57\,\mu m$. The reduction in power dissipation is 28%. Rather than minimizing the total transient power, an expression for the propagation delay [61] is used to minimize the power-delay product. The global minimum power-delay product of 91.4 μW nsec is achieved at $W_{INT} = 2.0\,\mu m$ and $W_n = 54\,\mu m$.

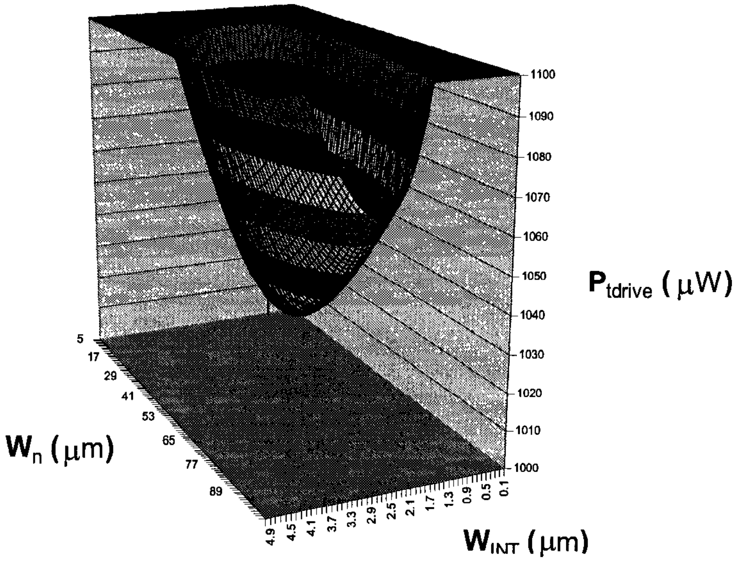


Figure 5.13: Total power dissipation with different wire and driver sizes. The number of load gates N is 10. Note that the minimum power occurs at $W_n = 57\ \mu m$ and $W_{INT} = 2.8\ \mu m$.

5.5.3 Effects of Interconnect Resistivity and Length on Transient Power Dissipation

The proposed criteria for interconnect width optimization is applied to different target circuits. The total transient power dissipation is obtained using three different interconnect widths; thin, optimum, and wide. Different case studies show the importance of the optimization process for reducing power. The optimum width is obtained for two line lengths, $l = 1$ mm (more resistive) and 5 mm (more inductive). For short (resistive) lines, the signal characteristics are not particularly sensitive to the line width. The optimum width, however, achieves a greater power reduction in more inductive lines.

Using the optimum width rather than the minimum width defined by the technology, the total power dissipation is decreased by reducing the short-circuit power. As listed in Table 5.3, the optimum width of a copper line reduces the total transient power by 68.5% for $l = 5$ mm as compared to 28.6% for $l = 1$ mm. For aluminum, a reduction of 77.9% (for l = 5 mm) is achieved as compared to 37.8% (for l = 1 mm). The more inductive the interconnect, the more sensitive the power dissipation is to a change in the line width (and the signal characteristics). Wire width optimization is, therefore, more effective for longer, more inductive lines.

A ten times wide line is used rather than the optimum line. The optimum width reduces the total power dissipation as compared to a wide line. A reduction occurs in both transient power components (short-circuit and dynamic). The per cent reduction in power is listed in the last column of Table 5.3. For both line lengths, the reduction in copper interconnect is higher

Table 5.3: Power reduction for different line parameters

Resistivity ρ $\mu\Omega\, cm$	Total Transient Power Dissipation (μW)				
	Resistive Line (l = 1 mm)				
	Optimum	Thin	Reduction	Wide	Reduction
1.7 (Copper)	583	817	28.6%	808	27.8%
2.5 (Aluminum)	606	976	37.8%	813	25.4%
	Inductive Line (l = 5 mm)				
1.7 (Copper)	1121	3563	68.5%	1931	41.9%
2.5 (Aluminum)	1236	5592	77.9%	1973	37.4%

than the reduction in aluminum interconnect. For l = 5 mm, the per cent reduction in power is 27.8% for copper interconnect as compared to 25.4% for aluminum interconnect. A reduction in copper interconnect of 41.9% is obtained versus 37.4% in aluminum interconnect for l = 1 mm. This result is nonintuitive as the line resistance is higher for aluminum and both lines have the same capacitance and inductance. The absolute value of the power dissipation is actually higher for aluminum interconnect than for copper interconnect. The inductance-to-resistance ratio $\frac{L}{R}$ of the copper interconnect is higher, increasing the importance of the optimum width for less resistive (highly inductive) lines. Alternatively, for thin lines, the line resistance has a greater effect on the signal characteristics. The reduction in power is higher for aluminum interconnect than for copper interconnect (note the reduction in Table 5.3).

5.6 Conclusions

It is shown in this chapter that the power characteristics of inductive interconnects may greatly influence wire sizing optimization techniques. Increasing the interconnect width can decrease the total transient power since the short-circuit power becomes smaller in inductive interconnect. A tradeoff therefore exists between dynamic and short-circuit power in choosing the width of inductive interconnects. This tradeoff is not significant in resistive lines as the signal characteristics are less sensitive to the line dimensions. The short-circuit power of an overdriven interconnect line decreases with line width, while the dynamic power increases. When the line exceeds the matched condition, not only the dynamic power but also the short-circuit power increases with increasing line width. Interconnect optimization criteria should consider changes in the matching characteristics between the line and the driver to achieve optimum circuit performance.

The matching condition between the driver and the load has an important effect on the line impedance characteristics. If the line is overdriven, the short-circuit power decreases with increasing line width. When the line exceeds the matched condition, the short-circuit power increases with increasing line width (and signal transition time). To achieve lower transient power dissipation, the minimum line width should be used if the line is underdriven. For a long inductive interconnect line, an optimum interconnect width exists that minimizes the total transient power dissipation.

An analytic solution of the signal transition time at the far end of an inductive interconnect line is presented and exhibits an error of less than 15%. The solution can be used to optimize the power dissipated by high speed CMOS circuits. An analytic solution is presented for determining this optimum width. This solution has high accuracy, producing an error of less than 6%. The optimum line width is more effective in reducing the total transient power as the line becomes longer. With aluminum interconnect, the power is reduced by about 80% and 37% as compared to thin and wide wires, respectively. For copper interconnect, the power is reduced by 68% and 42% for the same conditions. Greater power reduction is achieved for optimally sized lines with higher resistivity interconnect as compared to minimum width lines. The optimum interconnect width depends upon both the driver size and the size of the load. With this solution, the optimum driver and wire size that dissipate the minimum transient power can be simultaneously determined.

Chapter 6

Wire Sizing Within a Repeater System

6.1 Introduction

Interconnect design has become a dominant issue in high speed integrated circuits (ICs). With the decreased feature size of CMOS circuits, on-chip interconnect now dominates both circuit delay and power dissipation. Many algorithms have been proposed to determine the optimum wire size that minimizes a cost function such as the delay [46].

The number of long interconnects doubles every three years [26], further increasing the importance of on-chip interconnect. The behavior of inductive interconnect can no longer be neglected, particularly in long, low resistance interconnect lines [20]. As on-chip inductance becomes important, some wire optimization algorithms have been enhanced to consider *RLC* impedances

[53, 54]. Previous work has not considered the effect of the interconnect width on the repeater insertion process for long inductive lines.

Uniform repeater insertion is an effective technique for driving long interconnects. Based on a distributed *RC* interconnect model, a repeater insertion technique to minimize signal propagation delay was introduced in [56]. A uniform repeater structure decreases the total delay as compared to a tapered buffer structure when driving long resistive interconnects while buffer tapering is more efficient for driving large capacitive loads [57, 156]. Different techniques have been developed to enhance the model of a repeater system that considers a variety of design factors [157]-[163]. The drain/source capacitance of each repeater and multistage repeaters are considered in [164]. Noise aware techniques for repeater insertion and wire sizing have been described in [165]-[168]. In [169, 170], signal integrity and interconnect reliability and manufacturability issues are discussed.

The work described in [171] assumes that increasing the interconnect width while maintaining the thickness, spacing, and height from the substrate does not reduce the signal delay since the resistance decreases and the capacitance increases. This assumption is not accurate. Different factors affect the total delay such as the coupling capacitance, the driver size, and the load capacitance. Furthermore, with increasing inductive impedances, trends in the propagation delay with changing line width depend upon the number of repeaters and the size of the inserted repeaters.

For an *RC* line, repeater insertion outperforms wire sizing [60]. It is shown in this chapter that this behavior is not the case for an *RLC* line. The minimum signal propagation delay always decreases with increasing line width for *RLC* lines if an optimum repeater system is used.

With increasing demand for low power ICs, different strategies have been developed to minimize power in the repeater insertion process. Power dissipation and area overhead have been considered in previous work [172]-[177]. The line inductance, however, has yet to be considered in the optimization process of sizing a wire driven by a repeater system. As shown in Fig. 6.1, the minimum delay for a signal to propagate along an *RLC* line decreases while the power dissipation increases for wider interconnect [144].

In this chapter, the tradeoff between signal propagation delay and transient power dissipation in sizing a long interconnect driven by a repeater system is discussed. The minimum power delay product is used as a criterion to size long interconnects. Both line inductance and short-circuit power are considered. A new criterion, the Power-Delay-Area-Product (PDAP), is introduced as an efficient criterion to size interconnect within a repeater

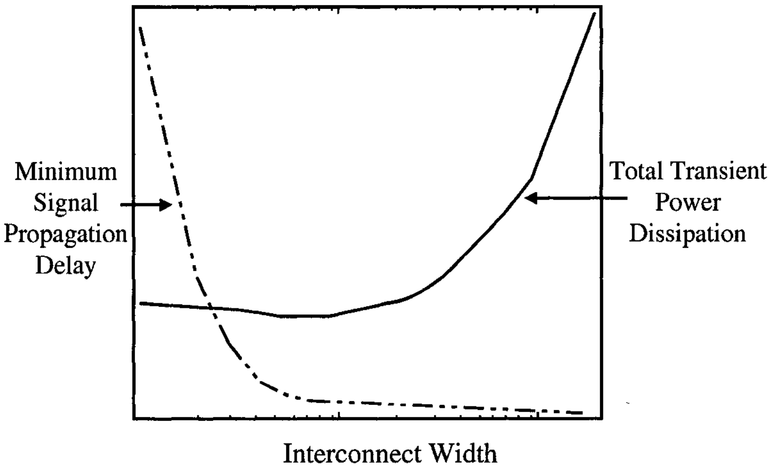


Figure 6.1: Minimum signal propagation delay and transient power dissipation as a function of line width for a repeater system

system.

The chapter is organized as follows. In section 6.2, an overview of a repeater system is presented. The minimum signal propagation delay as a function of interconnect width is described in section 6.3. In section 6.4, the dependence of the transient power dissipation on wire size is discussed. The area of a repeater system is characterized in section 6.5. In section 6.6, different criteria to size an interconnect within a repeater system are presented. These criteria are applied to different example circuits in section 6.7. Some conclusions are provided in section 6.8. In Appendix B, closed form expressions for the line impedance parameters of a shielded interconnect line are provided.

6.2 Overview of the Repeater Insertion Process

The primary objective of a uniform repeater insertion system is to minimize the time for a signal to propagate through a long interconnect. Uniform repeater insertion techniques divide the interconnect into equal sections and employ equal size repeaters to drive each section as shown in Fig. 6.2. In some practical situations, the optimum location of the repeaters cannot be achieved due to physical space constraints. Changing the repeater size can compensate for a change in the ideal physical placement. Bakoglu and Meindl have developed closed form expressions for the optimum number and size of repeaters to achieve the minimum signal propagation delay in an *RC* interconnect [56]. Adler and Friedman characterized a timing model for a CMOS inverter driving an *RC* load [58, 59]. They used this model to enhance the accuracy of the repeater insertion process in *RC* interconnects. Alpert considered the interconnect width as a design parameter [60]. He showed that, for *RC* lines, repeater insertion outperforms wire sizing.

The delay can be greatly affected by the line inductance, particularly low resistance materials with fast signal transitions. Ismail and Friedman

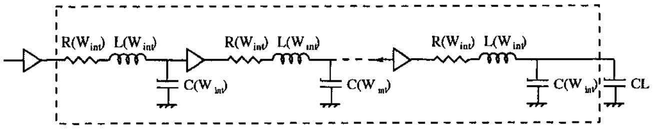


Figure 6.2: Uniform repeater system driving a distributed *RLC* interconnect

extended previous research in repeater insertion by considering the line inductance [61]. They showed that on-chip inductance can decrease the delay, area, and power of the repeater insertion process as compared to an *RC* line model [130]. Banerjee and Mehrotra developed an analytic delay model and methodology for inserting repeaters into distributed *RLC* interconnect which demonstrated the importance of including line inductance as technology advances [62]-[65].

Interconnect sizing within a repeater system affects two primary design parameters, the number of repeaters and the optimum size of each repeater as shown in Fig. 6.3. Different tradeoffs in sizing long inductive interconnect driven by an optimum repeater system are investigated in this chapter. Design criteria are developed to determine the optimum width, while considering different design objectives, such as the delay, power, and area.

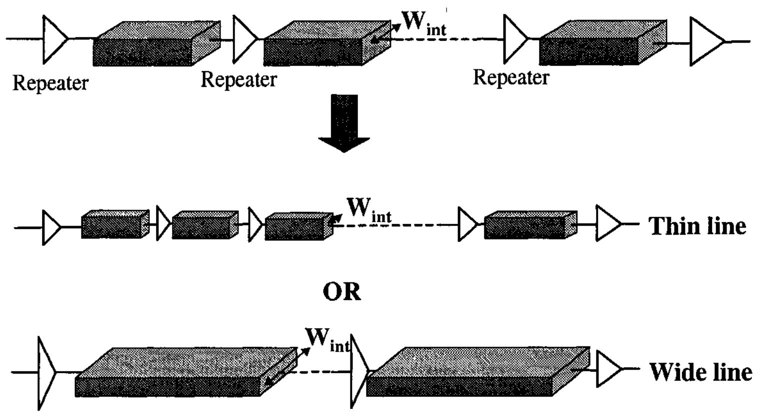


Figure 6.3: Wire sizing in a repeater insertion system

6.3 Propagation Delay

The interconnect resistance decreases with increasing line width, increasing $\frac{L}{R}$, the ratio between the line inductance and resistance. An increase in $\frac{L}{R}$ decreases the number of inserted repeaters to achieve the minimum propagation delay. For an *RLC* line, the minimum signal propagation delay decreases with wider wires until no repeaters should be used. Wire sizing outperforms repeater insertion in *RLC* lines.

Expressions for the optimum number of repeaters $k_{opt-RLC}$ and the optimum repeater size $h_{opt-RLC}$ [61] are

$$k_{opt-RLC}(W_{int}) = \sqrt{\frac{R_{int}(W_{int})C_{int}(W_{int})}{2.3R_0C_0}}\frac{1}{[1+0.16(T_{L_{int}/R_{int}}(W_{int}))^3]^{0.24}}, \tag{6.1}$$

$$h_{opt-RLC}(W_{int}) = \sqrt{\frac{R_0C_{int}(W_{int})}{R_{int}(W_{int})C_0}}\frac{1}{[1+0.18(T_{L_{int}/R_{int}}(W_{int}))^3]^{0.3}}, \tag{6.2}$$

where

$$T_{L_{int}/R_{int}}(W_{int}) = \sqrt{\frac{L_{int}(W_{int})/R_{int}(W_{int})}{R_0C_0}}. \tag{6.3}$$

C_0 and R_0 are the input capacitance and output resistance of a minimum size repeater, respectively. $R_{int}(W_{int})$, $C_{int}(W_{int})$, and $L_{int}(W_{int})$ are the interconnect line resistance, capacitance, and inductance as a function of the interconnect width. Closed form expressions for the line impedance parameters as a function of the interconnect width are provided in Appendix B.

For copper interconnect line, low κ dielectric material, $R_0 = 2$ KΩ, and $C_0 = 1$fF, $k_{opt-RLC}$ is determined from (6.1). For different line lengths l, the optimum number of repeaters $k_{opt-RLC}$ is illustrated in Fig. 6.4. It is shown in the figure that for an *RLC* line, the optimum number of repeaters which minimizes the signal propagation delay decreases with an increase in the line width for all line lengths. The number of repeaters reaches zero (or only one driver at the begining of the line) for an interconnect width = 3 μm and 4 μm for l = 5 mm and 10 mm, respectively. For widths greater than 4 μm, the wire should be treated as one segment. A repeater system should not be used above a certain width for each line length.

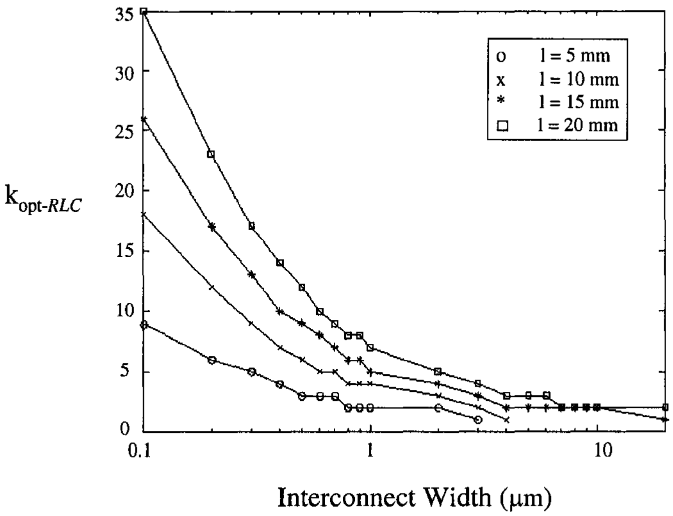


Figure 6.4: Optimum number of repeaters for minimum propagation delay for different line widths

The line capacitance per unit length increases with line width. As the number of inserted repeaters decreases with wider lines, a longer line section is driven by each repeater. An increase in the section length and width increases the capacitance driven by each repeater. To drive a high capacitive load, a larger repeater size is required to decrease the overall delay. As shown in Fig. 6.5, the optimum repeater size $h_{opt-RLC}$ is an increasing function of line width.

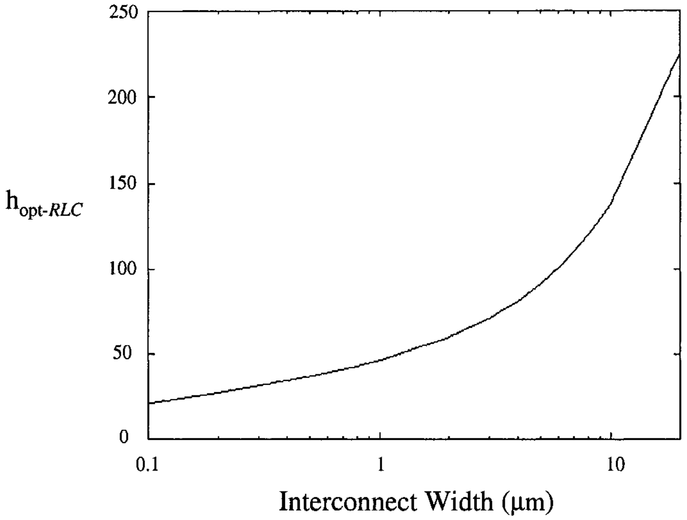


Figure 6.5: Optimum repeater size for minimum propagation delay for different line widths

The minimum signal propagation delay of an optimum repeater system decreases with increasing line width as the total gate delay decreases. For an inductive interconnect line, the total signal propagation delay is

$$t_{pd-total}(W_{int}) = k_{opt-RLC}(W_{int})\, t_{pd-section}(W_{int}), \tag{6.4}$$

where $t_{pd-section}(W_{int})$ is the signal delay of each RLC section as a function of the interconnect width.

$$
\begin{aligned}
t_{pd-section}(W_{int}) &= \frac{e^{-2.9\zeta^{1.35}}}{\omega_n} + 0.74(R_{tr}(W_{int})C_{section}(W_{int}) + R_{section}(W_{int})C_L(W_{int}) \\
&+ R_{tr}(W_{int})C_L(W_{int}) + 0.5R_{section}(W_{int})C_{section}(W_{int})), \qquad (6.5)
\end{aligned}
$$

where

$$
\begin{aligned}
\zeta &= \frac{\omega_n}{2}(0.5C_{section}(W_{int})R_{section}(W_{int}) + C_{section}(W_{int})R_{tr}(W_{int}) \\
&+ C_L(W_{int})(R_{section}(W_{int}) + R_{tr}(W_{int}))), \qquad (6.6) \\
\omega_n &= \frac{1}{\sqrt{L_{section}(W_{int})(C_{section}(W_{int}) + C_L(W_{int}))}}, \qquad (6.7)
\end{aligned}
$$

$$C_L(W_{int}) = C_{section}(W_{int}) + h_{opt-RLC}(W_{int})C_0. \qquad (6.8)$$

$$
\begin{aligned}
R_{tr}(W_{int}) &= \frac{R_0(W_{int})}{h_{opt-RLC}(W_{int})}, \qquad (6.9) \\
R_{section}(W_{int}) &= \frac{R_{line}(W_{int})}{k_{opt-RLC}(W_{int})}, \qquad (6.10) \\
L_{section}(W_{int}) &= \frac{L_{line}(W_{int})}{k_{opt-RLC}(W_{int})}, \qquad (6.11) \\
C_{section}(W_{int}) &= \frac{C_{line}(W_{int})}{k_{opt-RLC}(W_{int})}. \qquad (6.12)
\end{aligned}
$$

The minimum delay [obtained from (6.4)] is shown in Fig. 6.6 as a function of interconnect width. An increase in the inductive behavior of the line and a reduction in the number of repeaters decreases the minimum signal propagation delay that can be achieved by a repeater system.

The signal delay for different line lengths is shown in Fig. 6.7. The lower limit in the propagation delay decreases with increasing line width until the

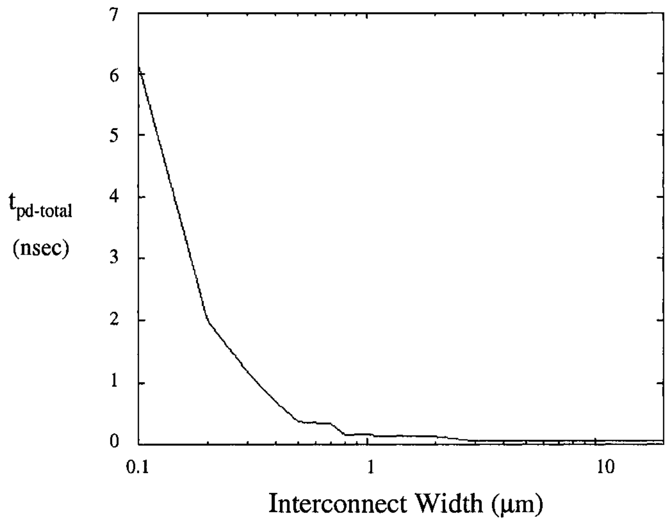


Figure 6.6: Minimum signal propagation delay as a function of interconnect width ($l = 5$ mm)

number of repeaters is zero. For a system of repeaters, there is no optimum width at which the total propagation delay is minimum. Rather, the delay is a continuously decreasing function of the line width. The propagation delay with no repeaters in an *RLC* line produces a smaller signal propagation delay than using any number of repeaters with any repeater size. For *RLC* interconnect, wire sizing outperforms repeater insertion, producing a smaller signal propagation delay. This characteristic is an important trend when developing a wire sizing methodology for a repeater system.

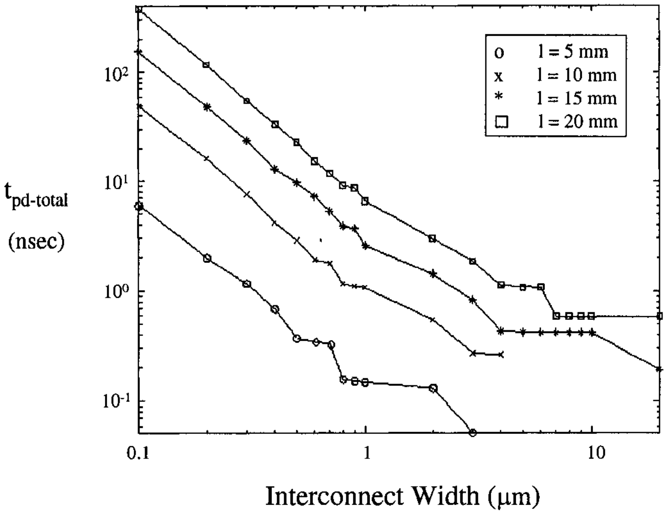


Figure 6.7: Minimum signal delay as a function of interconnect width for different line lengths

6.4 Power Dissipation

The power characteristics of a repeater insertion system is discussed in this section. The work described in [172]-[177] considers power and area as design constraints. The line inductance, however, has not been considered. In subsection 6.4.1, the factors that affect the short-circuit power while considering the line inductance of an interconnect driven by a repeater system is discussed. The dependence of the dynamic power on wire size is described in subsection 6.4.2. The total transient power dissipation characteristics are summarized in subsection 6.4.3.

6.4.1 Short-Circuit Power Dissipation

Short-circuit current flows when both transistors within an inverting repeater are simultaneously on. Thin lines cause less dynamic power and higher short-circuit power to be dissipated. For thin resistive lines, the number of repeaters can be large. The short-circuit power dissipation in all repeaters along a line is considered. Short-circuit power depends on both the input signal transition time and the load characteristics. A simple and accurate expression for the short-circuit power dissipation of a repeater driving an *RC* load has been presented in [58],

$$P_{sc-section} = \frac{1}{2} I_{peak}\, t_{base}\, V_{dd}\, f, \tag{6.13}$$

where I_{peak} is the peak current that flows from V_{dd} to ground, t_{base} is the time period during which both transistors are on, V_{dd} is the supply voltage, and f is the switching frequency.

Tang used this expression to characterize the short-circuit power of an *RLC* load [125]. A closed form expression for the signal transition time at the far end of an *RLC* line has been described in [142]-[146]. Increasing the line width has two competing effects on the short-circuit power. As described in [144], the short-circuit power decreases when a line is underdamped. For wide interconnect, the short-circuit power increases as the line capacitance becomes dominant. Furthermore, increasing the length of the section by reducing the number of repeaters increases the short-circuit power of each section due to the higher section impedance.

The total short-circuit power of a repeater system is

$$P_{sc-total} = k_{opt-RLC}\, P_{sc-section}. \tag{6.14}$$

Equation (6.14) is used in subsection 6.4.3 to characterize the power dissipation in terms of the interconnect width.

6.4.2 Dynamic Power Dissipation

The dynamic power is the power required to charge and discharge the various device and interconnect capacitances. The total dynamic power is the summation of the CV^2f power from the line capacitance and the repeaters.

$$P_{dyn-total} = P_{dyn-line} + P_{dyn-repeaters}, \tag{6.15}$$

where

$$P_{dyn-repeaters} = k_{opt-RLC}\, h_{opt-RLC}\, C_0\, {V_{dd}}^2\, f, \tag{6.16}$$

$$P_{dyn-line} = C_{int}\, {V_{dd}}^2\, f. \tag{6.17}$$

C_0 and C_{int} are the input gate capacitance of a minimum size repeater and the interconnect capacitance, respectively. $P_{dyn-repeaters}$ depends on both the number and size of each repeater. While the number of repeaters decreases, the repeater size increases.

The dynamic power dissipated by a line increases with greater line capacitance (as the line width is increased). The dynamic power of the repeaters, however, decreases since fewer repeaters are used with wider lines. As shown in Fig. 6.8, the total dynamic power is a minimum for thin interconnect. The effect of sizing the interconnect on the total transient power dissipation is discussed in subsection 6.4.3.

6.4.3 Total Power Dissipation

In order to develop an appropriate criterion for determining the optimal interconnect width between repeaters, the total transient power dissipation of a system needs to be characterized. The total transient power can be described as

$$\begin{aligned} P_{total}(W_{int}) &= V_{dd} f [k_{opt-RLC}(W_{int}) \, (\frac{1}{2} I_{peak}(W_{int}) \, t_{base}(W_{int}) \\ &+ h_{opt-RLC}(W_{int}) V_{dd} \, C_0) + V_{dd} \, C_{int}(W_{int})]. \qquad (6.18) \end{aligned}$$

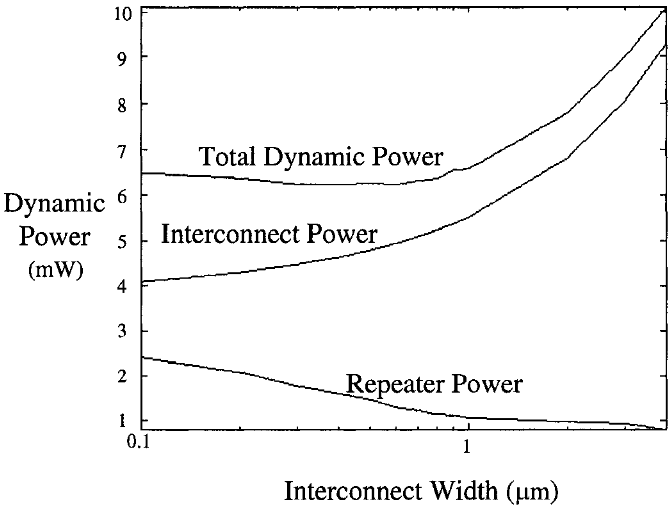


Figure 6.8: Dynamic power dissipation as a function of interconnect width for l = 20 mm

All of the terms in (6.18) are functions of the line width except V_{dd}, C_0, and f. As described in subsections 6.4.1 and 6.4.2, both transient power components decrease with increasing line width, thereby decreasing the total power until the line capacitance becomes dominant.

For an *RLC* interconnect, fewer repeaters are necessary to drive a line while achieving the minimum propagation delay [61]. For an inductive interconnect, the interconnect capacitance is typically larger than the input capacitance of the repeaters. Increasing the width reduces the power dissipation of the repeaters and increases the power dissipation of the line. The reduction in power dissipated by the repeaters overcomes the increase in the interconnect power until the line capacitance dominates the line impedance. After exceeding a certain width, the total power increases with increasing line width.

The total power dissipation as a function of line width for different interconnect lengths is shown in Fig. 6.9. As the line width increases from the minimum width (*i.e.,* 0.1 μm in the example technology), the total power dissipation is reduced. A minimum transient power dissipation therefore occurs with thin interconnect (see Fig. 6.9). The minimum transient power dissipation is obtained from

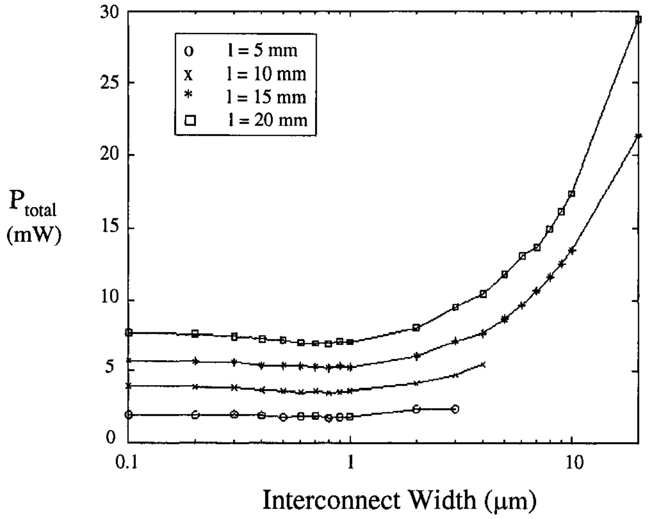


Figure 6.9: Total transient power dissipation as a function of interconnect width

$$\frac{\partial P_{total}}{\partial W_{int}} = 0, \tag{6.19}$$

where $\frac{\partial P_{total}}{\partial W_{int}}$ is a nonlinear function of W_{int}. Numerical methods are used to obtain values of W_{int} for specific interconnect and repeater parameters.

Over a range of practical interconnect width, the total transient power increases as shown in Fig. 6.9. As the line length increases, the total power dissipation rapidly increases with increasing line width as the interconnect capacitance becomes dominant. In section 6.6, the tradeoff between signal delay and power dissipation is considered in the development of a criterion for interconnect sizing.

6.5 Area of the Repeater System

For a specific interconnect width within a repeater system, the optimum number and size of the repeaters can be determined. Previous studies on repeaters have considered the silicon area, ignoring the metal layer resources [172]-[177]. Long global interconnects are typically wide and require shielding [178]-[181]. In order to develop appropriate criteria for considering the area overhead, both the silicon and interconnect area need to be characterized [10]-[12]. The area of the interconnect metal can be described as

$$A_{line}(W_{int}) = W_{int}\, l\,. \tag{6.20}$$

The interconnect metal area is illustrated in Fig. 6.10 as a function of the interconnect width. For CMOS inverters used as repeaters, the total silicon area of the active repeaters is

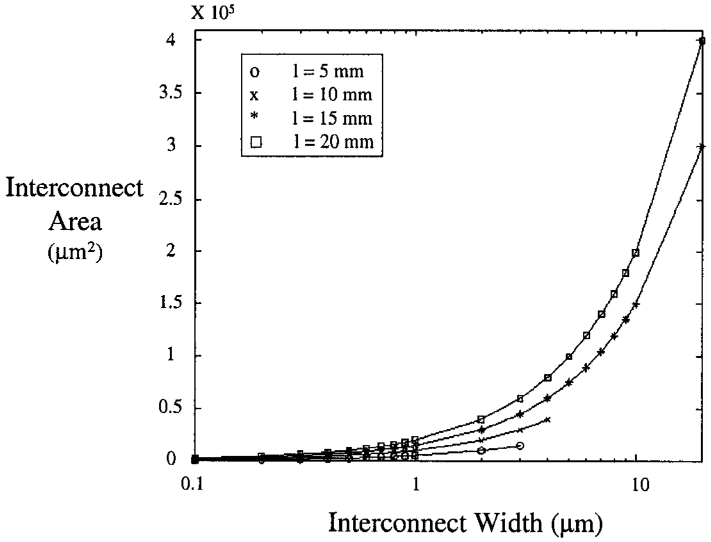


Figure 6.10: Interconnect area as a function of interconnect width for different line lengths

$$A_{repeater}(W_{int}) = 3\, k_{opt-RLC}(W_{int})\, h_{opt-RLC}(W_{int})\, {L_n}^2, \tag{6.21}$$

where L_n is the feature size. The PMOS transistor of each repeater is assumed to be twice the size of the NMOS transistor to achieve a symmetric transition.

For an *RLC* line, fewer repeaters are needed to minimize the propagation delay, reducing the silicon area as shown in Fig. 6.11.

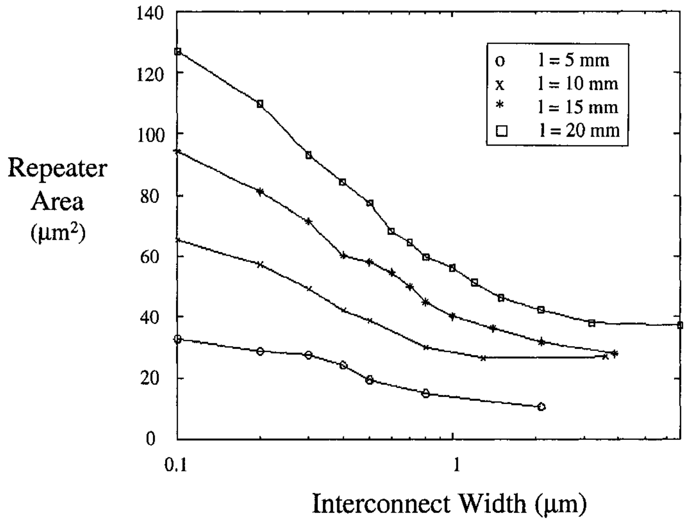


Figure 6.11: Total area of the repeaters as a function of the interconnect width for different line lengths

The active repeaters and the passive interconnects utilize different layers, making the area overhead of both elements independent, particularly for interconnects routed on the upper layers. A weighted product in (6.22) is used as a criterion to consider both area parameters in sizing the interconnect,

$$A_{product}(W_{int}) = A_{repeater}(W_{int})^{w_r} A_{line}(W_{int})^{w_l}, \tag{6.22}$$

where w_r and w_l are the weights of the two cost functions.

For $w_r = w_l = 1$, the area product of the system increases with different interconnect widths as shown in Fig. 6.12. Despite the reduction in repeater area with increasing interconnect width, the increased area occupied by the interconnect increases the overall area of the repeater system. In section 6.6, different design criteria are developed to size an interconnect within a repeater system.

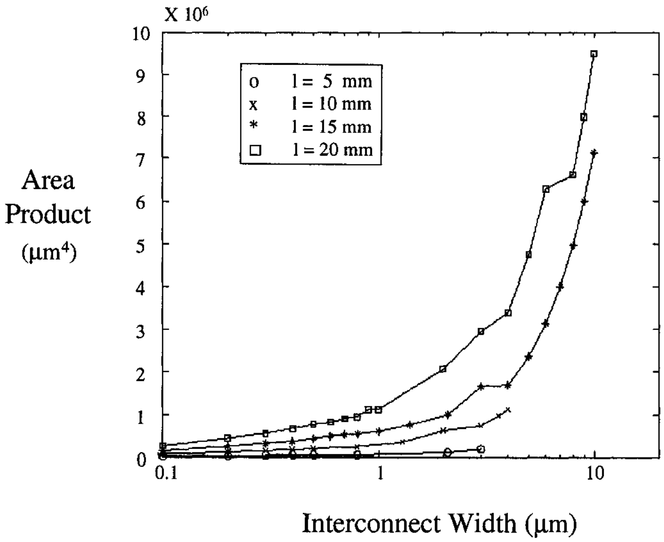


Figure 6.12: Product of interconnect and silicon area as a function of the interconnect width for different line lengths

6.6 Design Criteria for Interconnect Within a Repeater System

In this section, different design criteria to size interconnect within a repeater system are developed. The optimization criteria have been applied to different repeater systems. The results are summarized in section 6.7. In subsection 6.6.1, a constrained system is considered. Application to an unconstrained system is discussed in subsection 6.6.2.

6.6.1 Constrained Systems

For a constrained system, there is a delay target (minimum speed or maximum delay) and/or a limit on the power dissipation. The minimum signal propagation delay determines a lower limit on the line width while the maximum power dissipation determines the upper limit.

If the minimum limit on the line width obtained from (6.4) is greater than the maximum width obtained from (6.18), both limits cannot be simultaneously satisfied and one of the design constraints needs to be relaxed. If the minimum limit is lower than the maximum limit, both constraints can be satisfied.

For a constrained system, the silicon or metal area has an upper limit. The two factors change differently with the width; therefore, there is a tradeoff between the two area components.

6.6.2 Unconstrained Systems

For an *RLC* line, there are four criteria to size interconnect in an unconstrained system. The first criterion is for minimum power while sacrificing speed. The optimum solution for this criterion is obtained from (6.19).

The second criterion is for minimum delay. As no optimum interconnect width exists for minimum propagation delay, the practical limit is either the maximum repeater size or no repeaters, whichever produces a tighter constraint. The constraint in this case is either the maximum repeater size or the maximum line width. The optimum number of repeaters for a target line width is determined from [61]. If not possible, no repeaters should be used and the design problem reduces to choosing the width of a single section of interconnect [144].

The third and fourth criteria are presented in the following subsections. In subsection 6.6.2, the power-delay-product (PDP) as a criterion to size an interconnect within a repeater system is described. The power-delay-area-product (PDAP) is introduced in subsection 6.6.2 as an alternative design criterion.

Power-Delay-Product Design Criterion

The PDP criterion satisfies both the power dissipation and speed with no constraints on the area. From the discussions in sections 6.3 and 6.4, the minimum signal propagation delay of an *RLC* interconnect driven by a repeater system decreases with increasing line width. Alternatively, the total transient power has a global minimum at a narrow width. Over the entire range of line width, the total transient power increases with increasing line width. At a line width smaller than the line width for minimum power, the power and delay both increase. An upper limit on the line width is reached where the minimum propagation delay of a repeater system is attained. Beyond that limit, a single segment sizing criterion should be used to optimize the width according to a cost function (*i.e.,* delay [46] or power [142]-[146]). Between these two limits, a tradeoff exists between the power dissipation and signal propagation delay. A single expression for the power-delay-product (PDP) as a function of the interconnect width is

$$PDP(W_{int}) = P_{total}(W_{int})^{w_p}\, t_{pd-total}(W_{int})^{w_d}, \tag{6.23}$$

where w_p and w_d are the weights of the cost functions. A local minimum for the power delay product exists for each line length. The minimum power delay product is obtained by numerically solving the nonlinear equation,

$$\frac{\partial PDP}{\partial W_{int}} = 0. \tag{6.24}$$

The weights w_p and w_d describe which design objective is more highly valued.

Power-Delay-Area-Product Design Criterion

The criterion described in section 6.6.2 does not include the area of the system as a design parameter. In order to include the area of the system, the PDAP criterion is introduced. This criterion satisfies both the power dissipation and speed while considering area. The Power-Delay-Area-Product (PDAP) can be used as a criterion to size the interconnect. A single expression for the PDAP as a function of the interconnect width is

$$PDAP(W_{int}) = P_{total}(W_{int})^{w_p}\, t_{pd-total}(W_{int})^{w_d}\, A_{repeater}(W_{int})^{w_r}\, A_{line}(W_{int})^{w_l}. \tag{6.25}$$

A local minimum for the PDAP exists for each line length. The minimum PDAP is obtained by numerically solving the nonlinear equation,

$$\frac{\partial PDAP}{\partial W_{int}} = 0. \tag{6.26}$$

In the following section, different criteria are applied to different systems to size the interconnect within a repeater system. Different tradeoffs among the delay, power, and area are discussed.

6.7 Application of Interconnect Design Methodology

The four criteria are applied to a 0.24 μm CMOS technology to determine the optimum solution for different line lengths. No limit on the maximum buffer size is assumed. In order to characterize the line inductance in terms of the geometric dimensions, an interconnect line shielded by two ground lines is assumed. An interconnect line with resistance per square $R_2 = 25$ mΩ/Λ, capacitance per unit length for minimum width $C_{Wmin} = 66$ fF/mm, and inductance per unit length for minimum width $L_{Wmin} = 1$ nH/mm is used. For a repeater system with the following characteristics, $C_0 = 1\ fF$ and $w_p = w_d = 1$, the optimum solution for each criterion is listed in Table 6.1. A clock signal with a 20 psec transition time ramp input signal and 250 MHz frequency is used to determine the propagation delay and power dissipation.

The optimum line width for each design criterion is listed in the first row for each line length. The optimum number and size of the repeaters for each line width is listed in the second and third row of each line length. The per cent increase in the minimum propagation delay based on the optimum power and PDP as compared to no repeaters is also listed. The per cent increase in the total transient power dissipation is provided.

For an $l = 5$ mm line, the optimum interconnect width for both minimum PDP and no repeaters is the same, producing a 14.5% increase in power as compared to the optimum width for minimum power and a reduction of 68% as compared to the optimum width for minimum signal propagation delay.

For short interconnects, few repeaters are necessary to produce the minimum propagation delay. For longer interconnect, an increase in the line capacitance rapidly increases the power dissipation, while the minimum propagation delay decreases more slowly.

For $l = 15$ mm, the optimum solution that minimizes PDP increases the delay by 1.26 rather than 20 times for the solution for minimum power. The power increases by 45% rather than 3.1 times for the no repeater solution. Optimizing the interconnect to produce the minimum power delay product produces a smaller increase in both the power and delay as compared to separately optimizing either the power or delay. A reduction in the minimum propagation delay of 89% and in the power dissipation of 65% is achieved if the optimum width for the minimum PDP is used rather than the optimum width for either minimum power or no repeaters.

In order to consider the area of a repeater system, the PDAP criterion is used to size the interconnect. For $w_l = w_r = 1$, the minimum interconnect width is determined from the optimum solution for the minimum area product. The optimum solution for each criterion is listed in Tables 6.2 and 6.3.

For an $l = 5$ mm line, the optimum interconnect width for both minimum PDP and PDAP is the same, producing the same reduction in delay and increase in power as compared to the criteria listed in Table 6.1. However, both design objectives (delay and power) are decreased as compared to the minimum width. A reduction in delay of 90% and total power dissipation of 14% is achieved when the PDAP criterion is used. Furthermore, the silicon area is decreased by 67% while the interconnect uses more metal resources.

For $l = 15$ mm, a design based on the minimum PDAP criterion dissipates more power as compared to a design based on the PDP criterion. A reduction in power of 23% is achieved with a negligible increase in the propagation delay. Moreover, the interconnect area decreases from 39 times to 21 times the area of the minimum width, achieving a reduction of 46% in the metal area occupied by the interconnect line. As the interconnect line length increases, the PDAP criterion becomes more efficient if area is considered in the optimization process.

6.8 Conclusions

Repeater insertion outperforms wire sizing in *RC* lines. However, for *RLC* lines the minimum signal propagation delay always decreases with increasing wire width if an optimum repeater system is used. In *RLC* lines, wire sizing outperforms repeater insertion as the minimum signal propagation delay with the optimum width using no repeaters along the line is less than the minimum signal propagation delay using any number of repeaters. The minimum signal propagation delay always decreases with wider lines until the number of repeaters equals zero. In *RLC* lines, there is no optimum interconnect width for minimum signal propagation delay.

The total transient power dissipation of a repeater system driving an *RLC* line is minimum at small line widths. Below the width for minimum power, both the signal delay and the power dissipation increase. Increasing the line width above the width for minimum power reduces the number of repeaters and the minimum signal propagation delay while increasing the total transient power dissipation. A tradeoff between the transient power dissipation and the signal propagation delay, therefore, exists in sizing the interconnect width.

Optimizing the interconnect for minimum power delay product produces a much smaller increase in both the power and delay as compared to separately optimizing for either the power or delay. As the interconnects becomes longer, the difference between the optimum width for minimum power and the optimum width for minimum delay increases, further enhancing the effectiveness of the proposed criterion. A reduction in power of 65% and minimum delay of 97% is achieved for an example repeater system driving a long interconnect.

A criterion, Power-Delay-Area-Product (PDAP), is introduced as an efficient technique to size an interconnect within a repeater system if the system area is considered in the design process. A greater reduction in power dissipation of around 23% is achieved with a negligible increase in propagation delay if the line width is optimized for minimum PDAP rather than minimum PDP. Furthermore, a reduction in silicon area of 67% and metal area of 46% is achieved if the PDAP criterion is used.

Table 6.1: Uniform repeater system for different optimization criteria

$l = 5$ mm		Minimum Power	No Repeaters	Minimum PDP
W_{int} (μm)		0.8	2.1	2.1
Number of Repeaters		1	0	0
Repeater Size (of minimum)		43.3	61.2	61.2
Minimum Delay (nsec)	Total	0.157	0.051	0.051
	Increase (times)	2	1	1
Power (mW)	Total	1.73	1.98	1.98
	Increase (%)	0%	14.5%	14.5%
$l = 15$ mm		Minimum Power	No Repeaters	Minimum PDP
W_{int} (μm)		0.8	20	3.9
Number of Repeaters		5	0	1
Repeater Size (of minimum)		43.2	225.6	80.7
Minimum Delay (nsec)	Total	3.87	0.19	0.43
	Increase (times)	19.36	1	1.26
Power (mW)	Total	5.2	21.31	7.58
	Increase (%)	0%	310%	45.7%

Table 6.2: Uniform repeater system for different optimization criteria for $l = 5$ mm

$l = 5$ mm		Minimum Width	Minimum PDP	Minimum PDAP
W_{int} (μm)		0.1	2.1	2.1
Number of Repeaters		8	0	0
Repeater Size (of minimum)		21.0	61.2	61.2
Minimum Delay (nsec)	Total	0.52	0.051	0.051
	Reduction (%)	0%	90.2%	90.2%
Power (mW)	Total	2.3	1.98	1.98
	Reduction (%)	0%	14%	14%
Interconnect Area (μm^2)		500	10500	10500
	Increase (times)	1	21	21
Silicon Area (μm^2)	Total	33	11	11
	Reduction (%)	0%	66.7%	66.7%

Table 6.3: Uniform repeater system for different optimization criteria for $l = 15$ mm

$l = 15$ mm		Minimum Width	Minimum PDP	Minimum PDAP
W_{int} (μm)		0.1	3.9	2.1
Number of Repeaters		25	1	2
Repeater Size (of minimum)		21.0	80.7	61.2
Minimum Delay (nsec)	Total	2.2	0.43	0.44
	Reduction (%)	0%	80.5%	80.0%
Power (mW)	Total	8.26	7.58	6.34
	Reduction (%)	0%	8.2%	23.2%
Interconnect Area (μm^2)		1500	58500	31500
	Increase (times)	1	39	21
Silicon Area (μm^2)	Total	94	28	32
	Reduction (%)	0%	70.2%	66.0%

Chapter 7

Shielding Effect of On-Chip Interconnect Inductance

7.1 Introduction

With the decrease in feature size of CMOS circuits, on-chip interconnect dominates both circuit delay and power dissipation. Interconnect resistance increases the importance of modeling the interconnect as a distributed load. Based on different *RC* models, the signal propagation delay through a resistive load has been characterized [182]-[188]. These models consider the delay of the passive load, ignoring the delay of the gate which drives the load. Furthermore, the effect of the load resistance on the gate delay is not considered. The driver gate should also be included in the delay model for enhanced delay estimation [189]-[191]. Based on a reduced order model of the driving point impedance [192, 193], the concept of an effective capacitance has been introduced in [194] to better determine the gate delay. An iterative approach is proposed to determine the delay of a gate driving an *RC* tree. It has been shown that the effective capacitance of a distributed load is less than the total load capacitance, effectively reducing the gate delay. An enhanced method has been developed to replace the iterative approach [195]. As shown in [196], an effective capacitance improves the accuracy of the delay model.

In order to determine the effective capacitance seen by a driver, a reduced order model for the driving-point admittance is required. An efficient model for the driving-point characteristics of resistive interconnects is presented in [192, 193, 197, 198]. An accurate approximation is provided to estimate the delay of a gate driving an *RC* load [194]. The inductive behavior of interconnect, however, can no longer be neglected, particularly in long, low resistance interconnect lines [20, 199]. The inductive interconnect increases the on-chip noise as well as the computational complexity of the design process. Furthermore, the on-chip inductance affects certain design techniques such as repeater insertion [61]. It is shown in this chapter that the on-chip inductance can also decrease the signal propagation delay. The concept of an effective capacitance based on a high order model for the driving point admittance can be used to determine the gate delay of an *RLC* load.

The propagation delay of an inductive load has been previously analyzed in the literature. Most of these investigations replace the driver with a linear resistance [61], [200]-[207]. The accuracy of these models depends upon the ratio between the driver impedance and the load impedance and the accuracy of the model used to represent the equivalent impedance of the driver. The work described in [125] uses a more accurate driver model, with a lumped model for the load. A more accurate model for both the driver and the load is used in this chapter to demonstrate a new concept, the shielding effect of the load inductance. The shielding effect of the load inductance is used to characterize the effective capacitance of an *RLC* load. In order to determine the effective capacitance of an *RLC* load, a realizable reduced order model is used to characterize the load [208]-[210].

As shown in this chapter, the line inductance decreases the delay of the gate driving the load, increasing the interconnect delay. The total circuit delay may decrease with higher inductance as shown in Fig. 7.1. This result is the first to show (to the authors' knowledge) that interconnect inductance can decrease the delay of a circuit. The minimum delay occurs when the load is matched with the driver. From a noise perspective, the line inductance should be suppressed. As described in this chapter, however, the line inductance can save power and area. Furthermore, if the line is matched with the driver, any ringing effects are eliminated in the signal waveform.

The chapter is organized as follows. In section 7.2, the effective capacitance of an *RLC* load as compared to an *RC* load is presented. The effect of inductive shielding on the total propagation delay is discussed in section 7.3. In section 7.4, a comparison between inductive shielding and resistive shielding is described. An analytic solution for the signal propagation delay of an inverter driving an inductive load is provided in section 7.5. In section 7.6, a comparison between the analytic model and simulation is presented. Some conclusions are offered in section 7.7.

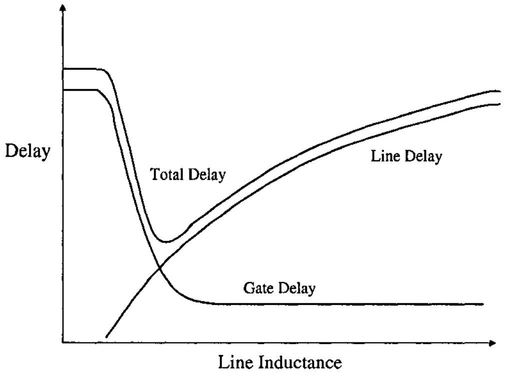


Figure 7.1: Propagation delay as a function of the line inductance

7.2 Effective Capacitance of *RLC* Interconnect

Reduced order models are used to increase the computation efficiency of the timing analysis process. A lumped model of an *RLC* load which uses the first two moments of the transfer function is shown in Fig. 7.2a. The lumped model suffers from significant inaccuracy. Furthermore, the shielding effect of the load inductance is not considered. A circuit representation of a three moment reduced order model (π_{21} model) is shown in Fig. 7.2b [192, 193].

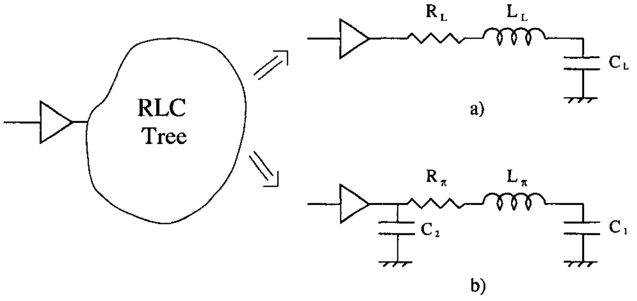


Figure 7.2: Reduced order model for a general *RLC* tree a) Lumped model b) π_{21} model

An efficient technique is presented in [208] to determine the values of R_π, L_π, C_1, and C_2 for a general *RLC* load. If the interconnect inductance is not considered, the π_{21} *RLC* model reduces to an π_{21} *RC* model with the same values of R_π, C_1, and C_2 [209, 210].

Intuitively, the effective capacitance is the equivalent capacitance which replaces the reduced order π_{21} model while producing the same delay at the load (as shown in Fig. 7.3). The effective capacitance of an RLC load is

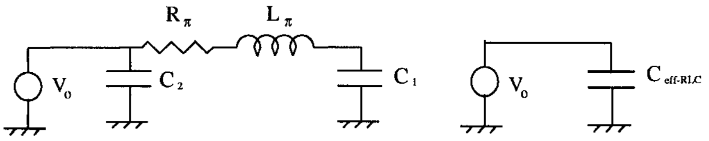


Figure 7.3: Effective capacitance of π_{21} RLC model

$$C_{eff-RLC} = C_2 + C_{x-RLC}, \tag{7.1}$$

where C_{x-RLC} is characterized in Appendix C. C_{x-RLC} is less than C_1, reducing the total capacitance seen by the driver for the π_{21} model as compared to a lumped model. C_{x-RC} is determined for an RC load in [194]. C_{x-RLC} is less than C_{x-RC} for an inductive load. C_{x-RLC} decreases with increasing load inductance since the inductive shielding effect increases. The gate delay is proportional to the effective capacitance seen at the driving point. Since the effective capacitance decreases for larger inductances, the gate delay decreases. The interconnect inductance shields part of the load capacitance, reducing the gate delay.

For a total load capacitance and resistance of 400 fF and 100 Ω, respectively, the impedance parameters of the π_{21} model are $R_\pi = 48\ \Omega$, $C_2 = 67$ fF, and $C_1 = 333$ fF [209]. As shown in [209, 210], L_π is linearly dependent on the load inductance. In order to characterize the effective capacitance for different load inductances, the ratio between the effective capacitance of an *RLC* model and an *RC* model is determined. The ratio between the effective capacitance of the π_{21} *RLC* and *RC* models for different load inductances is shown in Fig. 7.4. The effective capacitance decreases as the load inductance increases.

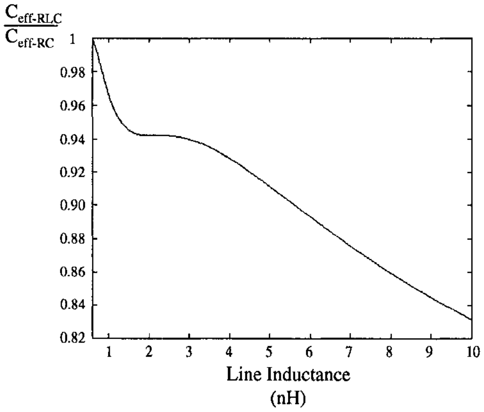


Figure 7.4: Ratio between the effective capacitance of an *RLC* and *RC* load

The shielding effect of the interconnect inductance increases the importance of including the line inductance in the delay analysis [211, 212]. Ignoring the inductance overestimates the circuit delay, requiring a larger buffer to drive the load. The effect of the interconnect inductance on the total signal propagation delay is discussed in section 7.3.

7.3 Effect of Line Inductance on the Delay Model

The effective capacitance can be used to characterize the gate delay. The signal propagation delay depends upon the active gate and passive interconnect components of the signal path. The gate delay is the time required to charge the capacitance seen through the equivalent resistance of the driver. The interconnect delay is the time required for the signal to propagate along the line. These two components cannot be separated as the driver and load represent a single system. The interconnect inductance reduces both the capacitance seen by the driver (as described in section 7.2) and the equivalent output resistance of the driver by increasing the period during which the driving transistors operate in saturation, reducing the overall gate delay.

For an ideal source driving a distributed *RLC* line, however, the signal delay is primarily due to the line delay. The line inductance increases the signal propagation delay. For an ideal source driving an *RLC* line, the line delay can be modeled as [61]

$$t_{pd-RLC} = \frac{e^{-2.9\zeta^{1.35}}}{\omega_n} + 0.74R_{line}(C_L + 0.5C_{line}), \tag{7.2}$$

where

$$\zeta = \frac{R_{line}\omega_n}{2}(0.5C_{line} + C_L),$$
$$\omega_n = \frac{1}{\sqrt{L_{line}(C_{line} + C_L)}},$$

C_L is the load capacitance driven by the line and R_{int}, C_{int}, and L_{int} are the total line resistance, capacitance, and inductance, respectively.

The line delay increases with the line inductance as described in Appendix D. As the line inductance increases, two competing effects change the total delay of the signal as shown in Fig. 7.1. The delay due to the active transistor decreases while the delay due to the passive interconnect increases.

To exemplify the effect of the line inductance on the propagation delay, a CMOS inverter driving a long inductive interconnect with $R_{line} = 50\ \Omega$ and $C_{line} = 400$ fF is considered. The total delay for different driver sizes based on a 0.24 μm CMOS technology is shown in Fig. 7.5. Different values of the line inductance with $C_L = 50$ fF are considered. Note the general similarity to Fig. 7.1.

The propagation delay decreases with increasing line inductance until a minimum delay is reached. The total delay decreases with higher line induc-

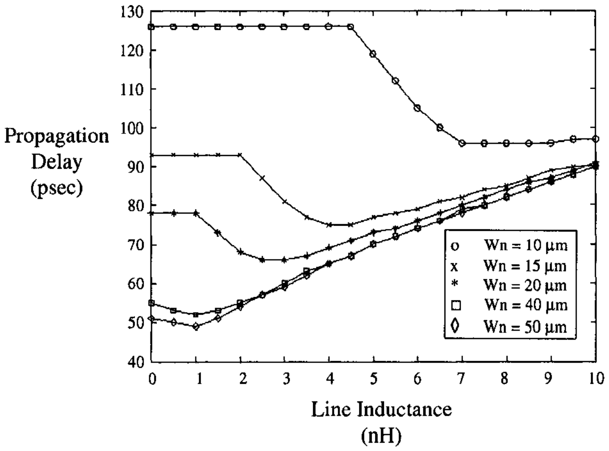


Figure 7.5: Total delay for different values of line inductance and driver size of a distributed *RLC* interconnect as determined by the Cadence circuit simulator

tance over a wide range of driver size (the NMOS transistor size W_n ranges from 10 μm to 50 μm). For small drivers (*i.e.*, $W_n < 5\,\mu$m), the line inductance has no effect on the propagation delay since the delay is dominated by the driver output resistance. For large drivers (*i.e.*, $W_n > 50\,\mu$m), the line inductance increases the delay. The output resistance of these drivers is small and the interconnect delay dominates the total delay. Large drivers are not preferred as the decrease in signal delay is not significant, while the required area and dissipated power are large. Furthermore, the input gate capacitance is greater with larger drivers, increasing the load and therefore the delay of the previous logic stage. Cascaded buffer tapering can be used for large drivers, but the power dissipation increases due to the additional inverters (cascaded tapered inverters [57]) employed to reduce the delay.

Curve fitting is used to determine the optimum value of the line inductance to achieve the minimum propagation delay. The minimum delay is determined over a wide range of line inductance (from 0.1 nH to 10 nH), load capacitance (from 10 fF to 250 fF), inverter size (from 5 μm to 50 μm), line capacitance (from 100 fF to 1 pF), and line resistance (from 25 Ω to 100 Ω). The minimum delay occurs when the ratio between the equivalent output resistance of the driver R_{tr} equals the magnitude of the lossy characteristic impedance of the line $|Z_{line}|$ or $Z_T = 1$,

$$Z_T = \frac{R_{tr}}{|Z_{line}|}, \tag{7.3}$$

$$R_{tr} = \frac{V_{dd}}{k_n(V_{dd} - V_{tn})^{\alpha}} + \frac{V_{dd}}{k_n\left[2(V_{dd} - V_{tn})V_{dd} - \frac{V_{dd}^2}{2}\right]}, \tag{7.4}$$

$$|Z_{line}| = \sqrt{\frac{\sqrt{{R_{line}}^2 + (\omega L_{line})^2}}{\omega C_{line}}}, \tag{7.5}$$

$$\omega = \frac{2\pi}{t_r}, \tag{7.6}$$

where V_{dd} is the supply voltage, k_n is the transconductance of the NMOS transistor of the driving inverter, V_{tn} is the threshold voltage of an NMOS transistor, $\alpha = 1.3$ and models the velocity saturation in a short-channel transistor, and t_r is the signal transition time at the output of the driving inverter. t_r is iteratively determined based on the concept of an effective capacitance.

The total propagation delay increases if the line inductance is less than the matched condition. Ignoring the line inductance overestimates the delay and the size of the driver. The line inductance is considered in section 7.6 in the design of an inverter driving a section of *RLC* interconnect. The savings in both power and area if line inductance is considered is noted.

Interconnect resistance also has a shielding effect on the gate delay. However, resistive shielding has a different effect on the total propagation delay. A comparison between the shielding effect of the interconnect resistance and inductance is described in section 7.4.

7.4 Inductive Shielding versus Resistive Shielding

The shielding effect, which reduces the effective capacitance seen by a driver, exists in both *RC* and *RLC* loads. The interconnect resistance and/or inductance impedes the propagation of the signal along the line, shielding part of the total line capacitance. The effective capacitance for both *RC* and *RLC* lines is less than the total line capacitance, reducing the gate delay. For *RC* interconnects, the line delay is linearly proportional to the line resistance. The increase in line delay overcomes the reduction in the gate delay. The total signal propagation delay increases with interconnect resistance as shown in Fig. 7.6. The propagation delay of a CMOS inverter driving a distributed *RLC* line with $L_{line} = 2$ nH is determined for the line parameters mentioned in section 7.3. Unlike the line inductance, the propagation delay increases with line resistance for different driver sizes.

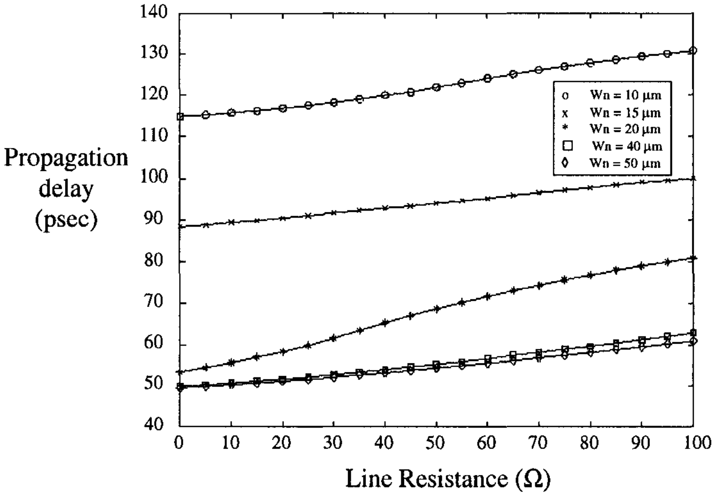


Figure 7.6: Total delay for different values of line resistance and driver size for a distributed *RLC* interconnect (Cadence circuit simulator)

For highly inductive lines, the line resistance does not significantly affect the signal propagation delay. The propagation delay is $\propto \sqrt{L_{line}C_{line}}$ in lossless lines. This limiting case provides intuition describing the sublinear dependence between the line delay and the line inductance. The line delay is sublinearly proportional to the line inductance in *RLC* lines. The reduction in gate delay, with an increase in line inductance, decreases the total propagation delay of the signal as described in section 7.3.

As technology advances, new materials are used to reduce the line resistance and therefore the signal delay. These lower resistive materials increase the importance of considering the line inductance. As interconnect resistance decreases, the interconnect inductance has a greater effect on the signal characteristics. As shown in Fig. 7.7, the propagation delay decreases as the line resistance decreases. The reduction in the propagation delay is shown for different values of line inductance. The propagation delay decreases more rapidly for those lines with a larger inductance. A greater reduction in propagation delay can be achieved if low resistive materials are used in highly inductive lines.

For an inductive load, more sophisticated models are required to capture the effects of the interconnect inductance on the signal characteristics. An analytic solution characterizing the signal propagation delay of an inverter

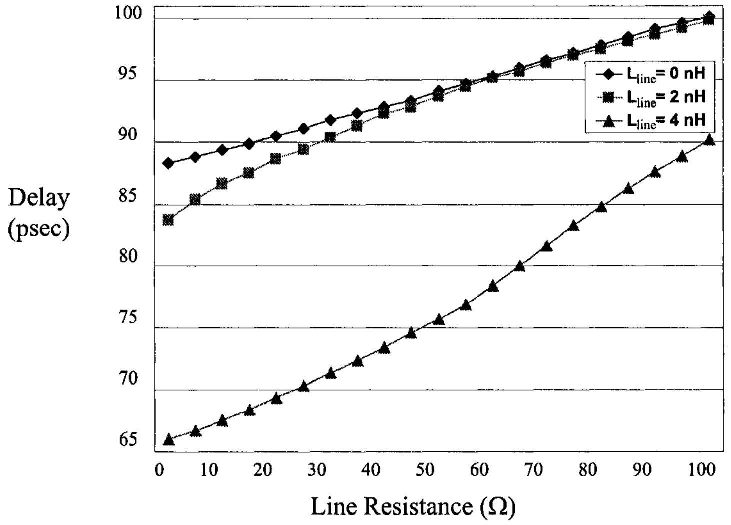


Figure 7.7: Total delay for different values of line resistance and inductance of a distributed *RLC* interconnect (Cadence circuit simulator)

driving a reduced order π_{21} model of a distributed *RLC* line is presented in section 7.5.

7.5 Propagation Delay of CMOS Inverter Driving an Inductive Load

Different models have been developed to determine the propagation delay of a CMOS gate (inverter) driving an *RLC* load. The propagation delay is used to refer to the total delay from the input of the gate to the load. Simple models are used in [61, 125] to simplify the circuit analysis process. A linear model for the driver transistor is not sufficiently accurate to characterize the propagation delay. The distributed model described in [61] is shown in Fig. 7.8a. This model replaces the driver of an *RLC* interconnect with an equivalent resistance. The accuracy of the model depends upon the accuracy of modeling the nonlinear element (inverter) with a constant resistance. The lumped model used to determine the delay expression in [125] is shown in Fig. 7.8b. This model suffers from inaccuracy since the shielding effect of the load inductance is not considered.

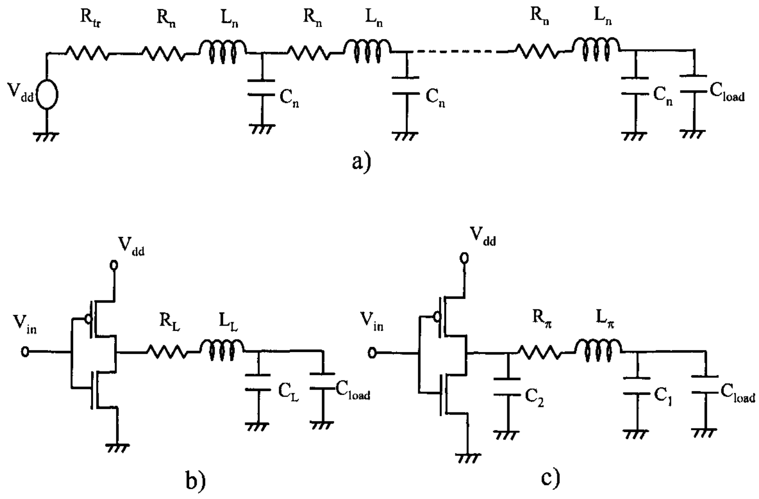


Figure 7.8: Interconnect and driver models a) distributed with constant source resistance [61] b) lumped with nonlinear transistor model [125] c) π_{21} with nonlinear transistor model

More accurate expressions to calculate the propagation delay of a CMOS inverter driving an *RLC* load based on the π_{21} model, which is shown in Fig. 7.8c, are provided in Appendix E. As described in section 7.2, the interconnect inductance reduces the effective capacitance seen by the driver, reducing the gate delay. Furthermore, the inductance decreases the effective resistance of the driving gate, further reducing the gate delay. The load inductance impedes the flow of the current to the interconnect load, delaying when the driving transistor enters the saturation region The reduction in the gate delay contributes to a reduction in the total propagation delay. A comparison between the three models for different load parameters is presented in section 7.6.

7.6 Simulation Results

Three different models are used to illustrate the importance of an accurate model to represent both the driver and the interconnect. In Tables 7.1 and 7.2, a comparison between the model described in [61], a lumped *RLC* model [125], and the π_{21} model (described in Appendix E) is listed. The π_{21} model achieves high accuracy, determining the delay with an average error of less than 9% for different line parameters.

The line inductance reduces the total signal propagation delay as discussed in previous sections of this chapter. Including the inductance in the interconnect model is important in the design of a line driver. Excluding the inductance overestimates the delay of the circuit and underestimates the current sourced by the driver. Including the line inductance can reduce the driver size, saving both area and power.

A 0.24 μm CMOS technology is used to demonstrate the effect of including the line inductance in the design of a line driver. An interconnect line with R_{line} = 10 Ω/mm, C_{line} = 105 fF/mm, and L_{line} = 650 pH/mm is assumed to determine the reduction in the size of the line driver if inductance is considered. A symmetric CMOS inverter is used to drive a line loaded by a capacitive load of 50 fF to achieve a target delay. The target delay and the driver size that achieves this delay are listed in Table 7.3. A reduction in power dissipation of 5% and in gate area of 13% is achieved if line inductance is considered. As technology advances, different dielectric and line materials will be used to reduce the interconnect delay. Low-κ dielectric materials and copper interconnect will reduce both the line capacitance and resistance, increasing the effect of inductance on the signal behavior. A 17% reduction in power dissipation and 29% reduction in gate area is demonstrated for a low-κ copper interconnect example circuit.

7.7 Conclusions

The shielding effect of interconnect inductance is introduced. The effective capacitance of an *RLC* load decreases with increasing line inductance, reducing the gate delay of a driver. Furthermore, the line inductance reduces the equivalent output resistance of a driver, reducing the total propagation delay. Resistive shielding, however, does not reduce the propagation delay since the increase in the line delay is typically greater than any reduction in the gate delay.

A parameter Z_T, the ratio between the output driver resistance and the magnitude of the lossy characteristic impedance of the line, is introduced to characterize the signal propagation delay of a CMOS inverter driving an *RLC* interconnect. The minimum propagation delay is achieved when $Z_T = 1$, where the driver is matched with the lossy characteristic impedance of the line.

The line inductance can significantly affect the resulting circuit performance. A smaller line driver can be used to drive an interconnect line if the line inductance is considered, more accurately achieving the target delay than if the line inductance is ignored. Furthermore, the per cent savings in both area and power dissipation is expected to increase as technology advances. A reduction of 17% in power dissipation and 29% in gate area is achieved for an example circuit.

An accurate model of the propagation delay of a CMOS inverter driving an *RLC* load is provided. An error of less than 9% as compared to dynamic circuit simulation is exhibited.

Table 7.1: Propagation delay with different models for different line inductance for $C_{line} = 400$ fF

$W_n = 20\ \mu\text{m}$, $R_{line} = 50\ \Omega$

L_{line}	$C_{line} = 400$ fF						
nH	Cadence	Ismail/Friedman [61]		Tang/Friedman [125]		π_{21}	
	(psec)	psec	Error	psec	Error	psec	Error
0.0	77	35.2	-54.2%	59.5	-22.7%	68.2	-11.3%
1.0	74	35.7	-51.7%	62.2	-15.8%	70.0	-5.4%
2.0	67	38.1	-43.0%	66.6	-0.5%	64.7	-3.4%
3.0	68	41.4	-39.0%	97.8	43.8%	63.3	-6.8%
4.0	70	45.0	-35.6%	101.8	45.5%	72.6	3.8%
5.0	73	48.6	-33.4%	105.2	44.1%	80.3	10.0%
Maximum		-54.27%		-45.95%		-11.35%	
Average		41.51%		30.75%		6.11%	

Table 7.2: Propagation delay with different models for different line inductance for $C_{line} = 1$ pF

$W_n = 20\ \mu\text{m}$, $R_{line} = 50\ \Omega$

L_{line}	$C_{line} = 1$ pF						
nH	Cadence	Ismail/Friedman [61]		Tang/Friedman [125]		π_{21}	
	(psec)	psec	Error	psec	Error	psec	Error
0.0	148	86.3	-41.6%	97.8	-33.8%	130.1	-12.0%
1.0	147	86.4	-41.2%	93.3	-36.5%	129.6	-11.7%
2.0	153	87.0	-43.0%	86.5	-43.4%	131.5	-14.0%
3.0	145	88.7	-38.7%	81.1	-44.0%	134.2	-7.3%
4.0	132	91.1	-30.9%	76.6	-41.9%	122.5	-7.1%
5.0	118	94.0	-20.2%	96.8	-17.8%	117.1	-0.7%
Maximum		-43.00%		-45.64%		-14.00%	
Average		36.23%		38.69%		8.91%	

Table 7.3: Reduction in area and power dissipation when considering line inductance for different dielectric and line materials

Dielectric Material	Resistivity	Target Delay	W_n		Per cent reduction in Power dissipation	Per cent reduction in Area
			RC	*RLC*		
SiO_2	Aluminum	100	19	16.5	5%	13%
	Copper	100	17.8	15.2	6%	15%
Low-K	Aluminum	60	23	19	9%	17%
	Copper	60	21	15	17%	29%

Chapter 8

Optimum Wire Shape of an *RLC* Interconnect

8.1 Introduction

With the decreased feature size of CMOS circuits, on-chip interconnect now dominates both circuit delay and power dissipation. Interconnect design has become a dominant issue in high speed integrated circuits (ICs). The interconnect width is a primary design choice in the interconnect design process. Many algorithms have been proposed to determine the optimum wire size that minimizes a cost function such as delay. As shown in [66, 67], the optimum interconnect shape which minimizes the signal propagation delay in an *RC* interconnect is an exponential function. Different extensions to this work have been applied to consider other circuit parameters such as fringing capacitance [68]-[83].

Wire tapering increases the interconnect width at the near end (the driver end) of the line as shown in Fig. 9.1. Wire tapering is usually applied to long lines, increasing the importance of including the line inductance [20, 199] in the optimization process of tapered lines. No previous work has been published (to the authors' best knowledge) that describes the optimum wire shape to minimize the propagation delay of an *RLC* line. Previous work in tapered *RLC* lines [72] uses the optimum shape for *RC* lines without demonstrating that the shape is optimum for *RLC* lines. Furthermore, an analytic solution to determine the optimum tapering factor has not been presented. Moreover, additional issues such as the efficiency of wire tapering over other techniques to drive long interconnect lines and the power dissipation of tapered interconnect have not been considered in *RLC* lines.

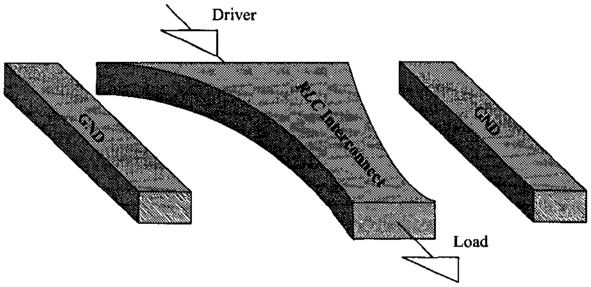


Figure 8.1: Coplanar tapered *RLC* interconnect

The research described in [60] shows that wire tapering improves signal speed by only 3.5% as compared to uniform wire sizing if an optimum repeater system is used to minimize the propagation delay of an *RC* line. Uniform wire sizing is an efficient technique to improve circuit performance [44]. As compared to tapered sizing, uniform wire sizing is also easier to implement if a repeater system is available. The inductance, however, has not been considered in the line model described in [60]. Furthermore, for practical reasons, a repeater system is not always possible. Moreover, repeater insertion increases the power dissipation due to the additional capacitance of the repeaters. It is shown in this chapter that, for minimum signal propagation delay, exponential wire tapering is the optimum shape for an *RLC* interconnect. An analytic expression to determine the optimum tapering factor for minimum propagation delay is also provided. Tapering *RLC* lines is compared with other performance enhancement techniques in this chapter. As described here, tapering *RLC* lines can achieve a greater reduction in delay as compared to tapered *RC* lines. Whenever possible, uniform repeater insertion is used as an efficient technique to reduce the signal propagation delay [56]. Also described in this chapter, wire tapering not only outperforms uniform wire sizing but also outperforms uniform (optimum) repeater insertion. For *RLC* lines, exponential tapering achieves the lowest propagation delay as compared to uniform wire sizing with or without repeaters.

Not only propagation delay but also the power dissipation characteristics are affected by wire sizing. As described in [143]-[145], wire sizing for *RLC* interconnects can decrease the total power dissipated by a circuit. Wire tapering as a wire sizing technique is shown to reduce power dissipation as well as the propagation delay [214].

In addition to the reduced propagation delay and power dissipation with tapered lines, tapered *RLC* interconnects may exhibit enhanced signal integrity, reducing the inductive noise. Noise reduction has become an important issue in the design of modern integrated circuits. Particularly for *RLC* interconnects, noise can cause signal degradation and even cause a circuit to malfunction. The line inductance may also produce overshoots and undershoots in the signal waveform, increasing the noise in the circuit. This issue of signal integrity in tapered lines is further discussed in the chapter.

The chapter is organized as follows. In section 8.2, the optimum wire shape that produces the minimum signal propagation delay of an *RLC* line is characterized. Different constraints on interconnect tapering are discussed in section 8.3. In section 8.4, a comparison between tapered *RC* and *RLC* lines is described. Wire tapering is presented in section 8.5 as an option to minimize the transient power dissipation of a circuit. In section 8.6, line tapering is compared with uniform repeater insertion. Signal integrity in tapered RLC networks is discussed in section 8.7. Some simulation results are presented in section 8.8. In section 8.9, some conclusions are provided.

8.2 Optimum Wire Shape for Minimum Propagation Delay

The signal propagation delay of a distributed RLC interconnect is described in [61, 36]. Two time constants characterize the signal speed and behavior in long interconnects, the resistive-capacitive (RC) time constant and the inductive-capacitive (LC) time constant (or the time of flight through the line $t_f = \sqrt{L_{int}C_{int}}$), where C_{int} and L_{int} are the line capacitance and inductance, respectively). For highly resistive (less inductive) lines, an RC delay model is sufficient to characterize the signal delay. The optimum tapering relation for these lines is an exponential tapering factor [66, 67]. If the inductive behavior of the line dominates the resistive behavior, the time-of-flight can dictate the time for the signal to propagate through the line [159]. The optimum shape that minimizes the propagation delay of an LC line is the shape function that minimizes the time-of-flight.

The line inductance and capacitance per unit length, respectively, can be expressed in terms of the line width by the following simple relationships,

$$L_{int}(W) = \frac{L_0}{W(x)}, \tag{8.1}$$

$$C_{int}(W) = C_0 W(x) + C_f, \tag{8.2}$$

where L_0 is the line inductance per square, C_f is the fringing capacitance per unit length, and C_0 is the line capacitance per unit area. $W(x)$ is the line width as a function of x, the distance from the load as shown in Fig. 8.2.

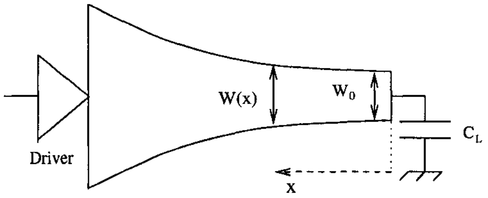


Figure 8.2: *RLC* line tapered by a general width tapering function $W(x)$

The time-of-flight for the signal is

$$t_f = \sqrt{\int_0^l \frac{L_0}{W(x)} \int_0^x (C_0 W(y) + C_f) dy dx}, \tag{8.3}$$

where l is the line length. If functions F and $u(x)$ are defined as

$$\begin{aligned} F &\equiv \frac{L_0}{W(x)} \int_0^x (C_0 W(y) + C_f) dy, \\ u(x) &\equiv \int_0^x W(y) dy, \end{aligned}$$

respectively, and Euler's differential equation is used to minimize (8.3), as similarly described in [66], the optimum $u(x)$ should satisfy the differential equation,

$$u'(x) = \frac{2L_0C_0}{c}u(x) + \frac{2C_fL_0l}{c}. \tag{8.4}$$

Thus,

$$W(x) = W_0\, e^{\frac{2L_0C_0}{c}x}, \tag{8.5}$$

where $c = \frac{2C_fL_0l}{W_0}$. W_0 is obtained by substituting (8.5) into (8.3) and differentiating (8.3) with respect to W_0. Setting the result to zero produces a nonlinear equation which can be solved numerically.

As shown in (8.5), the optimum tapering function of the width of an *LC* line is an exponential function. For either an *RC* or *LC* line, the general form of the optimum shaping function that minimizes the propagation delay is an exponential function. The *RC* and *LC* models are the two limiting cases of a general *RLC* interconnect. The optimum tapering function of an *RLC* line must satisfy the general exponential form $W(x) = qe^{px}$, where q is the line width at the load end and p is the tapering factor. The optimum value of q and p for an *RLC* line reduces to an *RC* line [66, 67] if the line inductance is negligible and to an *LC* line [with $q = W_0$ and $p = \frac{2L_0C_0}{c}$ in (8.5)] if the line resistance is negligible. The optimum value of q and p for an RLC line is between these two limits.

As described in [199, 211], for an RLC line, the signal propagation delay is minimum when the line is matched with the driver. The matched condition, from [211], is

$$R_{tr} = \left| Z_{line}(q,p) \right|, \tag{8.6}$$

which can be used to determine the optimum tapering function. $Z_{line}(q,p)$ is the lossy characteristic impedance of a line, where

$$|Z_{line}(q,p)| = \sqrt{\frac{\sqrt{R_{line}(q,p)^2 + (\omega L_{line}(q,p))^2}}{\omega C_{line}(q,p)}}, \tag{8.7}$$

$$\omega = \frac{2\pi}{3t_r}, \tag{8.8}$$

and R_{tr} is the equivalent output resistance of the driver. $R_{line}(q,p)$, $L_{line}(q,p)$, and $C_{line}(q,p)$ are the line resistance, inductance, and capacitance as functions of q and p, respectively. t_r is the signal transition time at the near end of the line which is determined from the reduced order model described in [211].

As there is one equation, (8.6), and two unknowns, q and p, there are two degrees of freedom in designing an optimum RLC line tapered for minimum delay. For a width q, there is an optimum tapering factor p_{opt} which satisfies (8.6) and at which the propagation delay is minimum. Other design constraints, such as the minimum and maximum line width and the power dissipation, are discussed in section 8.3 to determine a more power efficient solution.

8.3 Constraints on Optimum Tapering for *RLC* Lines

Tapering an interconnect assigns a smaller width for the line at the far end. The line width is greater at the near end, as shown in Fig. 8.2. As discussed in section 8.2, the width increases exponentially to produce the minimum propagation delay. By choosing q and solving (8.6) as a nonlinear equation in one unknown, the optimum tapering factor p_{opt} can be determined. There are two practical limits for choosing q,

1. $q \geq W_{min}$, where W_{min} is the minimum wire width of a target technology.
2. $q \leq W_{max}e^{-pl}$, where W_{max} is the maximum wire width of a target technology.

These two constraints should be satisfied when designing a tapered line. q cannot be smaller than the minimum wire width allowed by the technology. Alternatively, increasing q may result in a width at the near end (the largest width of the line) which may be greater than the maximum available wire width.

Another important design constraint is the power dissipation. Wire sizing affects the two primary transient power components, the dynamic power dissipated in charging and discharging the line capacitance and the short-circuit power dissipated within the load gate. The short-circuit power is minimum when the line is matched with the driver [142, 145], which is also the optimum solution for minimum delay.

The dynamic power is linearly proportional to the line capacitance. To decrease the line capacitance, the line width should be as narrow as possible, as the line capacitance increases superlinearly with the width [140]. In order to satisfy both high speed and low power design objectives, q should be chosen equal to W_{min}. The optimum value for the tapering factor p_{opt} is obtained by solving (8.6) for $q = W_{min}$. Optimum wire tapering is compared in section 8.4 with uniform wire sizing for both *RC* and *RLC* lines.

8.4 Tapering versus Uniform Wire Sizing in *RC* and *RLC* Lines

Interconnect tapering is more efficient in *RLC* lines than in *RC* lines. Two effects reduce the signal propagation delay of an exponentially tapered *RLC* line. The first effect is the shape of the line structure which minimizes both the *RC* and *LC* time constants.

The second effect is an increase in the inductive behavior of the line. Tapering an interconnect line decreases the line resistance, reducing the attenuation along the line. This effect increases the inductive behavior of the line. The inductive behavior of the line can be characterized by $\zeta = \frac{R_{line}}{2}\sqrt{\frac{C_{line}}{L_{line}}}$, the damping factor of a line [20]. As described in [20], when $\zeta < 1.0$, the inductive behavior of a line cannot be ignored. As shown in Fig. 8.3, the damping factor decreases (for different line thickness T and length l) as the line tapering factor increases, making the line behave more inductively. For $\zeta > 1.0$ (the dotted lines), the damping factor does not consider the inductive behavior of the line since the line is underdamped. The inductive effect of a line where $\zeta > 1.0$ is negligible.

The line inductance shields part of the line capacitance and decreases the equivalent output resistance of the gate that drives the line. The signal propagation delay decreases as the inductive behavior of the line becomes more pronounced [211]. This effect makes line tapering more attractive in long *RLC* lines.

Another criterion to optimize the interconnect width for minimum propagation delay is uniform wire sizing. A minimum width coplanar interconnect line is illustrated in Fig. 8.4 for two sizing criteria, uniform sizing and exponential tapering.

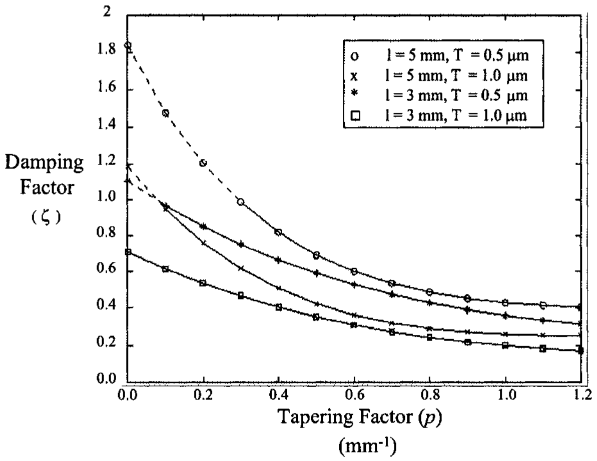


Figure 8.3: Interconnect damping factor as a function of the tapering factor for different line parameters

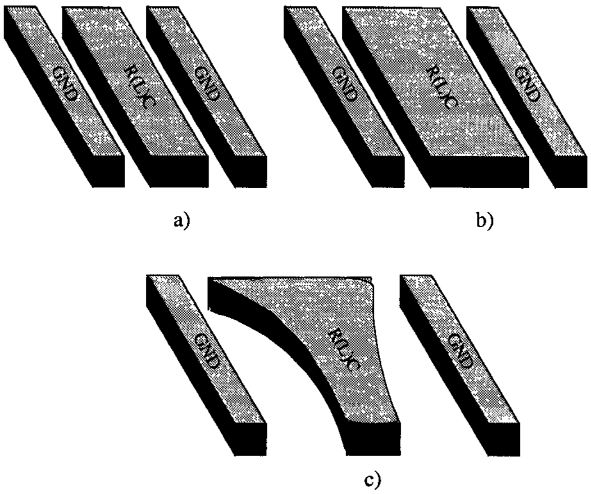

GND
R(L)C
GND
a)
GND
R(L)C
GND
b)
GND
R(L)C
GND
c)

Figure 8.4: Coplanar interconnect a) minimum width b) uniform sizing c) exponential tapering

A uniform wire size is composed of a constant interconnect width along the line length. Exponential wire tapering outperforms uniform wire sizing as discussed in section 8.2. As with wire tapering, uniform wire sizing can decrease the line resistance, making the inductive behavior greater; however, the superlinear increase in the line capacitance limits the effect of the line inductance on reducing the signal propagation delay. Wire tapering, however, produces a smaller delay than the delay achieved from uniform wire sizing. Optimum wire tapering produces a greater delay reduction in *RLC* lines than in *RC* lines since the delay is further reduced due to the inductive behavior of the line as described in [211]. The line inductance makes tapering more efficient than uniform wire sizing in *RLC* lines.

For an *RLC* line, tapering not only reduces the propagation delay, but also decreases the total power dissipation as compared to uniform wire sizing. An increase in the inductive behavior of the line reduces the signal transition time at the load, reducing the short-circuit current and, consequently, the total transient power dissipation [142, 129]. Simulation results are presented in section 8.8.1 that illustrate the efficiency of exponential wire tapering on both the propagation delay and power dissipation of *RLC* lines. Exponential tapering is shown in section 8.5 to minimize the total transient power dissipation of a circuit.

8.5 Interconnect Tapering for Minimum Power Dissipation

Wire sizing for *RLC* interconnects can decrease the total power dissipation of a circuit since the power dissipated in the load can be traded off with the power dissipated by the driver [142]-[146]. Uniform wire sizing decreases the transition time at the load, reducing the short-circuit power of the load gate. Tapered wire sizing, also, reduces the attenuation along the interconnect line, decreasing the signal transition time at the load. A tradeoff, therefore, exists between the short-circuit power of the load gate and the dynamic power of the driver in long tapered interconnect.

The power components of an inverter driving a load of two inverters through a long interconnect is shown in Fig. 9.3. As the tapering factor increases, the power dissipation in the load gates (inverters) decreases. The signal transition time becomes smaller, decreasing the short-circuit power of the load gates. The power dissipated by the driver increases, since the interconnect line capacitance is larger, increasing the dynamic power dissipated to charge the line capacitance. An optimum tapering factor, therefore, exists for minimum total transient power dissipation.

The work described in [145] provides an analytic solution for the optimum interconnect width for minimum power dissipation. The uniform interconnect

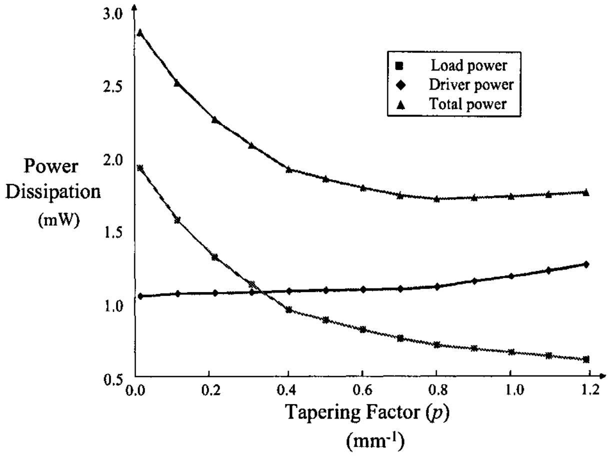


Figure 8.5: Power dissipation in a load driven by a long tapered interconnect line

width W_{int} is replaced with an exponential function qe^{px}. A minimum interconnect width at the load end $q = W_{min}$ is assumed. The optimum tapering factor rather than the optimum width is determined from

$$\frac{dP_t}{dp} = fV_{dd}^2\frac{dC_{line}}{dp} + \frac{NfG}{0.8}\left(\frac{dt_{10\%}}{dp} - \frac{dt_{90\%}}{dp}\right) = 0, \tag{8.9}$$

where G is a function of V_{dd}, threshold voltage V_t, transconductance K of the load gate, and capacitive load C_L. f is the operating frequency, N is the number of driven gates, P_t is the total power dissipation, $t_{10\%}$ and $t_{90\%}$ are the times at which the voltage at the load end reaches 10% and 90%, respectively, $\frac{dt_{10\%}}{dp}$ and $\frac{dt_{90\%}}{dp}$ are described in [145], and $\frac{dC_{line}}{dp}$ is obtained from the capacitance expression described in Appendix F. The analytic solution to optimize a tapered interconnect line for minimum transient power dissipation is exemplified in section 8.8.2. In section 8.6, the performance of interconnect tapering is compared with uniform repeater insertion.

8.6 Interconnect Tapering versus Repeater Insertion

No repeaters are assumed to be placed along the interconnect line described in section 8.4. Practical reasons may restrict the use of repeaters along the interconnect. If practically possible, however, repeater insertion can improve the circuit performance in *RC* lines. Repeater insertion is an efficient technique to reduce propagation delay for long *RC* interconnects [58]. Uniform repeater insertion techniques divide the interconnect line into equal sections and employ equal size repeaters to drive each section [56, 58]. As compared to repeater insertion with uniform wire sizing, wire tapering improves the speed of an *RC* line by at most 3.5% as described in [60]. Unlike tapered *RC* lines, tapering *RLC* lines can achieve a greater reduction in the propagation delay as compared to uniform repeater insertion. As described in [137], wire sizing is more efficient than repeater insertion in *RLC* lines. In *RLC* interconnects, wire sizing decreases the number of repeaters required to achieve the minimum propagation delay. The propagation delay of wide *RLC* interconnect lines with no repeaters is less than the propagation delay of thin lines driven by an optimum repeater system [137]. Uniform and tapered sizing of *RLC* interconnects are two wire sizing techniques which outperform repeater insertion. Exponential wire tapering is more efficient than uniform wire sizing as presented in section 8.4. Among the three criteria, exponential wire tapering achieves the minimum propagation delay, since the optimum interconnect shape is exponential and, in general, wire sizing outperforms repeater insertion in *RLC* lines. Some simulation results are presented in section 8.8.3 that compare wire tapering with repeater insertion. In section 8.7, an additional advantage of wire tapering in *RLC* interconnects is presented.

8.7 Signal Integrity in Tapered *RLC* Interconnects

Signal integrity is an important design issue in integrated circuits. Particularly for inductive interconnects, the impedance mismatch may cause reflections at both the driver output and the load. The impedance mismatch between the driver and the load in digital circuits may distort the signal, causing overshoots and undershoots in the signal waveform. Tapered interconnect lines can enhance signal integrity as compared to uniformly sized lines. Line tapering reduces the magnitude of the reflections, since the line resistance is higher at the load end. The line resistance dominates the line impedance at the load, reducing the inductive noise of the signal propagating along the line. Moreover, exponential tapering reduces the inductive noise, since the impedance mismatch is distributed along the line and not concentrated at the load.

As described in section 8.2, exponential tapering produces a smaller propagation delay as compared to uniform wire sizing. In some interconnect networks (such as clock distribution networks), the delay can be increased to enhance the signal integrity. Line tapering can achieve the same signal characteristics (propagation delay and transition time) of a uniform line while reducing ringing in the interconnect network. An efficient technique for tapering the interconnect lines of a clock distribution network while maintaining the same signal characteristics is described in [215]. This technique is used to demonstrate the efficiency of interconnect tapering to improve signal integrity.

The difference between the first overshoot and undershoot $\Delta V_{over-under}$ at the driving point of an interconnect network is treated as a metric to characterize the reflections (the ringing effect). An example clock distribution network is considered in section 8.8.4 to demonstrate the improvements in signal integrity achieved when tapered interconnect lines are considered.

8.8 Simulation Results

In order to determine the optimum tapering factor, the line impedance parameters (R_{line}, L_{line}, and C_{line}) are expressed in terms of the design parameters q and p. Closed form expressions for the line parameters are provided in Appendix F.

A 0.24 μm CMOS technology is used to demonstrate the efficiency of tapering an RLC line. A 5 mm long interconnect line with $T = 0.5\,\mu$m, $W_{min} = 0.5\,\mu$m, $W_{max} = 20\,\mu$m, and $S_{min} = 1.0\,\mu$m is considered as an example. A long interconnect driven by a CMOS inverter is modeled by twenty RLC sections. The line is shielded by two $1.0\,\mu$m wide ground lines, and loaded with N CMOS inverters. In subsection 8.8.1, tapered wire sizing is compared with uniform wire sizing. In subsection 8.8.2, the interconnect line is tapered for minimum power dissipation. A comparison between wire tapering and repeater insertion is presented in subsection 8.8.3. An example clock distribution network is used in subsection 8.8.4 to demonstrate signal integrity in an interconnect network.

8.8.1 Tapering versus Uniform Wire Sizing

As listed in Table 8.1, the effect of tapering on three different circuits is evaluated. W_n and W_{nl} are the width of the NMOS transistor of the driving and load inverters, respectively. t_{r-In} is the transition time of the signal at the input of the driving inverter. As described in section 8.3, q is chosen to minimize the power dissipation based on the minimum line width W_{min}. The width of each section and the corresponding line impedance parameters are described in Appendix F.

Table 8.1: Circuit parameters of example circuits

	W_n (μm)	W_{nl} (μm)	t_{r-In} (psec)	q (μm)	p (m^{-1})
Circuit1	15	5	50	0.5	550
Circuit2	20	1	50	0.5	600
Circuit3	15	15	20	1.0	400

The minimum delay is determined for both uniform wire sizing and exponential line tapering. As shown in Fig. 8.6, wire tapering outperforms uniform wire sizing for all of the circuits. The reduction in the minimum delay is greater for an *RLC* line as compared to an *RC* line, making tapering more efficient in *RLC* lines. A 15% reduction in delay for an *RLC* line as compared to a reduction of 7% for an *RC* line is achieved when optimum tapering is used rather than uniform wire sizing.

In addition to a smaller propagation delay, the total transient power dissipation is lower. A tapered line with q equal to the minimum width reduces the total line capacitance, thereby decreasing the dynamic power (as compared to uniform wire sizing). Furthermore, the power dissipation is further decreased in an RLC line since the short-circuit power is lower. The reduction in power dissipation for several RC and RLC lines is shown in Fig. 8.7. A reduction in power dissipation of as much as 16% for an RLC line as compared to 11% for an RC line is achieved when optimum tapering is used rather than uniform wire sizing.

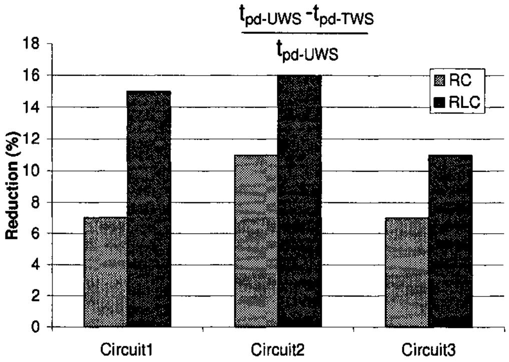


Figure 8.6: Reduction in propagation delay. UWS stands for Uniform Wire Sizing and TWS stands for Tapered Wire Sizing.

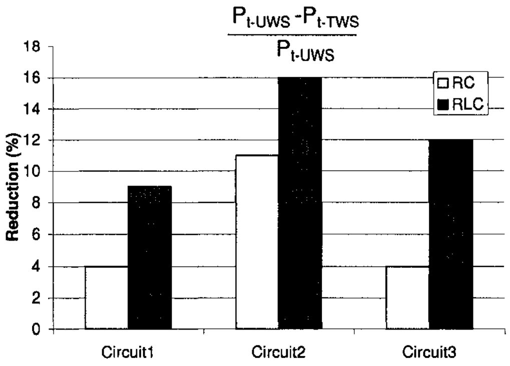


Figure 8.7: Reduction in total power dissipation

8.8.2 Tapering for Minimum Power Dissipation

In section 8.8.1, the optimum wire tapering for minimum signal propagation delay is determined for several example circuits. As described in section 8.5, line tapering can be used to minimize the power dissipation of a circuit. The analytic solution presented in section 8.5 is applied to determine the optimum tapering factor for minimum power dissipation. For $W_n = 25$ μm, $W_{nl} = 15$ μm, and $W_{min} = 0.1$ μm, the optimum tapering factor is listed in Table 9.2. A different number N of load inverters is considered to determine the total power dissipation of the circuit. The total power dissipation for $N = 1$, 2, and 5 is shown in Fig. 9.5.

As the number of loads increases, the reduction in power dissipation in-

Table 8.2: Optimum tapering for minimum power dissipation

	Optimum tapering for minimum power $p_{opt-Power}$ (mm^{-1})	
Number of Loads N	Analytic	Simulation
1	0.76	0.75
2	0.83	0.85
5	0.94	1.20

creases with tapered interconnect lines. A higher per cent of the power is dissipated in the load gates (inverters), decreasing the overall power dissipation.

The optimum tapering factor for minimum power dissipation is determined by the analytic expression and simulation as listed in Table 9.2. For the tapering factor determined analytically and by simulation, the total power dissipated by the circuit described in section 8.8.1 for a different number of loads is listed in Table 8.3. The per cent reduction in power for each tapering factor rather than a uniform (minimum) interconnect width is also listed. The analytic solution is shown to be highly accurate in determining the optimum

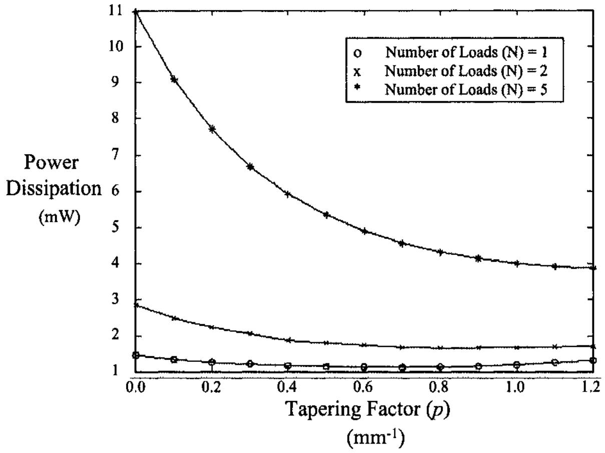


Figure 8.8: Power dissipation for different number of loads driven by a long tapered interconnect line

tapering factor for minimum power. The difference between the reduction in power using the analytic solution and simulation is less than 2%.

Tapering is more efficient in reducing the total power dissipation as the number of load gates increases (greater power is dissipated in the loads). For a large number of loads (*e.g.*, $N = 5$), a significant reduction in power dissipation of around 65% is achieved.

8.8.3 Tapering versus Repeater Insertion

In order to verify the efficiency of wire tapering as compared to inserting repeaters in RLC interconnects, the propagation delay of a uniform repeater system is determined. The optimum number of repeaters is determined for two values of interconnect widths, $q = 0.5\ \mu m$ and $q = 1.0\ \mu m$ [61]. The optimum tapering factor is obtained for different driver sizes based on the matched condition, (8.6). Equally sized repeaters divide the line into sections of equal lengths. For $q = 1.0\ \mu m$, the propagation delay at the end of a uniform line driven by repeaters is listed in the second column of Table 8.4. For $q = 1.0\ \mu m$, one repeater in the middle of the interconnect line is the optimum solution to drive the interconnect [61]. As listed in the table, for all values of the driver (repeater) size, line tapering outperforms repeater insertion. Replacing a repeater system with an optimally tapered line decreases the overall signal propagation delay. A reduction in delay of up to 24% is achieved using an optimally tapered line.

The minimum permissible interconnect width decreases with advancing technology (assumed in this chapter to be 0.5 μm). For $q = 0.5\ \mu m$, two repeaters are required to achieve the minimum propagation delay using optimum repeater insertion. The propagation delay of this system is listed in Table 8.5.

As the interconnect width decreases, more repeaters are required to drive the more resistive interconnect. Tapering the line, however, achieves a smaller propagation delay as compared to inserting repeaters. The per cent reduction in the propagation delay increases with decreasing line width. With advances in technology, interconnect tapering will become more effective since a greater reduction in the propagation delay will be achieved.

8.8.4 Signal Integrity Characteristics in an Example Clock Distribution Network

An example clock distribution network is used to demonstrate the improvement in signal integrity as wire tapering is applied to size the clock lines. Wide interconnect lines are usually used in clock distribution networks to improve the signal characteristics (propagation delay and signal transition time). A clock distribution network with 64 sinks covering a die area of 3.5 X 3.5 mm is modeled as a distributed *RLC* network. A symmetric capacitive load is assumed at all of the sinks (no clock skew among the sinks). The delay is determined at the sinks of the network for minimum width interconnect lines ($q = 0.5$ μm). The signal waveform at three points; the input and output waveform of the driver of the tree and the sinks (or load) are shown in Fig. 8.9a. For minimum interconnect width, the line inductance has a negligible effect on the signal waveform.

Uniform interconnect sizing is used to minimize the propagation delay and transition time. For wide lines, the interconnect inductance affects the signal waveform. Overshoots and undershoots appear in the signal waveform as shown in Fig. 8.9b.

Wire tapering can be used to achieve the same signal characteristics while reducing the inductive noise [215]. The propagation delay and the difference between the first overshoot and undershoot $\Delta V_{over-under}$ are listed in Table 8.6 for the three example circuits.

As shown in Fig. 8.9c, the difference between the overshoots and undershoots $\Delta V_{over-under}$ decreases from 793 mV to 524 mV at the source of the tree when tapered lines are used. Tapering the interconnects achieves a reduction in $\Delta V_{over-under}$ of approximately 34%, reducing the inductive noise, thereby improving the signal integrity.

8.9 Conclusions

The optimum wire shape that produces the minimum signal propagation delay in an *RLC* line is determined in this chapter. It is shown that an exponentially tapered interconnect minimizes the time of flight of an *LC* line. The general form of the optimum shaping function for an *RLC* line is qe^{px}. The optimum tapering factor p which achieves the minimum delay while lowering the power is determined for different driver and load characteristics.

Optimum wire tapering as compared to uniform wire sizing is more efficient in *RLC* lines than in *RC* lines. The line inductance makes tapering more attractive in *RLC* lines since tapering produces a greater reduction in delay as compared to uniform wire sizing. A reduction in delay of 15% for an *RLC* line as compared to 7% for an *RC* line is achieved when optimum tapering is applied rather than uniform wire sizing.

With a minimum wire width at the far end of the line and an optimum tapering factor, both the propagation delay and power dissipation are reduced. Greater line inductance increases the savings in power in an optimally tapered line as compared to uniform wire sizing. A reduction in power dissipation of 16% for an *RLC* line as compared to 11% for an *RC* line is achieved when optimum tapering is applied rather than uniform wire sizing. Summarizing, tapering improves both the speed and power characteristics of an *RLC* line.

An analytic solution for the tapering factor that produces the minimum transient power exhibits an error of less than 2% as compared to dynamic circuit simulation. The reduction in power increases as the number of driven gates increases. A reduction in the total power dissipation of about 65% is achieved when tapering for minimum power is used rather than uniform sizing with minimum line width.

Tapered wire sizing outperforms both uniform wire sizing and uniform repeater insertion. A reduction in the propagation delay of about 36% is achieved for an example circuit when optimum tapering is used rather than uniform repeater insertion. Wire tapering as compared to repeater insertion becomes more efficient as technology advances, since the reduction in the delay of tapered lines increases.

Wire tapering can improve signal integrity by reducing the inductive noise. Tapered interconnect lines in clock distribution networks can achieve the same signal characteristics of uniformly sized lines, while reducing the reflections along the line. The difference between the signal overshoots in an example clock distribution network decreases by 34% when tapered interconnect is used rather than uniform interconnect that produces the same signal delay and transition time.

Table 8.3: Total power dissipation using different sizing techniques

Number of Loads	No tapering ($p = 0$)	Optimum tapering ($p_{opt-Power}$)			
N	(mW)	Analytic (mW)	Reduction (%)	Simulation (mW)	Reduction (%)
1	1.47	1.129	22.94%	1.128	23.00%
2	2.86	1.658	41.98%	1.654	42.12%
5	10.96	4.092	62.66%	3.876	64.64%

Table 8.4: Propagation delay for a long interconnect (5 mm) with $q = 1.0$ μm

Driver (Repeater) Size (μm)	Propagation Delay (psec)		
	Uniform Repeater Insertion	Optimum Line Tapering	Reduction (%)
10	279	229	18%
15	227	179	21%
20	199	151	24%
25	182	141	23%

Table 8.5: Propagation delay for a long interconnect (5 mm) with $q = 0.5$ μm

Driver (Repeater) Size (μm)	Propagation Delay (psec)		
	Uniform Repeater Insertion	Optimum Line Tapering	Reduction (%)
10	325	227	30%
15	278	181	35%
20	255	163	36%
25	244	181	26%

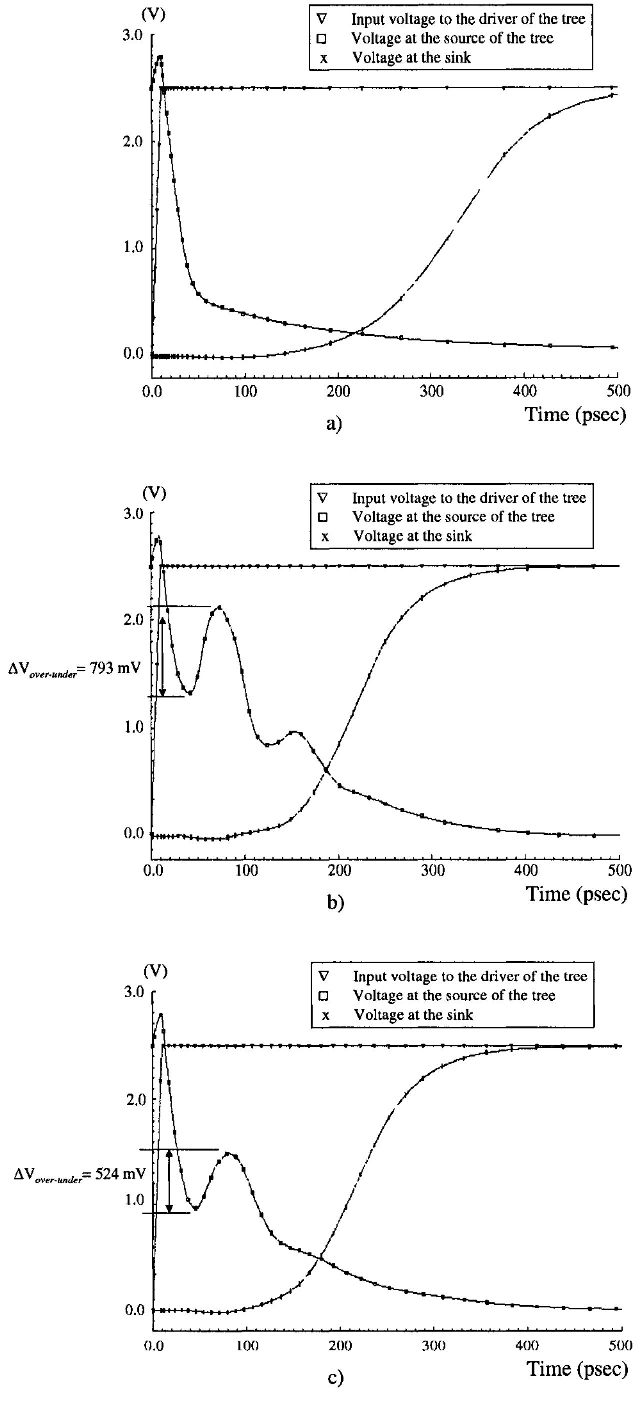


Figure 8.9: Waveforms at different nodes within the tree using a) minimum width lines b) uniformly sized lines c) tapered lines

Table 8.6: Propagation delay and $\Delta V_{over-under}$ for different interconnect sizing techniques

		Minimum width	Uniform wire sizing	Tapered wire sizing
Propagation delay	(psec)	325	216	215
$\Delta V_{over-under}$	(mV)	0	793	524
	Reduction (%)	0	0	34%

Chapter 9

Optimum Wire Tapering for Minimum Power Dissipation of *RLC* Interconnects

9.1 Introduction

Interconnect design has become a dominant issue in high speed integrated circuits (ICs). As the feature size of CMOS circuits decreases, the on-chip interconnect now dominates both the circuit delay and power dissipation characteristics of high complexity integrated circuits. Wire sizing has been proposed as a technique to improve circuit performance [144]. Exponential wire tapering is an efficient technique to decrease signal propagation delay in *RC* interconnects [66, 68]. Wire tapering increases the interconnect width at the driver end of the line as shown in Fig. 9.1.

The inductive behavior of the interconnect can no longer be neglected, particularly in long interconnect lines operating at high frequencies. Wire tapering is usually applied to long lines, further increasing the importance of including line inductance in the optimization process. In [214], exponential tapering is shown to be the optimum shape function to minimize propagation delay in *RLC* lines.

Wire sizing can also affect the power dissipated by a circuit [129]. Uniform wire sizing decreases the transition time at the load, reducing the short-circuit power of the load gate [129]. Uniform wire sizing for *RLC* interconnects can decrease the total power dissipation of a circuit since the power dissipated in the load can be traded off with the power dissipated by the driver [142]-[146]. As described in [142]-[146], the width of an *RLC* interconnect can be optimized for minimum power dissipation.

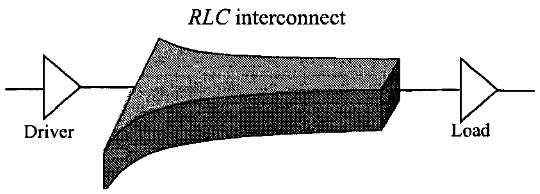


Figure 9.1: Coplanar tapered *RLC* interconnect

In this chapter, *RLC* wire tapering is shown to reduce the power dissipated by a circuit. An analytic expression to determine the optimum tapering structure that produces the minimum transient power dissipation is provided.

Moreover, the efficiency of wire tapering over uniform wire sizing in reducing the power dissipation is considered.

The chapter is organized as follows. In section 9.2, wire tapering as a criterion to minimize transient power dissipation is presented. An analytic solution to determine the optimum wire shape that produces the minimum power dissipation of an *RLC* line is characterized in section 9.3. In section 9.4, optimum wire tapering is compared with optimum uniform wire sizing for minimum power dissipation. Some simulation results are presented in section 9.5. In section 9.6, some conclusions are provided.

9.2 Interconnect Tapering for Minimum Power Dissipation

Tapering an interconnect line can decrease the signal transition time at the load, decreasing the short-circuit power of the load gate. As described in [142]-[146], the reduction in line resistance (with increasing wire width) decreases the signal attenuation along the line, improving the signal transition time. The same criterion can be used to reduce the power dissipation of a load driven by a tapered interconnect line.

Exponential tapering produces the optimum shape to minimize the propagation delay in *RLC* interconnects [214]. Exponential tapering can also be used as a sizing technique to decrease the power dissipation. For the circuit shown in Fig. 9.1, a long (5 mm) interconnect line is used to connect the load (a CMOS inverter) with the driver (a CMOS inverter). The interconnect width is exponentially tapered based on the tapering function $W(x) = qe^{px}$, where $W(x)$ is the line width at a distance x from the load, q is the initial line width at the load, and p is the tapering factor. The signal transition time at the input of the load as a function of the tapering factor p is shown in Fig. 9.2. As shown in the figure, the signal transition time decreases as the tapering factor p increases. The line becomes less resistive (more inductive) with tapering, reducing the transition time at the load.

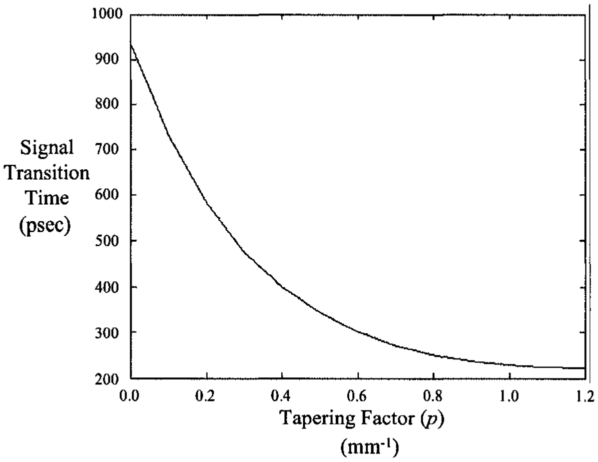


Figure 9.2: Signal transition time at the input of a load driven by a long tapered interconnect line

For $q = 0.1$ μm and 0.2 μm, the power components of the circuit structure shown in Fig. 9.1 are illustrated in Fig. 9.3. For increasing tapering factor, the short-circuit power dissipated in the load gate deceases. The power dissipated by the driver increases, since the line capacitance is greater with tapering. A tradeoff, therefore, exists between the short-circuit power dissipated in the load and the dynamic power of the driver in long tapered interconnects. For high values of p, the increase in the driver power is greater than the reduction in the load power. An optimum tapering factor that produces the minimum total transient power dissipation exists in a tapered RLC interconnect. For each value of q, there is an optimum tapering factor p_{opt} at which the total transient power dissipation is minimum.

As q increases, the dynamic power dissipated by the driver increases, changing the optimum tapering factor that produces the minimum power. An optimum initial width q_{opt} exists that produces the minimum power dissipation. q_{opt} and p_{opt} should be determined simultaneously. In section 9.3, an analytic solution that can be used to determine the optimum tapering structure for minimum power is described.

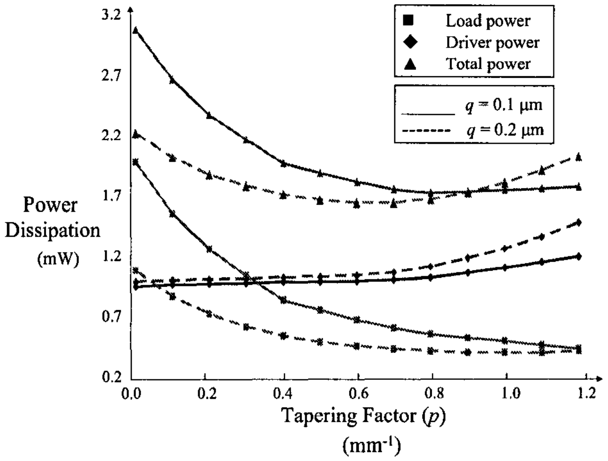


Figure 9.3: Power dissipation in a load driven by a long tapered *RLC* interconnect line

9.3 Optimization Criterion for a Tapered Line

The work described in [144] provides an analytic solution for the optimum uniform interconnect width that produces the minimum power dissipation. The total transient power dissipation is presented in terms of the uniform interconnect width W_{int}. The uniform width is replaced here with an exponential function qe^{px}. For an inverter driving N gates, as shown in Fig. 9.4, the total transient power dissipation $P_t(q,p)$ is a function of the initial line width q and tapering factor p,

$$P_t(q, p) = P_{Driver}(q, p) + N\, P_{Load}(q, p) + P_c, \tag{9.1}$$

where P_c is the summation of the dynamic power of the load gate and the short-circuit power of the driver and $P_{Driver}(q, p)$ and $P_{Load}(q, p)$ are the dynamic power of the driver and the short-circuit power of the load, respectively. P_c is a weak function of q and p. P_c is therefore assumed constant, since the dynamic power of the load gate depends upon the load characteristics and the short-circuit power of the driver depends primarily upon the signal transition time at the input of the driver.

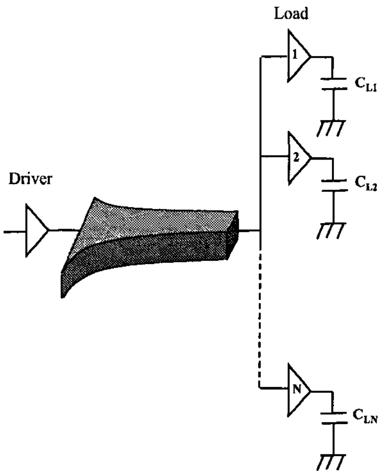


Figure 9.4: Coplanar tapered *RLC* interconnect

To achieve the minimum transient power dissipation, the initial wire size and tapering factor are simultaneously determined. Differentiating (9.1) with respect to q and p and equating each expression to zero, two nonlinear equations in q and p are

$$\frac{\partial P_t}{\partial p} = fV_{dd}^2 \frac{\partial C_{line}}{\partial p} + \frac{NfG}{0.8} \left(\frac{\partial t_{10\%}}{\partial p} - \frac{\partial t_{90\%}}{\partial p} \right) = 0, \tag{9.2}$$

$$\frac{\partial P_t}{\partial q} = fV_{dd}^2 \frac{\partial C_{line}}{\partial q} + \frac{NfG}{0.8} \left(\frac{\partial t_{10\%}}{\partial q} - \frac{\partial t_{90\%}}{\partial q} \right) = 0, \tag{9.3}$$

where G is a function of V_{dd}, threshold voltage V_t, transconductance K of the load gate, and capacitive load C_L [144], f is the operating frequency, N is the number of driven gates, $t_{10\%}$ and $t_{90\%}$ are the times at which the voltage at the load end reaches 10% and 90% of the final voltage, respectively, $\frac{\partial t_{10\%}}{\partial p}$ and $\frac{\partial t_{90\%}}{\partial p}$ are described in [144], and $\frac{\partial C_{line}}{\partial p}$ is obtained from the capacitance expression described in [214]. The two nonlinear equations in q and p can be solved numerically. In section 9.4, tapered wire sizing is compared with uniform wire sizing to decrease the total power dissipation of a circuit. The optimum solution is determined for an example circuit and compared with simulations in section 9.5.

9.4 Tapering versus Uniform Wire Sizing for Minimum Power Dissipation

Uniform and tapered wire sizing can be used to minimize the power dissipation of a circuit. As compared to uniform wire sizing, tapered wire sizing can achieve enhanced signal characteristics with a lower total interconnect capacitance. As described in [215], for the same signal characteristics (signal propagation delay and transition time), the capacitance of a tapered interconnect line is smaller than the capacitance of a uniformly sized line, since the coupling component of the line capacitance is less. The reduction in line capacitance reduces both the short-circuit power of the load gate and the dynamic power of the driver, reducing the total power dissipation as compared to uniform sizing. The total power dissipation of an optimally tapered *RLC* interconnect for minimum power is less than the total power dissipation of a uniformly sized interconnect designed for minimum power. A comparison of the power components for both tapered and uniform wire sizing is presented for an example circuit in section 9.5.

9.5 Simulation Results

In order to determine the optimum tapering factor, the line resistance R_{line}, inductance L_{line}, and capacitance C_{line} are expressed in terms of q and p. Closed form expressions for the line impedance parameters are provided in [214]. Since precise tapering is difficult, the interconnect line is divided into sections. The width of each line section is determined according to the initial width and tapering factor. Twenty *RLC* line sections are used to model the interconnect assuming the line is shielded with two 1.0 μm wide ground lines [216]. A fixed width for each section with an exponential increase in the section width towards the driver is used, permitting the impedance parameters of each section to be determined.

A 0.18 μm CMOS technology is used to demonstrate the efficiency of tapering an *RLC* line. A 5 mm long interconnect line with a line thickness $T = 0.5\,\mu$m, minimum width $W_{min} = 0.1\,\mu$m, maximum width $W_{max} = 20\,\mu$m, and minimum spacing between the line and ground shield $S_{min} = 1.0\,\mu$m is considered. CMOS inverters are used as the driver and loads. In subsection 9.5.1, the analytic solution is used to determine the optimum tapering structure to minimize the power dissipation. Tapered wire sizing is compared with uniform wire sizing in subsection 9.5.2.

9.5.1 Tapering for Minimum Power Dissipation

The analytic solution presented in section 9.3 is used to determine the optimum tapering factor for minimum power dissipation. The total power dissipation is determined assuming $W_n = 20\ \mu m$, where W_n is the width of the NMOS transistor of the driver (for a symmetric CMOS inverter) and $W_{nl} = 10\ \mu m$, where W_{nl} is the width of the NMOS transistor of the load inverter. The total power for $q = 0.1\ \mu m$ and $N = 1$, 2, and 5 is shown in Fig. 9.5. The total power dissipation decreases as the interconnect line is tapered until the minimum power is achieved. The total power dissipation has a local minimum for each initial width q, which can be obtained by determining p_{opt} using (9.2). A tradeoff among the power components of the circuit exists in choosing the initial width q.

The optimum tapering structure described by p_{opt} and q_{opt} is determined by simultaneously solving (9.2) and (9.3). The optimum solution of the tapered structure and a uniformly sized line is listed in Table 9.1. In section 9.5.1, wire tapering is compared with uniform sizing as criteria to minimize the total transient power dissipation.

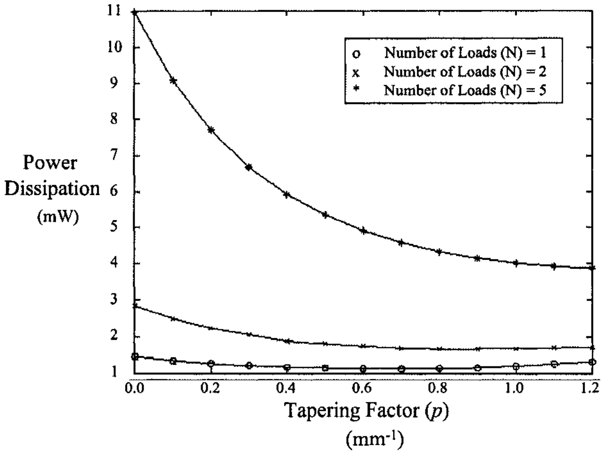


Figure 9.5: Power dissipation for different number of loads driven by a long tapered interconnect line

9.5.2 Tapering versus Uniform Wire Sizing

The total power dissipation is determined for different sizing criteria to evaluate the tapering criteria presented in section 9.5.1. The power dissipation for the minimum interconnect width is listed in the second column of Table 9.2 for different number of loads. The power dissipation along with the per cent reduction using different interconnect sizing techniques are listed in the table.

The optimum initial interconnect width q_{opt} and tapering factor p_{opt} are used to size the interconnect section of a long interconnect line. The total

Table 9.1: Optimum sizing for minimum power dissipation

Number of loads (N)	Uniform sizing	Tapered sizing	
	W_{opt} (μm)	q_{opt} (μm)	p_{opt} (mm^{-1})
1	0.8	0.3	0.45
2	1.2	0.7	0.38
5	2.1	1.2	0.34

power dissipated by the circuit is listed with the per cent reduction in power as compared to using the minimum interconnect width. Alternatively, circuit simulation is used to determine the optimum solution for minimum power. The power dissipation using both an analytic solution and simulation is listed in the final four columns. As listed in the table, the difference in the amount of power dissipation and per cent reduction in power is negligible ($< 2\%$). The analytic solution achieves high accuracy in determining the optimum tapering solution for minimum power dissipation.

As the number of loads increases, the reduction in power dissipation increases when tapering the interconnect line. A higher per cent of the power is dissipated in the load gates (inverters), increasing the efficiency of line tapering as a technique to decrease power dissipation. For a large number of loads (*e.g.*, $N = 5$), a significant reduction in power dissipation of around 72% is achieved.

In the third and fourth columns of Table 9.1, the minimum power obtained using uniform wire sizing is listed with the per cent reduction in power. A greater reduction in power dissipation is achieved when an optimally tapered interconnect line is used rather than a uniformly sized interconnect. A reduction in power dissipation of 24% is achieved when optimum wire tapering is used as compared to a 17% reduction when uniform sizing is applied.

In Fig. 9.6, different power components are shown using the optimum solution for both uniform and tapered lines. The power dissipated by the driver, one of the loads, and the total power is shown in Figs. 9.6a, 9.6b, and 9.6c, respectively. As described in section 9.4, both power components decrease, since an optimally tapered line has a lower total line capacitance. The transient power dissipation is decreased by about 8% if optimum wire tapering is used rather than uniform wire sizing.

9.6 Conclusions

Interconnect tapering is shown in this chapter to minimize the transient power dissipation. Wire tapering reduces the power dissipated by the load gate and increases the power dissipated by the driver. A tradeoff, therefore, exists in a tapered line between the power dissipated in the load and the driver. An analytic solution for the power dissipation with an error of less than 2% is provided to determine the optimum initial wire width and tapering factor for a tapered interconnect structure. The reduction in power becomes greater as the number of driven gates increases. A reduction in total power dissipation of about 72% is achieved when optimal tapering for minimum power is used rather than uniform sizing with minimum line width.

Optimum tapering for minimum power dissipation is more efficient than uniform wire sizing. Tapering lowers the interconnect capacitance, reducing both transient power components (dynamic and short-circuit). A 24% reduction in power dissipation is achieved when optimum tapering is applied rather than a reduction of 17% with uniform wire sizing. For an example circuit, as compared to uniform wire sizing, optimum wire tapering can reduce the power dissipation by 8%.

Table 9.2: Optimum tapering for minimum power dissipation

Power dissipation (μW)							
Number of loads	Minimum width	Uniform sizing		Tapered sizing			
N			Reduction	Analytic	Reduction	Simulation	Reduction
1	1.4	1.2	17.4%	1.1	22.5%	1.0	23.7%
2	2.8	1.7	41.5%	1.6	44.0%	1.5	45.6%
5	11.0	3.3	69.7%	3.2	71.0%	3.1	71.5%

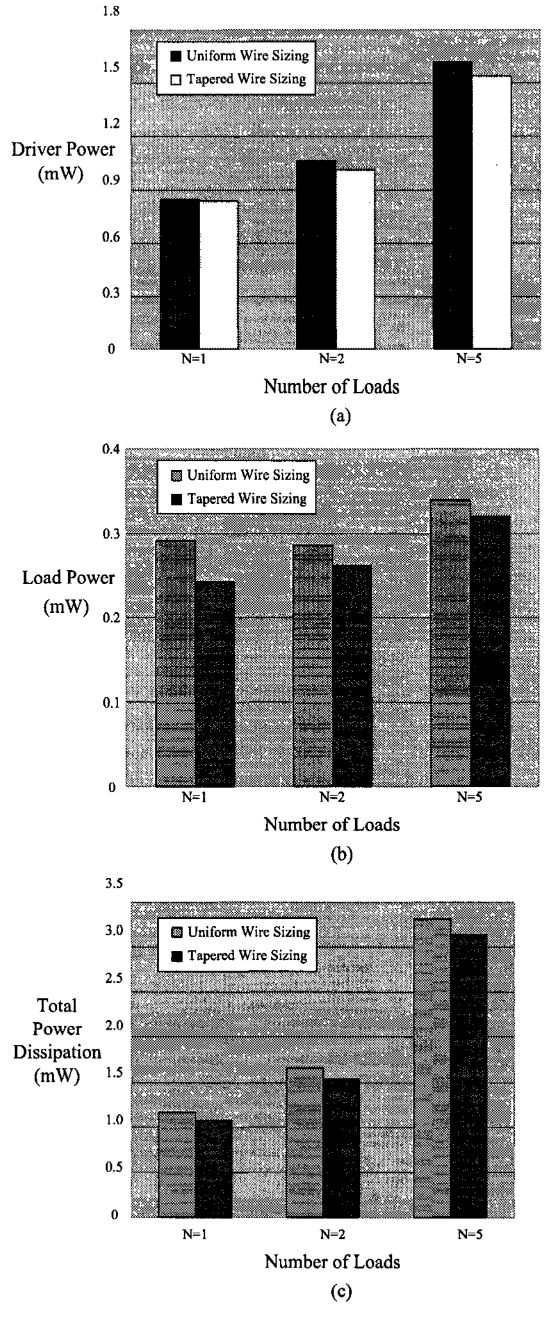


Figure 9.6: Power components for different number of loads using optimum tapered and uniform wire sizing a) driver power b) load power c) total power

Chapter 10

Exponentially Tapered H-Tree Clock Distribution Networks

10.1 Introduction

With the decrease in feature size of CMOS integrated circuits (IC), interconnect design has become a primary issue in high speed ICs. Interconnect design is most often used to increase circuit speed [44]-[60], however, the interconnect also affects the power dissipated by a circuit [214]. The dynamic power dissipated in charging the interconnect capacitance represents a large portion of the total transient power dissipation. Clock networks can dissipate a large portion of the total power dissipated within a synchronous IC, ranging from 25% to as high as 70% [132]. Some work has been published that considers power dissipation in the interconnect design process [48, 129],[142]-[146]. Interconnect shaping has been previously introduced as an efficient technique to improve circuit performance [66, 67]. In this chapter, interconnect shaping is proposed as a technique to reduce the power dissipated by a clock distribution network as well as the inductive noise. An interconnect shaping technique is proposed to reduce the power dissipated by an H-tree structured clock distribution network without degrading the signal characteristics.

H-tree clock distribution networks are widely used [216]-[230]. For global clock networks, H-trees are highly efficient in reducing clock skew [229]. The line widths within a standard H-tree are typically divided by two at the branch points to reduce reflections [231]. This technique matches the impedance at the branch points to eliminate signal reflections, reducing ringing in the signal. A matched impedance improves the signal integrity, reducing the inductive noise. The proposed criterion does not maintain a tapering factor of two in sizing the interconnects in H-trees. Rather, exponentially tapered interconnects, as shown in Fig. 10.1, are proposed.

With increasing signal frequencies and a corresponding decrease in signal transition times, the interconnect impedance can behave inductively [20]. Clock distribution networks, particularly H-trees, are routed on the top metal layers, using wide interconnect lines. These lines can have considerable inductance [20], requiring a shielding technique to eliminate the inductive noise. A variety of shielding techniques have been proposed to reduce the inductive

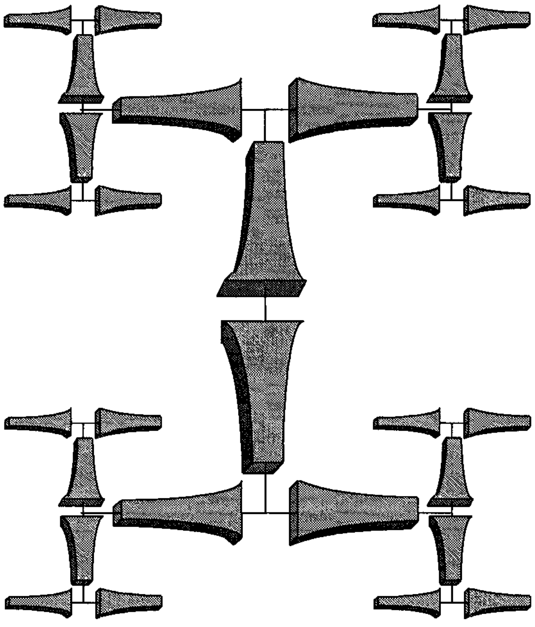


Figure 10.1: Exponentially tapered H-tree interconnect structure

behavior of the interconnects within a clock distribution network [232]-[235]. Shielding clock lines with two adjacent ground lines is a widely used technique [232, 178].

The proposed design methodology not only decreases the transient power dissipation but also reduces the inductive noise of the interconnects. Fewer reflections occur at the branch points, improving the signal integrity.

The chapter is organized as follows. In section 10.2, a criterion for tapering an H-tree network is presented. Different issues that affect the proposed technique are discussed in section 10.3. In section 10.4, simulation results are presented. Some conclusions are provided in section 10.5.

10.2 Tapering an H-Tree for Low Power

Exponential tapering has been shown to be the optimum shape function to produce the minimum signal propagation delay in *RLC* lines [214]. A tapered line, shown in Fig. 10.2a, can achieve the same signal characteristics (signal delay and transition time) as the uniform line shown in Fig. 10.2b with a smaller total line capacitance. Tapering a line reduces the coupling capacitance between the signal line and the adjacent ground lines, and, consequently, the total capacitance of the signal line. Although the line capacitance is reduced, the line resistance is greater, thereby maintaining approximately the same signal characteristics. A reduction in the line capacitance decreases the dynamic power while an increase in the line resistance decreases the inductive behavior of the interconnect. In section 10.2.1, a criterion is presented for tapering the interconnects of an H-tree clock distribution network based on a first order moment approximation of the transfer function characterizing the clock tree. A second moment approximation is used in section 10.2.2 to taper the interconnects of a clock distribution network while considering the interconnect inductance.

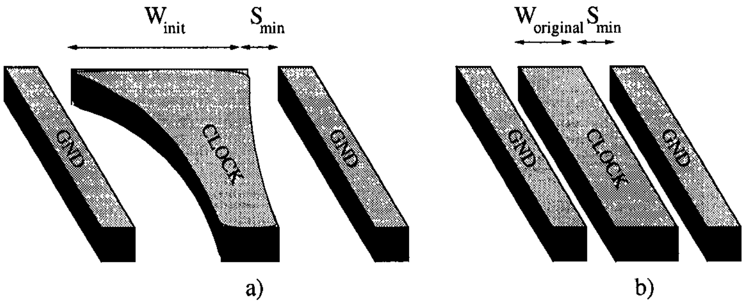


Figure 10.2: Coplanar clock line a) exponential tapering b) uniform (no tapering)

10.2.1 Tapering using First Order Moment Approximation

An exponentially tapered *RLC* interconnect line is described in Appendix G. Due to practical limitations, the line is divided into equal length sections. A first order approximation of the transfer function of each line section is used to characterize the signal. As described in section 10.3, the line becomes less inductive with tapering, since the line resistance increases. A first order approximation is adequate to characterize the time constant of each line section at relatively low frequencies. Additional savings in power can be achieved if a higher order approximation is used as described in section 10.2.2. If the *RC* time constants are maintained the same in both techniques (exponential and uniform), the signal characteristics (propagation delay and transition time) remain the same. The same signal characteristics are maintained with exponential tapering. The summation of the RC time constants of an exponentially tapered line along each branch of an H-tree is maintained equal to or less than the summation of the RC time constants of a uniformly sized line.

The optimum tapering structure for minimum power satisfies

$$\sum_{i=1}^{N} R_{i-T}C_{i-T} \leq \sum_{i=1}^{N} R_{i-U}C_{i-U}, \tag{10.1}$$

and consequently, achieves the minimum line capacitance, where R_{i-T} and R_{i-U} are the resistance of each section in a tapered and uniform line, respectively, C_{i-T} and C_{i-U} are the capacitance of each section in a tapered and uniform line, respectively, and N is the number of sections in each branch.

Two design parameters are used to size the interconnect within the tree; the initial width W_{init} and the tapering factor p. A practical implementation for exponential tapering is considered in Appendix G. For the technology dependent precision of the wire width ΔW, different values of W_{init} and p can satisfy (10.1). Two practical constraints limit the choice of the initial line width W_{init} and the optimum tapering factor p for each branch level. These practical limits can be represented by

1. $W_{init} \leq W_{max}$, where W_{max} is the maximum wire width of a target technology.

2. $p \leq \frac{N}{l(N-1)} ln(\frac{W_{init}}{W_{min}})$, where W_{min} is the minimum wire width of a target technology and l is the length of the line segment.

These two constraints should be satisfied for a tapered line segment. W_{init} cannot be greater than the maximum wire width permitted by the technology. Alternatively, increasing p may result in the width of the far end of a line being smaller than the minimum available wire width. W_{init} and p are chosen to satisfy (10.1) and any practical constraints while simultaneously minimizing the total line capacitance. A C program is used to determine the optimum tapering structure. Pseudocode for the C program is provided in Appendix H. In section 10.2.2, the line inductance is considered in the optimization process.

10.2.2 Tapering using Second Order Moment Approximation

In section 10.2.1, a first order approximation, the *RC* time constant, is used to determine the optimum tapering structure (initial width W_{init} and tapering factor p) for each segment of an H-tree. Reductions in power dissipation without any degradation in the signal characteristics are achieved using the first moment approximation as described in section 10.4.1 [215]. Interconnect lines within H-tree clock distribution networks are often wide and long, exhibiting considerable line inductance, particularly at high frequencies. The optimum tapering structure can therefore be more accurately determined if line inductance is considered.

An approximation of the second moment of the transfer function of a signal propagating through an *RLC* line is used in [154] to estimate the delay of an *RLC* tree. The approximation of the second moment m_2 of an *RLC* line [154] is equivalent to the approximation of the first moment m_1, the *RC* time constant, of an *RC* line. The approximate second moment of the transfer function is used to maintain the signal characteristics of a tapered line width. The line is divided into a number of sections as described in Appendix G. The second moment of the transfer function at the end of a line section is

$$m_2{}^i = \left(\sum_k C_k R_{ik}\right)^2 - \sum_k C_k L_{ik}, \tag{10.2}$$

where C_k is the capacitance of each line section, R_{ik} is the summation of the resistance of all of the line sections from the begining of the line to the target section, and L_{ik} is the summation of the inductance of all of the line sections from the begining of the line to the target section.

Equivalent to the Elmore delay, the second moment m_{2-U-L_n} is determined at the end of the line segment. For a uniform line segment in branch level L_n, the second moment is

$$\begin{aligned} m_{2-U-L_n} &= \sum_{i=1}^{N_{L_n}} \left(R_{i-U-L_n} \left(\sum_{k=1}^{i} C_{k-U-L_n} + C_{L-L_n} \right) \right)^2 \\ &- L_{i-U-L_n} \left(\sum_{k=1}^{i} C_{k-U-L_n} + C_{L-L_n} \right), \end{aligned} \tag{10.3}$$

where N_{L_n} and C_{L-L_n} are the number of sections and the load capacitance of line segment L_n, C_{k-U-L_n} is the capacitance of section k of a uniform line segment, and R_{i-U-L_n} and L_{i-U-L_n} are the resistance and inductance of section i of a uniform line segment, respectively.

The second moment approximation of a tapered line is

$$\begin{aligned} m_{2-T-L_n} &= \sum_{i=1}^{N_{L_n}} \left(R_{i-T-L_n} \left(\sum_{k=1}^{i} C_{k-T-L_n} + C_{L-L_n} \right) \right)^2 \\ &- L_{i-T-L_n} \left(\sum_{k=1}^{i} C_{k-T-L_n} + C_{L-L_n} \right), \end{aligned} \tag{10.4}$$

where C_{k-T-L_n} is the capacitance of section k of a tapered line segment and R_{i-T-L_n} and L_{i-T-L_n} are the resistance and inductance of section i of a tapered line segment, respectively. The second moment for all possible tapering structures (all possible initial widths W_{init} and tapering factor p as described in Appendix G) is compared with the moments of a uniform line. The optimum tapering structure is that structure which satisfies (10.5) and has the minimum total line capacitance,

$$m_{2-T-L_n} \leq m_{2-U-L_n}. \tag{10.5}$$

In order to simplify the process of determining the optimum tapering structure, a hierarchical technique is applied. The optimum tapering structure of each branch level of a tree is determined separately. Given the load capacitance at the leaf of an H-tree, the optimum tapering structure for the last segment (at the last branch level L_M or the leaf of the tree) is determined, where M is the number of branch levels. The total capacitance for that segment is used to determine the optimum structure for the higher branch level L_{M-1}. This process is repeated until the optimum tapering structure for the first level (the root of the tree) is obtained.

Practical constraints on the maximum and minimum line width, which are presented in section 10.2.1, are used to determine the optimum structure based on the second moment approximation. The pseudocode for the C program is provided in Appendix I. Additional considerations in the design of a tapered clock tree are discussed in section 10.3.

10.3 Design Issues in Exponentially Tapered H-Trees

Different issues that affect the design of an H-tree structured clock network are discussed in this section. In section 10.3.1, the effect of tapering on the signal characteristics of an H-tree is described. The area overhead of the interconnect network of an exponentially tapered tree is discussed in section 10.3.2. The proposed structure is also compared in this section with a uniform structure with the same area overhead. In section 10.3.3, skew reduction in an exponentially tapered H-tree network is discussed.

10.3.1 Signal Integrity

The line width of an interconnect within an H-tree is typically divided by two in a uniformly tapered tree to match the line impedance at the branch points, as shown in Fig. 10.3a. In a uniformly tapered tree, the interconnect inductance often cannot be ignored, particularly at the source of the tree where the line is widest. Matching the impedance reduces reflections and improves signal integrity [229], decreasing the inductive noise. This characteristic is not maintained in exponential tapering.

The branches of a tree are numbered according to the number of branch

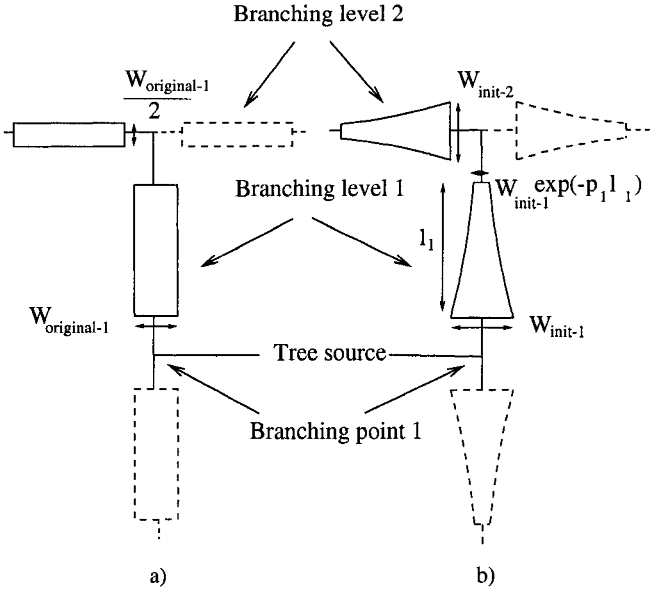

Branching level 2
$W_{original-1}$ / 2
W_{init-2}
Branching level 1
$W_{init-1}\exp(-p_1 l_1)$
l_1
$W_{original-1}$
W_{init-1}
Tree source
Branching point 1
a)
b)

Figure 10.3: Interconnect in an H-tree a) uniform tapering b) exponential tapering

points (see Fig. 10.3). As shown in Fig. 10.3b, the initial width of the interconnect at each branch level W_{init-L_n} is chosen based on the constraints described in section 10.2. The tapering factor of each branch level p_{L_n} is determined by satisfying (10.1) for the first order approximation and (10.5) for the second order approximation. All of the interconnects in the tree belonging to the same branch level have the same p_{L_n} and W_{init-L_n}.

With the criterion proposed in this chapter, the impedance mismatch does not affect the signal integrity of the lines since the interconnect resistance is greater. If a simple RC line model is considered, in order to reduce the line capacitance (to reduce the dynamic power) while the RC time constant is maintained the same, the line resistance is increased, reducing the effect of the interconnect inductance on the signal waveform. Furthermore, this technique reduces the reflections at the branch point, reducing the inductive noise. The line resistance dominates the line impedance at the branch points, reducing the inductive noise along the line. Moreover, exponential tapering reduces the inductive noise, since the impedance mismatch is distributed along the line and not concentrated at the branch points. Alternatively, an increase in the line resistance does not affect the signal characteristics as the line capacitance decreases. Tapering also reduces the resistance at the source of the interconnect branch since the width is greater. A reduction in resistance at the source of the line compensates the signal degradation that occurs due to the increase in the line resistance at the far end of the line. Moreover, the total capacitance of each tapered line segment is less than the capacitance of a uniform segment, reducing the load capacitance at each branch level.

The inductive behavior of the line can be characterized by the line damping factor $\zeta = \frac{R_{line}}{2}\sqrt{\frac{C_{line}}{L_{line}}}$ [20], where R_{line}, C_{line}, and L_{line} are, respectively, the line resistance, capacitance, and inductance. The inductive behavior decreases as the damping factor increases, reducing the importance of matching the line impedance at the branch points. A mismatch at the branch points does not increase the reflections as illustrated in the simulation results presented in section 10.4. The difference between the first overshoot and undershoot $\Delta V_{over-under}$ at the driving point of the tree is treated as a metric characterizing the reflections in the tree, as shown in Fig. 10.4. The area overhead of the proposed technique is discussed in section 10.3.2.

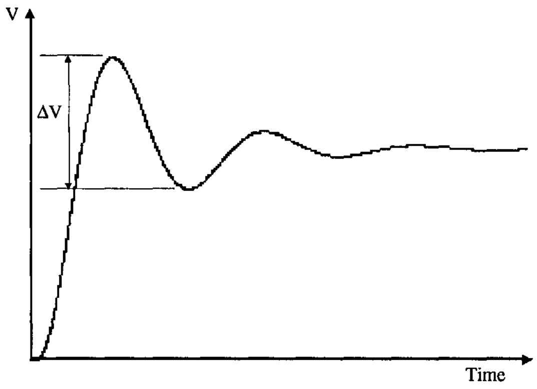


Figure 10.4: Difference between first overshoot and undershoot for an inductive interconnect

10.3.2 Routing Area

In the proposed H-tree structure, the interconnects comprising the clock network are assumed to be shielded by two ground lines. Coplanar shielded structures are commonly used in industry, particularly in clock networks, to reduce the interconnect coupling to adjacent lines and to minimize delay uncertainty of the clock signal [100], [232]-[235]. In the proposed structure, the interconnect width at the near end is larger, reducing the space between the signal (or clock) line and the ground shield. The space is assumed to be minimum in the uniform structure shown in Fig. 10.2b. In order to maintain the space between the signal and ground shield, the distance between the ground lines S_{large} is increased by the same amount as the increase in the initial width W_{init}, as shown in Fig. 10.5,

$$S_{large} = \frac{W_{init} - W_{original}}{2} + S_{min}. \tag{10.6}$$

For wider spacing between the signal and ground shield, the interconnect area is greater.

For the same area overhead, the line capacitance is reduced by increasing the space between the shield lines without changing the signal (or clock) line width, as shown in Fig. 10.5b. The capacitance (and therefore the dynamic power dissipation) of a line structure with wider spacing and uniform interconnect width is greater than the capacitance of an exponentially tapered structure.

Increasing the distance between the ground shield and the signal lines,

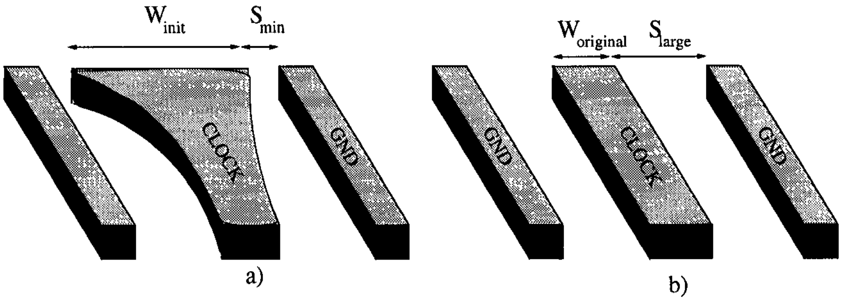


Figure 10.5: Coplanar clock line a) exponential tapering b) uniform line with wider spacing

as shown in Fig. 10.5, produces a smaller reduction in the line capacitance (and dynamic power) as compared to exponentially tapering the lines. Furthermore, a wider space between the ground lines increases the inductance of the line since the area of the current return path is larger. Furthermore, an increase in the space without a change in the interconnect width, as shown in Fig. 10.5b, maintains the same resistance as a uniform structure. An increase in the line inductance (without an increase in the resistance) increases the inductive behavior of the line. In section 10.4, a comparison is presented between the proposed tapered structure and two alternative non-tapered structures.

10.3.3 Clock Skew

H-trees are primarily used in clock distribution networks. An important issue in the design of a clock distribution network is clock skew. H-trees provide close to zero skew if the loads at all of the clock sinks are identical [229]. Different techniques have been developed to minimize clock skew in trees with varying loads. These techniques can be classified into two categories; (1) techniques that employ active elements (dummy loads or inserted buffers), [236]-[250], and (2) techniques that passively change the tree structure (the interconnect width or length or the topology of the tree) [246]-[253].

An exponentially tapered tree structure can be integrated with standard active skew reduction techniques without adapting the skew reduction phase of the design process. Active elements, inserted along the tree to reduce the skew, can be placed at the same locations in a tapered tree. Alternatively, in passive techniques, a more complicated model should be used to optimize the tree for low power while simultaneously minimizing the skew.

10.4 Simulation Results

Different industrial H-tree structured clock distribution networks have been investigated to evaluate the proposed design technique. The optimum width W_{init-L_n} and tapering factor p_{L_n} for each branch level L_n within each tree are determined. There are six branch levels ($M = 6$) in this clock tree example. Closed form expressions for the line impedance parameters (resistance, capacitance, and inductance) are used to model the tree interconnect [214]. Each interconnect branch is divided into a number of sections with length $l_1 = 125$ μm. l_1 is chosen to be greater than l_{min}, the shortest line in the tree. Two ground lines, with a 1 μm width, shield the tree interconnects. The minimum distance between the clock line and the ground shield S_{min} is 1 μm. Copper interconnect and low-κ dielectric materials are assumed in order to evaluate the inductive properties of the lines.

A 64 sink clock tree covering a die area of 4.25 X 4.25 mm is modeled as a distributed RLC network to observe the signal characteristics. A symmetric capacitive load is assumed at all of the sinks (no clock skew among the sinks). In section 10.4.1, a first order approximation is used to determine the optimum interconnect structure. A second order approximation is used in section 10.4.2.

10.4.1 First Order Approximation

used to size the interconnect within the tree as listed in Table 10.1. The interconnect branch level is listed in the first column. The width of the uniform wires that achieves the minimum signal transition time at the loads of the tree is listed in the second column. As listed in the table, for a standard H-tree, the interconnect width is decreased by half at each branch level to match the line impedance. An interconnect width of 10 μm at the source of the tree is assumed to minimize the signal transition time at the load end. The signal characteristics of the overall H-tree are provided in Table 10.2.

In the third and fourth columns, the optimum initial width and tapering factor, respectively, of each branch level are listed for an exponentially tapered interconnect based on a first order approximation . The optimum structure (the initial width and tapering factor) is determined from the program represented by the pseudocode described in Appendix H.

The ratio between the damping factor of each line segment for a tapered line and a uniform line is listed in the fifth column. The damping factor increases as compared to a uniform line, reducing the inductive effects in the signal waveform. In order to compare the proposed structure with a uniform structure with the same area overhead, the spacing S_{min} is increased to S_{large}

while maintaining the lines unshaped. A uniform line width (listed in the second column) with a larger spacing (listed in the sixth column) is also listed in the table as a design choice. Unlike a tapered line, the damping factor decreases if a larger spacing is used, increasing the inductive behavior (ringing effects) in the signal waveform.

Table 10.1: H-tree design techniques using a first moment approximation

Interconnect	Uniform tapering	Exponential tapering			Uniform with larger spacing	
Branch Level	$W_{original}$ (μm)	W_{init} (μm)	p (mm^{-1})	$\zeta/\zeta_{original}$	S_{large} (μm)	$\zeta/\zeta_{original}$
1	10.0	14.7	1.8	1.30	3.4	0.83
2	5.0	8.3	1.8	1.18	2.6	0.80
3	2.5	4.3	3.7	1.14	2.0	0.83
4	1.3	2.6	4.0	1.11	1.7	0.84
5	0.6	0.7	2.5	1.01	1.0	0.98
6	0.5	0.5	0.0	1.00	1.0	1.00

A reduction in the inductive behavior of the line can be observed by a change in the damping factor of the lines within the tree. As listed in Table 10.1, the damping factor ζ of an exponentially tapered structure increases while the damping factor of a uniform (with wider spacing) structure decreases. An increase in the damping factor reduces the inductive behavior of the interconnects, enhancing the signal integrity.

A 0.24 μm CMOS inverter is used to drive the tree in the example circuit characterized by Table 10.1. An input ramp signal with a 50 psec transition time is applied at the input of the driver of the tree. The lines at the source of the tree are wide (highly inductive), making these lines the most inductive among all of the interconnect within the tree. The greatest amount of reflections occurs at the source of the tree. The attenuation of the signal along the interconnect tree degrades the overshoots at the load end. The difference between the first overshoot and undershoot is therefore observed at the source of the tree. The difference between the first overshoot and undershoot $\Delta V_{over-under}$ decreases from 683 mV to 675 mV at the first branching point of a tapered structure. Alternatively, the difference increases to 836 mV when a larger spacing is assumed without shaping the lines. Tapering the interconnects achieves a reduction in $\Delta V_{over-under}$ of approximately 20% as compared to a uniform design with the same area overhead.

In Table 10.2, the signal characteristics (the propagation delay and transition time) and the transient power dissipated by a tree are listed for three interconnect structures. Exponential tapering and uniform tapering with a larger spacing maintain the same signal characteristics while dissipating less power. Exponential tapering, however, further reduces the power. A reduction in power dissipation of about 12% is achieved as compared to about 3.5% with no tapering.

10.4.2 Second Order Approximation

With increasing clock frequency, the signal transition time decreases, increasing the importance of considering the interconnect inductance. The signal transition time at the input of the H-tree described in section 10.4.1 is reduced to 10 psec. For such a fast transition time, a second order approximation is more effective as a criterion for tapering the lines within the tree. The interconnect width for an exponentially tapered line based on a second moment approximation is listed in Table 10.3. A greater reduction in the damping factor is achieved using a second moment approximation, reducing reflections in the tree (compare, for example, column five of Tables 10.1 and 10.3).

The signal transition time, propagation delay, and power dissipation are listed in Table 10.4. The second moment approximation achieves a greater power reduction of 15% as compared to the first order approximation.

The signal waveform at three points; the input of the driver, the first branching point, and the sinks (or load) is shown in Fig. 10.6. The difference between the first overshoot and undershoot $\Delta V_{over-under}$ decreases from 784 mV to 511 mV at the first branching point of a tapered structure. The difference increases to 854 mV when a larger spacing is assumed without shaping the lines. Tapering the interconnects achieves a reduction in $\Delta V_{over-under}$ of approximately 35%, reducing the inductive noise, thereby improving the signal integrity. Alternatively, increasing the spacing increases $\Delta V_{over-under}$ by 10%, degrading the signal integrity of the H-tree. As compared to a uniform tree with the same area overhead, the difference between the overshoots is reduced by 40% in a tapered line.

The aspect ratio (the ratio between the line thickness to the line width) increases as technology advances, reducing the propagation delay. In order to demonstrate the effect of a higher aspect ratio on the proposed tapering technique, exponential tapering, based on a second order approximation, is compared with uniform tapering in Table 10.5 for an interconnect thickness of 0.1 μm. The signal delay, transition time, and power dissipation are listed in the table. A higher reduction in power dissipation is achieved (as compared to Tables 10.2 and 10.4) since the line thickness is larger. For a higher aspect ratio, the coupling capacitance is greater, increasing the per cent reduction in

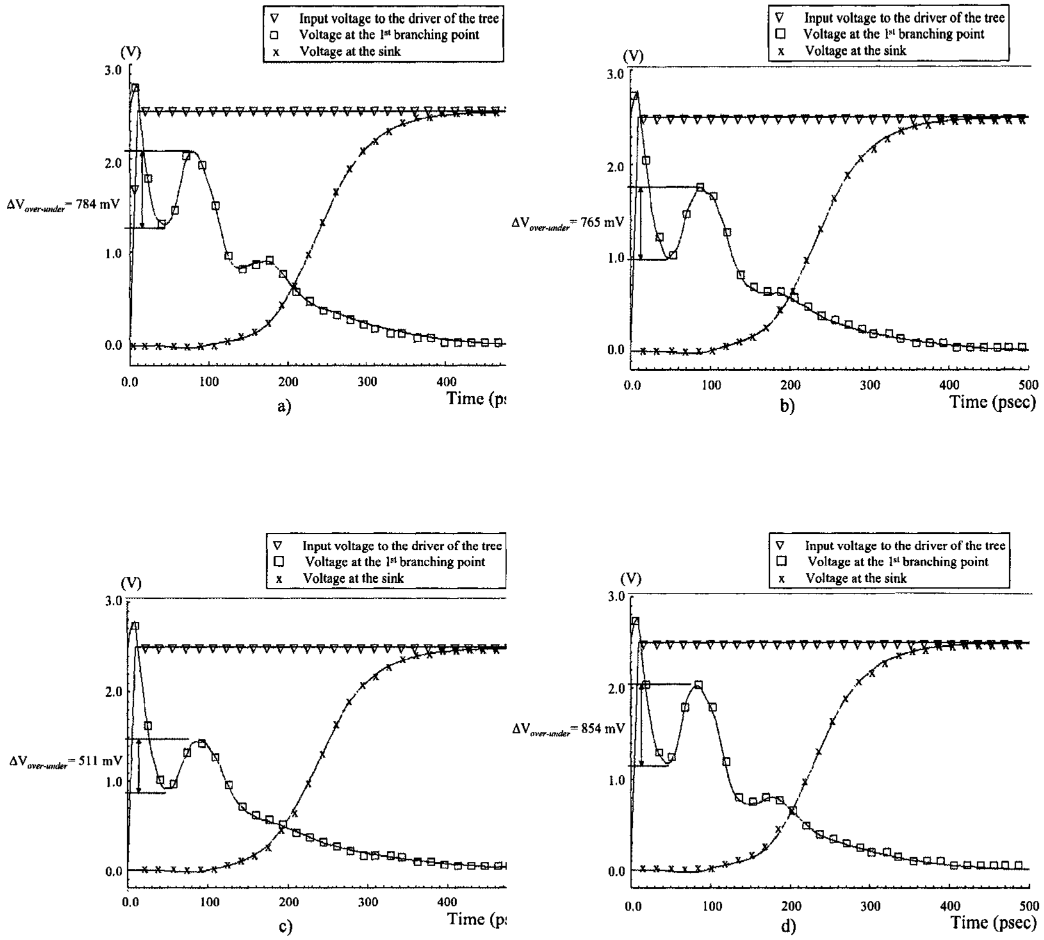


Figure 10.6: Waveforms at different nodes within the tree a) uniform tapering b) exponential tapering using first order approximation c) exponential tapering using second order approximation d) uniform tapering (with large spacing)

power dissipation in tapered lines. As technologies advance, a higher aspect ratio and interconnect thickness becomes typical. The proposed tapering technique will therefore achieve a greater reduction in power with technology scaling.

10.5 Conclusions

Exponentially tapered interconnect can reduce the dynamic power dissipated by clock distribution networks. A structure for sizing the interconnects within an H-tree network is proposed. The structure does not maintain a tapering factor of two in the line width at the branch points along the H-tree. The proposed technique reduces the power dissipation while improving the signal characteristics.

First and second order approximations of the transfer function can be used to size tapered lines of a clock distribution network. The first order approximation reduces the power dissipation and inductive noise of an H-tree structured clock distribution network. Alternatively, a second order approximation can be used to achieve a greater reduction in both power dissipation and inductive noise.

Exponentially tapered interconnects based on a first order approximation are shown to reduce the power dissipated by an industrial clock distribution network by up to 12% while maintaining the same signal transition times and propagation delay at the load. A higher reduction in power dissipation of 15% is achieved when the second moment is used in the optimization process. This exponential tapering technique is expected to be more efficient with advancements in technology.

Furthermore, the inductive behavior of the interconnects is reduced, reducing the inductive noise. Smaller reflections occur in an exponentially tapered tree. A reduction of 35% in the difference between the signal overshoots at the input of a tree is achieved, increasing the efficiency of using exponential tapering in propagating signals at high frequencies. As compared to a uniform tree with the same area overhead, the difference between the overshoots is reduced by 40%.

Table 10.2: Signal characteristics and power dissipation of different H-tree clock distribution structures

Technique	t_r	t_{pd}	P_{total}		$\Delta V_{over-under}$	
	(psec)	(psec)	(mW)	Reduction	(mV)	Reduction
Uniform Tapering	149	227	5.18	—	683	—
Exponential using first order Approximation	141	215	4.56	12%	675	1%
Uniform (larger spacing)	143	208	5.00	3.5%	836	-23%

Table 10.3: H-tree design techniques using second moment approximation

Interconnect	Uniform tapering	Exponential tapering			Uniform with larger spacing	
Branch Level	$W_{original}$ (μm)	W_{init} (μm)	p (mm^{-1})	$\zeta/\zeta_{original}$	S_{large} (μm)	$\zeta/\zeta_{original}$
1	10.0	11.6	2.2	1.85	1.80	0.91
2	5.0	8.0	2.3	1.07	2.50	0.82
3	2.5	3.8	4.6	1.56	1.65	0.87
4	1.3	2.1	3.5	1.20	1.40	0.89
5	0.6	0.73	2.7	1.02	1.05	0.98
6	0.5	0.5	0.0	1.00	1.00	1.00

Table 10.4: Signal characteristics and power dissipation of different H-tree clock distribution structures

Technique	t_r	t_{pd}	P_{total}		$\Delta V_{over-under}$	
	(psec)	(psec)	(mW)	Reduction	(mV)	Reduction
Uniform Tapering	142	236	6.09	—	784	—
Exponential using first order Approximation	142	232	5.38	12%	765	2%
Exponential using second order Approximation	147	235	5.18	15%	511	35%
Uniform (larger spacing)	139	228	5.60	8%	854	-10%

Table 10.5: Signal characteristics and power dissipation of different H-tree clock distribution structures

Technique	t_r (psec)	t_{pd} (psec)	P_{total}	
			(mW)	Reduction
Uniform Tapering	168	271	4.3	
Exponential using second order Approximation	167	271	4.2	3%

Chapter 11

Conclusions

Interconnect design has become significant as operating frequencies have increased since the interconnect affects the two primary design criteria, speed and power. Furthermore, the line inductance cannot be neglected in next generation high speed circuits. Including line inductance in the design process can enhance both the delay and power as well as improve the accuracy of the overall design process. The line inductance introduces new circuit tradeoffs and design methodologies.

A tradeoff exists between dynamic and short-circuit power in inductive interconnects. This tradeoff is not significant in resistive lines as the signal characteristics are less sensitive to the line dimensions. The short-circuit power of an overdriven interconnect line decreases with line width, while the dynamic power increases. When the line exceeds the matched condition, not only the dynamic power but also the short-circuit power increases with increasing line width. The matched condition between the driver and the load has an important effect on the line impedance characteristics. If the line is overdriven, the short-circuit power decreases with increasing line width. When the line exceeds the matched condition, the short-circuit power increases with increasing line width (and signal transition time). To achieve lower transient power dissipation, the minimum line width should be used if the line is underdriven. For a long inductive interconnect line, an optimum interconnect width exists that minimizes the total transient power dissipation.

Repeater insertion outperforms wire sizing in *RC* lines. However, for *RLC* lines, the minimum signal propagation delay always decreases with increasing wire width if an optimum repeater system is used. In *RLC* lines, wire sizing outperforms repeater insertion as the minimum signal propagation delay with no repeaters is less than the minimum signal propagation delay using any number of repeaters. The minimum signal propagation delay always decreases with wider lines until the number of repeaters equals zero (only one driver at the begining of the line is sufficient). In *RLC* lines, there is no optimum interconnect width for minimum signal propagation delay. The total transient power dissipation of a repeater system driving an *RLC* line is minimum at small line widths. Below the width for minimum power, both the signal delay and the power dissipation increase. Widening a line beyond the width for minimum power reduces the number of repeaters and the minimum signal propagation delay while increasing the total transient power dissipation. A tradeoff between the transient power dissipation and the signal propagation delay, therefore, exists in sizing the interconnect width. Optimizing the interconnect for minimum power delay product produces a much smaller increase in both the power and delay as compared to separately optimizing for either the power or delay. As interconnects become longer, the difference between the optimum width for minimum power and the optimum width for minimum delay increases, further enhancing the effectiveness of the proposed criterion.

A criterion, the Power-Delay-Area-Product (PDAP), is introduced as an efficient technique to size an interconnect within a repeater system if the system area is considered in the design process. A significant reduction in power dissipation is achieved with a negligible increase in propagation delay if the line width is optimized for minimum PDAP rather than minimum PDP. Furthermore, a reduction in silicon area is achieved if the PDAP criterion is used.

On-chip inductance shields part of the interconnect capacitance. The effective capacitance of an *RLC* load decreases with increasing line inductance, reducing the gate delay of a driver. Furthermore, the line inductance reduces the equivalent output resistance of a driver, reducing the total propagation delay. A parameter Z_T, the ratio of the output driver resistance to the magnitude of the lossy characteristic impedance of the line, is introduced to characterize the signal propagation delay of a CMOS inverter driving an *RLC* interconnect. The minimum propagation delay is achieved when $Z_T = 1$ where the driver is matched with the lossy characteristic impedance of the line. A smaller buffer can be used to drive an interconnect line if the line inductance is considered, more accurately achieving the target delay than if the line inductance is ignored.

The optimum wire shape that produces the minimum signal propagation delay in a distributed *RLC* line is shown to be an exponential function. An exponentially tapered interconnect minimizes the time of flight of an *LC* line. The general form for the optimum shaping function of an *RLC* line is qe^{px}. The optimum wire width at the load end q and the optimum tapering factor p which achieve the minimum delay and low power are determined for the driver and load characteristics. Optimum wire tapering as compared to uniform wire sizing is more efficient in *RLC* lines than in *RC* lines. The line inductance makes tapering more attractive in *RLC* lines since tapering produces a greater reduction in delay as compared to uniform wire sizing.

With a minimum wire width at the far end and an optimum tapering factor, both the propagation delay and the power dissipation are reduced. The line inductance increases the savings in power in an optimally tapered line as compared to uniform wire sizing. An analytic solution for the tapering factor that produces the minimum transient power is determined.

Tapered wire sizing outperforms both uniform wire sizing and uniform repeater insertion. A reduction in the propagation delay is achieved when optimum tapering is used rather than uniform repeater insertion. Wire tapering as compared to repeater insertion becomes more efficient as technology advances, since the reduction in the delay of tapered lines increases.

Wire tapering can improve signal integrity by reducing the inductive noise. Tapered interconnect lines in clock distribution networks can achieve the same signal characteristics of uniformly sized lines, while reducing the reflections along the line. The difference between the signal overshoots decreases when tapered interconnect is used rather than uniform interconnect while producing the same signal delay and transition time.

Exponentially tapered interconnect can reduce the dynamic power dissipated by clock distribution networks. A structure for sizing the interconnects within an H-tree network is proposed. The structure does not maintain a tapering factor of two in the line width at the branch points along the H-tree.

The proposed technique reduces the power dissipation while improving the signal characteristics.

First and second order approximations of the transfer function can be used to size tapered lines of a clock distribution network. The first order approximation reduces the power dissipation and inductive noise of an H-tree structured clock distribution network. Alternatively, a second order approximation can be used to achieve a greater reduction in both power dissipation and inductive noise.

On-chip inductance must be included in the design process in high frequency circuits. By including on-chip inductance, the efficiency of different circuit design techniques such as wire sizing, repeater insertion, line tapering, and driver sizing can be greatly enhanced.

Chapter 12

Future Work

Interconnect inductance has become important in modeling on-chip interconnects. Neglecting the line inductance may result in inefficient circuits. It is shown in this dissertation that different circuit design techniques can be enhanced when on-chip inductance is included in the design process. Novel tradeoffs and methodologies have been proposed to achieve efficient circuit operation at high frequencies. These techniques and methodologies can be further enhanced to achieve the design requirements of very deep submicrometer (VDSM) circuits.

In the following sections, different approaches are suggested to further improve existing design methodologies which consider the inductive characteristics of the interconnect lines. In Section 12.1, a reduced order model to characterize a tapered interconnect is discussed. This model is important to characterize the line using fewer elements. In Section 12.2, tapering an interconnect line in three dimensions is proposed. Novel techniques have been described in [254]-[258] to drive long interconnects. The inductance of these interconnects should be considered when evaluating the efficiency of these techniques. In Section 12.3, the importance of line inductance on advanced circuit techniques for driving long interconnects is discussed. Trends in high frequencies are described in Section 12.4 to motivate more advanced circuit design methodologies. In Section 12.5, these suggested topics for future research are summarized.

12.1 Reduced Order Model for Tapered *RLC* Interconnect

Interconnect tapering is presented in Chapters 8 and 10 as an efficient technique to reduce signal propagation delay and power dissipation. Exponential tapering changes the line impedance parameters, affecting the signal characteristics. Accurate modeling of tapered lines is required in order to characterize the line impedance in a reduced order model. A reduced order model of a tapered line also improves the computational speed as compared to dynamic simulation.

A tapered interconnect is a physically complicated structure which requires a simplified reduced order model to enhance the circuit simulation process. A reduced order model at the driving point would be useful to determine the signal characteristics with a fewer number of impedance elements to model the line. A reduced order model for a tapered line can therefore be used to increase the efficiency of the design process.

12.2 Interconnect Tapering in Three Dimensions

From the discussion in Chapter 8, tapering is an efficient technique to reduce signal delay and power dissipation. Moreover, exponential tapering is shown to be more efficient in *RLC* lines than in *RC* lines. As technology advances, interconnect design will become an increasingly important issue in the IC design process.

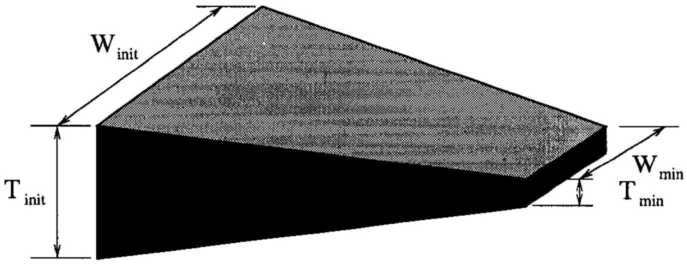


Figure 12.1: Tapered interconnect line in three dimensions

Exponential tapering can be expanded by tapering the line in three dimensions, as shown in Fig. 12.1. Tapering the interconnect height can improve the performance of a circuit. Furthermore, the line capacitance of a tapered interconnect is less than the capacitance of a uniform interconnect, due to decreased fringing fields, reducing the dynamic power dissipation. Moreover, the inductive noise of a tapered line is smaller than in a uniform line. Three-dimensional tapering, however, greatly complicates the manufacturing process. Also, practically, precise tapering is extremely difficult. The optimum exponential shape can be approximated by dividing the line into sections with different widths and thicknesses for each section as shown in Fig. 12.2.

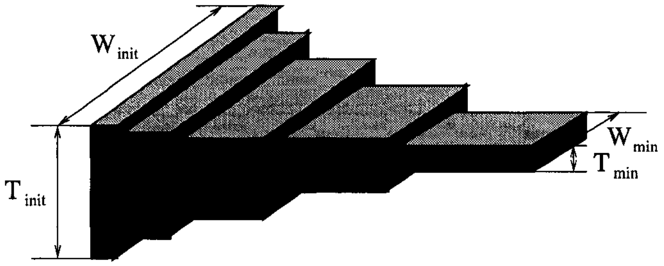


Figure 12.2: 3-D tapered interconnect using sections with different widths and thicknesses

Different techniques can be developed to simplify the fabrication process for tapering the line thickness. The number of metal layers increases with advances in technology, and is expected to reach ten layers by 2007 [4]. Certain upper metal layers can be dedicated to global communication. These lines can be tapered in three dimensions to improve circuit performance while reducing power dissipation. In order to simplify the process, interconnect lines can be categorized according to the line length into a few sets $\{S_1, S_2, S_3, ...S_n\}$. Each set S_i contains a range of line lengths l_i, where

$$l_{i1} < l_i < l_{i2}, \tag{12.1}$$

$$l_{(i)2} = l_{(i+1)1}. \tag{12.2}$$

The tapering factor of each set can be maintained constant, reducing the variation in the line thickness for different interconnect lines. Long vias can be used to produce the tapered shape as shown in Fig. 12.3. Different tapering factors can be achieved by using different lengths for each metal layer.

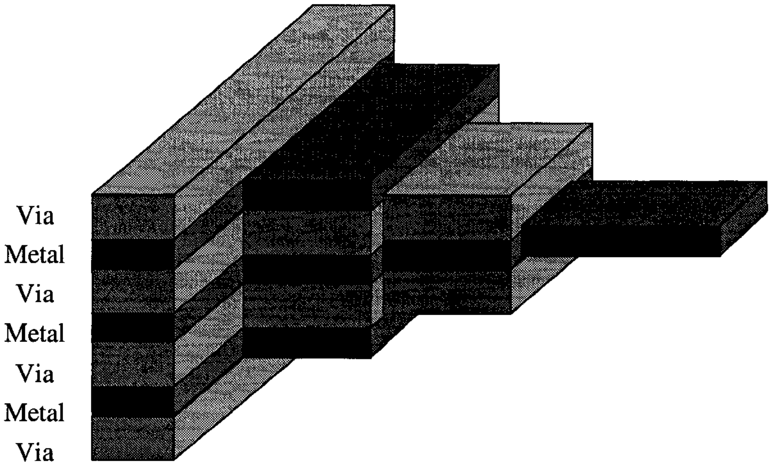


Figure 12.3: 3-D tapered interconnect using long vias

This technique can potentially enhance circuit performance from 10% to

20%. Simultaneously, the power dissipation can be decreased by up to 20% while also decreasing the inductive noise of the line.

12.3 Techniques to Drive Long Interconnects

Many of the more widely used techniques to drive long interconnects have been described in this dissertation. There are several circuit design techniques to enhance circuit speed. Current sensing [254]-[256], transparent repeaters [258], and boosters [257] are examples of these promising design techniques.

Current sensing is a technique for quickly transferring data along long distances by sensing changes in the current flowing through the interconnect. The data can propagate along these long distances without repeaters. This technique, however, has been investigated without considering line inductance. Since the technique is based on sensing current, the interconnect inductance may affect the efficiency and applicability of this technique. Topics such as noise and reliability should also be considered. Furthermore, the inductive properties of the line could potentially be used to enhance the current sensing properties of the design technique.

Capacitive coupling has been considered in current sensing techniques [255]. As shown in Fig. 12.4, the effect of a switching neighbor on the operation of a circuit is used to evaluate the effective capacitive coupling.

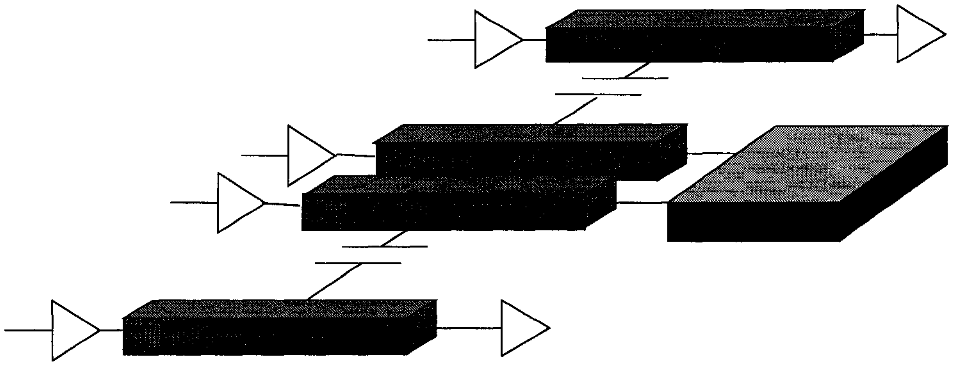


Figure 12.4: Capacitive coupling in current sensing technique

The interconnect lines of a current sensing circuit can provide a return path since there is a direct path to ground. Unlike electric field lines, magnetic field lines do not vanish at the adjacent interconnect line. The magnetic field lines can extend in space, affecting both lines of the sensing circuit, as shown in Fig. 12.5. Inductive coupling can therefore potentially affect the successful operation of a circuit. Furthermore, the inductance of the lines used to sense the current may provide a new design opportunity for the sensing circuit. The shape, width, and/or separation of these lines could improve the circuit characteristics.

Transparent repeaters (or boosters) are proposed in [257, 258] to drive long interconnects. The interconnect inductance has also been neglected in this circuit technique. As described in this dissertation, the line inductance can introduce new types of design tradeoffs. The interconnect inductance can, therefore, affect the number and placement of the boosters (or trans-

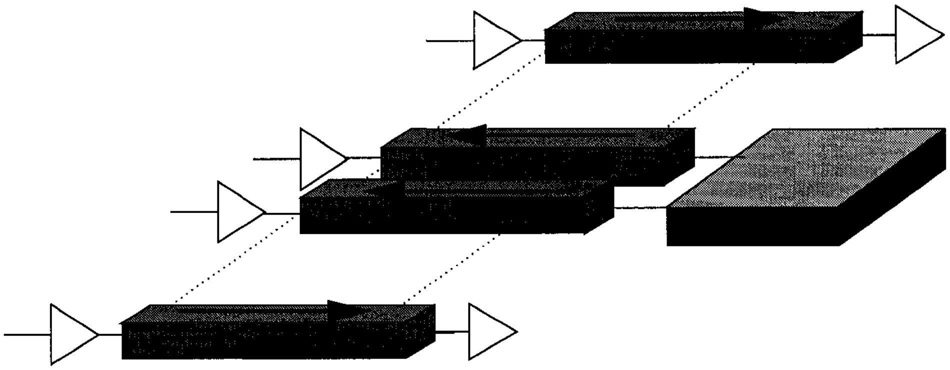


Figure 12.5: Inductive coupling in current sensing technique

parent repeaters). The inductive noise can affect the function and limit the application of these circuits. Despite these limitations, these approaches can be quite useful in certain applications.

12.4 Design Methodologies for Frequency Dependent Interconnect Impedances

With increasing clock frequencies, different mechanisms affect the signal characteristics in long interconnects. These mechanisms alter the impedance characteristics of the interconnect. At high frequencies, the current distribution along the interconnect cross section changes. The change in the current distribution affects the flow of current due to related phenomena such as skin and proximity effects [87]. These effects cause a change in the line resistance and inductance. The skin and proximity effects occur at high frequencies, increasing the resistance and decreasing the inductance of a line. For small spacing between interconnect lines, the proximity effect alters the current distribution along the cross section of the interconnect. The resistance of a 4 μm wide aluminum line as a function of frequency is shown in Fig. 12.6. Assuming 1 μm wide ground lines shielding a victim line from both sides, the line inductance and resistance behave as shown in Fig. 12.6 [112].

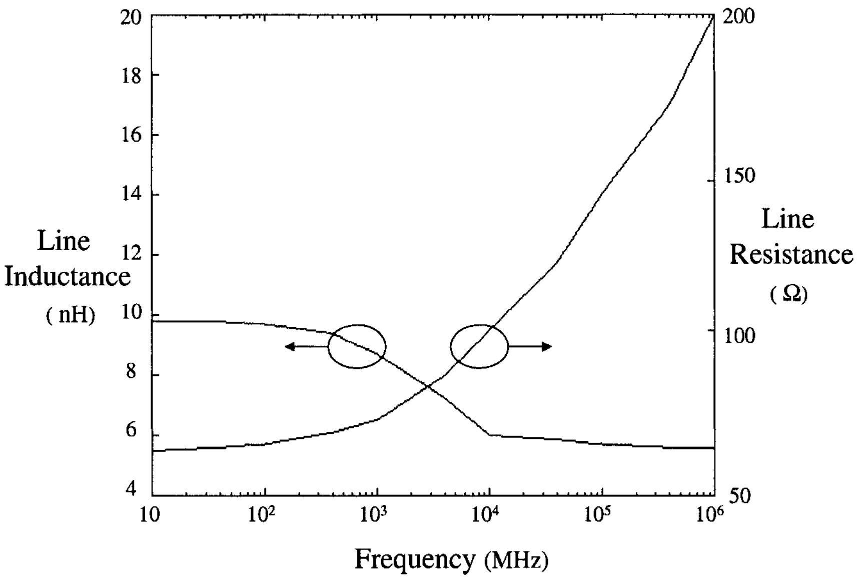


Figure 12.6: Interconnect resistance and inductance with frequency

Advanced design methodologies will be necessary that consider frequency dependent changes in the line impedance parameters when the frequency exceeds the limit at which existing interconnect models are no longer accurate. These effects may alter trends and suggest different speed/area/power tradeoffs in existing methodologies. Methodologies will therefore need to be developed that manage interconnects deep into the gigahertz frequency range.

Due to skin and proximity effects, the effective width W_{eff} (the width through which the current flows) of the interconnect is less than the actual (physical) width. The effective width of an interconnect can be expressed in terms of the line geometry, the distance to the surrounding conductors, and the signal transition time. The concept of an effective width can simplify the model of the impedance characteristics at high frequencies.

In order to develop efficient optimization techniques, advanced models of the line inductance and resistance as a function of the effective width are required,

$$L_{int} = g(W_{eff}), \tag{12.3}$$

$$R_{int} = g(W_{eff}), \tag{12.4}$$

where W_{eff} is a function of the interconnect width and thickness, spacing between the interconnects, and the signal frequency.

12.5 Summary

Different interconnect design methodologies will need to be enhanced to include the interconnect inductance in interconnect line models. The on-chip inductance has an increasing influence on existing design methodologies for circuits operating at high frequencies. More sophisticated design methodologies that consider line inductance can achieve a target performance while reducing power dissipation as well as inductive noise. Advanced design methodologies are therefore required to achieve target performance objectives for circuits operating at gigahertz frequencies. The effects of the on-chip inductance should therefore be integrated into existing and future CAD tools to improve the efficiency of high speed integrated circuits.

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Appendices

Appendix A

Transition Time for a Signal at the Far End of an Inductive Interconnect

To determine an analytic solution for the signal transition time at the far end of an inductive interconnect, a lumped RLC model of the interconnect impedance is assumed. A lumped RLC model is widely used as a simple reduced order model for inductive interconnects [20], [125], [151]-[155]. The total line resistance, capacitance, and inductance are $R_t = R\,l$, $C_t = C\,l$, and $L_t = L\,l$, respectively, where l is the line length. Adding the gate capacitance C_g to the line capacitance, the total load capacitance is $C_p = C_t + C_g$. The input ramp signal is

$$V_{in}(t) = \begin{cases} \frac{t}{\tau_r} V_{dd} & \text{for } 0 \leq t \leq \tau_r, \\ V_{dd} & \text{for } t > \tau_r, \end{cases} \tag{A.1}$$

where τ_r is the transition time of the input signal. The line is assumed to be driven by a CMOS inverter. For the case where the transition time of the input and output signals is comparable, the operation of a CMOS inverter can be divided into four regions as listed in Table A.1. Some of these regions can be of short duration or not occur, but in the general case, all of these regions may exist. When V_{in} transitions from low-to-high, the PMOS transistor initially operates in the triode region, then enters the saturation region. When the input signal reaches $V_{dd} - |V_{tp}|$, the PMOS transistor turns off, and the charge on the capacitive load discharges through the NMOS transistor. The NMOS transistor initially operates in the saturation region, then moves into the triode region.

The PMOS and NMOS transistors can be modeled by the equivalent resistances $R_p = 1/\gamma_p$ and $R_n = 1/\gamma_n$, respectively. According to the n_{th}-power law MOSFET model [213], γ_p is

$$\gamma_p = \alpha_p K_p \left(|V_{gsp} - V_{tp}|\right)^{m_p}, \tag{A.2}$$

where K_p and m_p control the triode region characteristics of the transistor, α_p is a constant between one and two which represents the dependence of the MOSFET equivalent resistance on the drain-to-source voltage V_{ds}, and V_{gs} is the gate-to-source voltage of the transistor. p and n connote the P-channel

Table A.1: Different regions of operation for a CMOS inverter with a ramp input signal for comparable input and output signal transitions after the input signal exceeds the threshold voltage of the NMOS transistor ($V_{in} > V_{tn}$)

Region	Condition		NMOS	PMOS
I	$V_{dd} - \|V_{tp}\| > V_{in} \geq V_{tn}$	$V_o > V_{in} + \|V_{tp}\|$	Saturation	Triode
II		$V_o > V_{in}$ - V_{tn}	Saturation	Saturation
III		$V_o \leq V_{in}$ - V_{tn}	Triode	Saturation
IV	$V_{in} \geq V_{dd} - \|V_{tp}\|$		Triode	Cut-off

and N-channel transistor, respectively.

In region I, after V_{in} exceeds the NMOS transistor threshold voltage V_{tn}, the saturation current of the NMOS transistor is

$$I_{nI}(t) = B_n(V_{in}(t) - V_{tn})^{n_n} \text{ for } t \geq \tau_{nON} \ , \tag{A.3}$$

where B_n and n_n describe the saturation region characteristics of the NMOS transistor and τ_{nON} is given by $V_{dd}\frac{\tau_r}{V_{tn}}$. At the output node of the driver, the KCL and KVL equations are

$$I_p + I_l = I_n, \tag{A.4}$$

$$V_o = V_c - V_r - V_l, \tag{A.5}$$

respectively, where V_o is the voltage at the output node and V_r, V_l, and V_c are the voltages across the resistance, inductance, and capacitance, given by (A.6), (A.7), and (A.8), respectively. I_p, I_n, and I_l are the currents through the PMOS transistor, the NMOS transistor, and the load capacitor, respectively,

$$V_r(t) = I_l(t)\, R_t, \tag{A.6}$$

$$V_l(t) = L_t\, \frac{dI_l(t)}{dt}, \tag{A.7}$$

$$V_c(t) = -\frac{1}{C_p} \int I_l(t). \tag{A.8}$$

In region I, I_p, I_l, and V_c are given by (A.9), (A.10), and (A.11), respectively,

$$I_{pI}(t) = \gamma_p(V_{dd} - V_o), \tag{A.9}$$

$$I_{lI}(t) = A + B\,t + D_1\, e^{-\alpha_{p1}\, t} + D_2\, e^{-\alpha_{p2}\, t}, \tag{A.10}$$

$$V_{cI}(t) = V_{dd} - \frac{1}{C_p}\, [\, A\,t + B\, \frac{t^2}{2} + D_1\,(1 - e^{-\alpha_{p1}\, t}) + D_2\,(1 - e^{-\alpha_{p2}\, t})], \tag{A.11}$$

where A, B, D, E, α_{p1}, and α_{p2} are constants given by

$$A = -(D_1 + D_2), \tag{A.12}$$

$$B = q\, C_p\, L_t, \tag{A.13}$$

$$D_1 = q\, e^{\beta \alpha_{p1}} \frac{1}{\alpha_{p1}^2(\alpha_{p2} - \alpha_{p1})}, \tag{A.14}$$

$$D_2 = q\, e^{\beta \alpha_{p2}} \frac{1}{\alpha_{p2}^2(\alpha_{p1} - \alpha_{p2})}, \tag{A.15}$$

$$\alpha_{p1} = \frac{\frac{1+R_t\gamma_p}{L_t\gamma_p} + \sqrt{\left(\frac{1+R_t\gamma_p}{L_t\gamma_p}\right)^2 - \frac{4}{L_tC_p}}}{2}, \tag{A.16}$$

$$\alpha_{p2} = \frac{\frac{1+R_t\gamma_p}{L_t\gamma_p} - \sqrt{\left(\frac{1+R_t\gamma_p}{L_t\gamma_p}\right)^2 - \frac{4}{L_tC_p}}}{2}, \tag{A.17}$$

$\beta = \frac{\tau_r V_{tn}}{V_{dd}}$, and $q = (n_n)!(\frac{V_{dd}}{\tau_r})^{n_n}$.

Region II starts when $V_o(t)$ reaches $V_{in} + |V_{tp}|$. In this region, the PMOS transistor is saturated. The output voltage in this region can be determined using a Newton-Raphson iteration. $V_c(\tau_{psat})$ is determined by (A.11), where τ_{psat} is the initial time of this region. Since both transistors have the same drain voltage, the second region of operation in which both transistors are saturated is quite short, permitting the change in V_c during this region to be neglected.

During region III, the NMOS transistor operates in the triode region, and the PMOS transistor is saturated. Expressions for $I_l(t)$ and $V_c(t)$ are similarly obtained as in region I, and are given by (A.18) and (A.19), respectively.

$$I_{lIII}(t) = A_1 + B_1\,t + E_1\,e^{-\alpha_{n1}t} + E_2 e^{-\alpha_{n2}t}, \tag{A.18}$$

$$V_{cIII}(t) = V_c(\tau_{psat}) - \frac{1}{C_p}\int_{\tau_{psat}}^{t} I_{lIII}(t)\,dt, \tag{A.19}$$

where A_1, B_1, E_1, and E_2 are constants given by

$$\begin{aligned}
A_1 &= I_{lIII}(\tau_{psat}) - (B_1\tau_{psat} + E_1 e^{-\alpha_{n1}\tau_{psat}} + E_2 e^{-\alpha_{n2}\tau_{psat}}), && \text{(A.20)}\\
B_1 &= -2\,C_p\,\frac{b}{\gamma_n}, && \text{(A.21)}\\
E_1 &= \frac{\alpha_{n1}{}^2\gamma_n V_{oIII}(\tau_{psat}) - 2b - a^2 b\alpha_{n1}{}^2 - 2ab\alpha_{n1}}{\alpha_{n1}{}^2(\alpha_{n2} - \alpha_{n1})\gamma_n L_t}, && \text{(A.22)}\\
E_2 &= \frac{\alpha_{n2}{}^2\gamma_n V_{oIII}(\tau_{psat}) - 2b - a^2 b\alpha_{n2}{}^2 - 2ab\alpha_{n2}}{\alpha_{n2}{}^2(\alpha_{n1} - \alpha_{n2})\gamma_n L_t}, && \text{(A.23)}\\
\alpha_{n1} &= \frac{\frac{1+R_t\gamma_n}{L_t\gamma_n} + \sqrt{(\frac{1+R_t\gamma_n}{L_t\gamma_n})^2 - \frac{4}{L_tC_p}}}{2}, && \text{(A.24)}\\
\alpha_{n2} &= \frac{\frac{1+R_t\gamma_n}{L_t\gamma_n} - \sqrt{(\frac{1+R_t\gamma_n}{L_t\gamma_n})^2 - \frac{4}{L_tC_p}}}{2}, && \text{(A.25)}\\
b &= B_p(\frac{V_{dd}}{\tau_r})^{n_p}, && \text{(A.26)}\\
a &= \frac{(V_{dd} - V_{tp})\tau_r}{V_{dd}}, && \text{(A.27)}\\
\gamma_n &= \alpha_n K_n (V_{gsn} - V_{tn})^{m_n}, && \text{(A.28)}
\end{aligned}$$

K_n and m_n control the triode region characteristics of the NMOS transistor, B_p and n_p are parameters that determine the characteristics of the saturation region of a PMOS transistor, and α_n is similar to α_p for an NMOS transistor.

Once V_{in} reaches $V_{dd} - |V_{tp}|$, the PMOS transistor turns off, initiating region IV. The time at which this region begins is $\tau_{pOFF} = \frac{(V_{dd}-|V_{tp}|)\tau_r}{V_{dd}}$, where $V_o(\tau_{pOFF})$ is obtained from (A.5). After the PMOS transistor turns off, the NMOS transistor continues to operate in the triode region. An expression for $V_c(t)$ in this region is

$$V_{cIV}(t) = V_c(\tau_{pOFF})e^{-\alpha_{n2}(t-\tau_{pOFF})}. \tag{A.29}$$

The transition time is expressed by $\tau_0 = \frac{t_{10\%}-t_{90\%}}{0.8}$, where $t_{10\%}$ and $t_{90\%}$ are the times at which the signal reaches 10% and 90% of the final value, respectively.

Appendix B

Expressions for line impedance parameters of an interconnect shielded with two ground lines

For an interconnect line shielded with two ground lines, analytic expressions for the line impedance can be characterized. Closed form expressions for the interconnect resistance, capacitance, and inductance are provided in this appendix. Neglecting skin and proximity effects, the line resistance is characterized by the simple relation,

$$R_{line} = \frac{\rho\, l}{W_{INT}\, T}, \tag{B.1}$$

where ρ and T are the line resistivity and thickness, respectively. The line capacitance is [140]

$$C_{int} = \epsilon_{ox}\, l\, (C_a + 2C_b), \tag{B.2}$$

where

$$\begin{aligned} C_a &= \frac{W_{int}}{H} + 2.24(\frac{W_{int}}{H})^{0.0275}(1 - 0.85e^{(-0.62\frac{S}{H})}) \\ &+ 0.32log(\frac{T}{S})(0.15\frac{S}{H}e^{-1.62\frac{T}{S}} - 0.12e^{(-0.065\frac{S}{T})}), \qquad \text{(B.3)} \\ C_b &= \frac{T}{S} + 1.31(\frac{T}{H})^{0.073}(\frac{S}{H} + 1.38)^{-2.22} \\ &+ 0.4log(1 + 5.46\frac{W_{int}}{S})(\frac{S}{H} + 1.12)^{-0.81}. \qquad \text{(B.4)} \end{aligned}$$

S is the spacing between the signal line ground shield and H is the height of the metal layer from the substrate. Assuming the return path is in an adjacent ground line [141], the line inductance is

$$L_{int} = l\,(L_s - 2.0M_{sg} + \frac{L_g}{2.0} + \frac{M_{gg}}{2.0}), \qquad \text{(B.5)}$$

$$\begin{aligned} L_g &= 0.2\,(log(\frac{2\,l}{W_g + T}) + 0.5 + 0.22\frac{W_g + T}{l}), \qquad \text{(B.6)} \\ M_{sg} &= 0.2\,(log(\frac{2\,l}{d_{sg}}) - 1.0 + \frac{d_{sg}}{l}), \qquad \text{(B.7)} \\ M_{gg} &= 0.2\,(log(\frac{2\,l}{d_{gg}}) - 1.0 + \frac{d_{gg}}{l}), \qquad \text{(B.8)} \\ L_s &= 0.2\,(log(\frac{2\,l}{W_{int} + T}) + 0.5 + 0.22\frac{W_{int} + T}{l}), \qquad \text{(B.9)} \end{aligned}$$

where W_g is the width of the ground shield, d_{sg} is the distance between the center of the signal line and the ground shield, and d_{gg} is the distance between the center of the two ground shields.

Appendix C

Effective Capacitance of an *RLC* Load

In order to compare the effective capacitance of *RC* and *RLC* delay models, the signal transition time at the output of a driving inverter V_o is assumed equal for both models. The waveform used in [194] is assumed to compare the effective capacitance of an *RLC* model with the model described in [194].

$$V_o(t) = \begin{cases} V_{dd} - ct^2 & \text{for } 0 \leq t \leq t_x, \\ a + b(t - t_x) & \text{for } t_x \leq t \leq t_D, \end{cases} \tag{C.1}$$

where $b = -0.8\frac{V_{dd}}{t_r}$ and t_x, t_D, a, and c are constants that characterize the waveform of V_o. t_r is the transition time of V_o which is obtained iteratively after determining the effective capacitance. The waveform of a signal propagating along an *RLC* line may be distorted by the inductance. However, the effect of this distortion on the effective capacitance is not significant. The effective capacitance of the π_{21} model is the capacitance which draws an average current equal to the average current drawn from both C_1 and C_2 in the π_{21} model [194]. The average currents, I_{c1-av} and I_{c2-av}, discharge (for an output high-to-low transition) the capacitances C_1 and C_2, respectively, as shown in Fig. C.1.

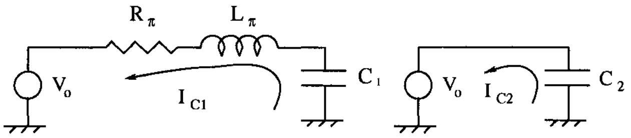

Figure C.1: Discharge currents for the π_{21} RLC model

Laplace transforms are used to obtain an expression for I_{c1-av}. The average I_{c1-av} during a high-to-low transition is

$$I_{c1-av} = \frac{I_{c1-av-I}t_x + I_{c1-av-II}(t_D - t_x)}{t_D}, \tag{C.2}$$

where

$$\begin{aligned} I_{c1-av-I} &= \frac{-1}{t_x L_\pi}(A\frac{{t_x}^2}{2} + Bt_x + D + Ee^{-\alpha_1 t_x} + Fe^{-\alpha_2 t_x}) + C_1\frac{V_{dd}}{t_x} \quad (C.3) \\ I_{c1-av-II} &= \frac{-1}{(t_D - t_x)L_\pi}(A_1(t_D - t_x) + B_1 + D_1 e^{-\alpha_1(t_D - t_x)} \\ &+ E_1 e^{-\alpha_2(t_D - t_x)}) + C_1\frac{V_{C1t_x}}{(t_D - t_x)}, \quad (C.4) \end{aligned}$$

$$V_{C1t_x} = \frac{1}{C_1 L_\pi}\left(A\frac{t_x^2}{2} + Bt_x + D + Ee^{-\alpha_1 t_x} + Fe^{-\alpha_2 t_x}\right), \tag{C.5}$$

$$A = -2cL_\pi C_1, \tag{C.6}$$

$$B = -2cR_\pi L_\pi C_1^2, \tag{C.7}$$

$$D = -(E+F) + V_{dd}L_\pi C_1, \tag{C.8}$$

$$E = \frac{E_0}{\alpha_1^3(\alpha_1 - \alpha_2)}, \tag{C.9}$$

$$F = \frac{F_0}{\alpha_2^3(\alpha_2 - \alpha_1)}, \tag{C.10}$$

$$E_0 = -2c + \alpha_1^2 V_{dd} + \alpha_1^4 V_{dd} L_\pi C_1 - \alpha_1^3(R_\pi C_1 V_{dd}), \tag{C.11}$$

$$F_0 = -2c + \alpha_2^2 V_{dd} + \alpha_2^4 V_{dd} L_\pi C_1 - \alpha_2^3(R_\pi C_1 V_{dd}), \tag{C.12}$$

$$\alpha_1 = \frac{\frac{R_\pi}{L_\pi} + \sqrt{\left(\frac{R_\pi}{L_\pi}\right)^2 - \frac{4.0}{L_\pi C_1}}}{2}, \tag{C.13}$$

$$\alpha_2 = \frac{\frac{R_\pi}{L_\pi} - \sqrt{\left(\frac{R_\pi}{L_\pi}\right)^2 - \frac{4.0}{L_\pi C_1}}}{2}, \tag{C.14}$$

$$A_1 = L_\pi C_1 b, \tag{C.15}$$

$$B_1 = L_\pi C_1 V_{C1t_x} - D_1 - E_1, \tag{C.16}$$

$$D_1 = \frac{D_2}{\alpha_1^2(\alpha_2 - \alpha_1)}, \tag{C.17}$$

$$E_1 = \frac{E_2}{\alpha_2^2(\alpha_1 - \alpha_2)} - \alpha_2 Fe^{-\alpha_2 t_x}, \tag{C.18}$$

$$D_2 = b - \alpha_1 a + \alpha_1^2(kL_\pi C_1 + R_\pi C_1 V_{C1t_x}) - \alpha_1^3 L_\pi C_1 V_{C1t_x}, \tag{C.19}$$

$$E_2 = b - \alpha_2 a + \alpha_2^2(kL_\pi C_1 + R_\pi C_1 V_{C1t_x}) - \alpha_2^3 L_\pi C_1 V_{C1t_x}, \tag{C.20}$$

$$k = \frac{1}{C_1 L_\pi}(At_x + B - \alpha_1 E e^{-\alpha_1 t_x}). \tag{C.21}$$

Equalizing the average current required to drive an effective capacitance $I_{Ceff-av}$ with the summation of I_{C1-av} and I_{C2-av}, the effective capacitance $C_{eff-RLC}$ can be expressed as

$$C_{eff-RLC} = C_2 + C_{x-RLC}, \tag{C.22}$$

where

$$C_{x-RLC} = \frac{t_D}{2ct_x(t_D - \frac{t_x}{2})} I_{c1_a v}. \tag{C.23}$$

Appendix D

Dependence of Delay on Line Inductance

The delay of a signal propagating through an interconnect line increases as the line inductance increases. The line inductance impedes the propagation of the signal through the line. This behavior can be described analytically by differentiating the delay expression (7.2) with respect to the line inductance. The sign of the resulting differentiated function describes whether the delay increases or decreases with inductance. A negative solution means that the delay decreases with an increase in the line inductance.

By differentiating (7.2), the range of line damping factor ζ at which the sign of the differentiation changes is obtained. The delay decreases with line inductance over the range at which the differentiation is negative. This condition is satisfied by the differentiation if

$$\zeta > \frac{2.8e-3}{{L_{line}}^{2.86}}. \tag{D.1}$$

The differentiation is negative when (D.1) is satisfied. A practical value of on-chip interconnect inductance is much less than 1 μH. Substituting $L_{line} =$ 1 μH into (D.1),

$$\zeta > 4X10^{14}. \tag{D.2}$$

In practical circuits, ζ is much less than $4X10^{14}$. The line propagation delay is an increasing function of line inductance as the differentiation is always positive in practical circuits.

Appendix E

Propagation Delay based on π_{21} Reduced Order Model

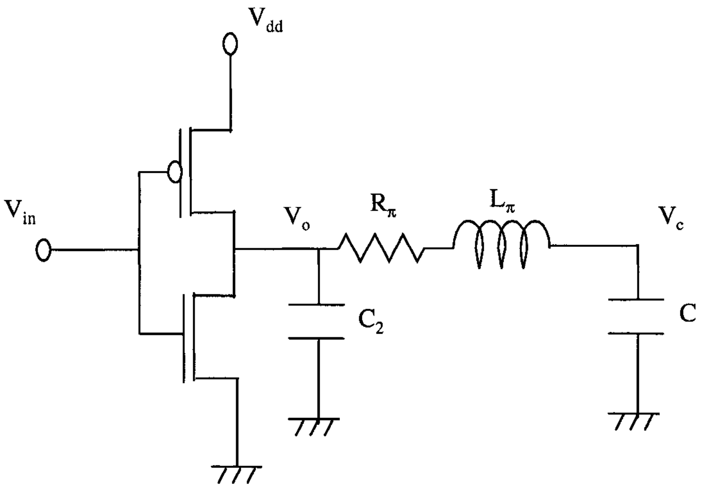

Figure E.1: CMOS inverter driving a π_{21} interconnect model

In order to determine an analytic solution for the propagation delay assuming the π_{21} model shown in Fig. E.1, an expression for the signal waveform across C during a high-to-low transition is

$$\begin{aligned} V_c(t) &= \frac{1}{C_2 C L_\pi}(A_2 e^{a(t-\tau_{nsat})} + B_2 e^{b(t-\tau_{nsat})} \\ &+ D_3 e^{d(t-\tau_{nsat})}), \end{aligned} \tag{E.1}$$

$$A_2 = \frac{\theta + CV_{c2}(aC_2 + \gamma_n)(R_\pi + aL_\pi)}{(a-b)(a-d)}, \tag{E.2}$$

$$B_2 = \frac{\theta + CV_{c2}(bC_2 + \gamma_n)(R_\pi + bL_\pi))}{(b-a)(b-d)}, \tag{E.3}$$

$$D_3 = \frac{\theta + CV_{c2}(dC_2 + \gamma_n)(R_\pi + dL_\pi)}{(d-a)(d-b)}, \tag{E.4}$$

$$\theta = C_2 V_{o2} + CV_{c2}, \tag{E.5}$$

$$C = C_1 + C_{Load}, \tag{E.6}$$

$$\gamma_n = \alpha B_n (V_{dd} - V_{tn})^{(n_n - m_n)}, \tag{E.7}$$

where α, B_n, n_n, and m_n are the nth power law transistor parameters [213]. a, b, and d are the roots of the polynomial,

$$x^3 + e_2 x^2 + e_1 x + e_0 = 0, \tag{E.8}$$

where

$$\begin{aligned} e_0 &= \frac{C_2CR_\pi + \gamma_n CL_\pi}{C_2CL_\pi}, & \text{(E.9)} \\ e_1 &= \frac{C + C_2 + CR_\pi\gamma_n}{C_2CL_\pi}, & \text{(E.10)} \\ e_2 &= \frac{\gamma_n}{C_2CL_\pi}. & \text{(E.11)} \end{aligned}$$

V_{o2} and V_{c2} are the voltage across C_2 and C, respectively, when the PMOS transistor of the driving inverter turns off. V_{o2} is

$$V_{o2} = K\left(\frac{\tau_{nsat}}{t_{rIn}}V_{dd} - V_{tn}\right)^{m_n}. \tag{E.12}$$

τ_{nsat} is determined by solving

$$V_o(\tau_{nsat}) - V_{DSSat} = 0, \tag{E.13}$$

where

$$V_{DSSat} = K(V_{in} - V_{tn})^{m_n}, \tag{E.14}$$

and K is an nth power law transistor parameter [213]. V_{c2} and $V_o(\tau_{nsat})$ are described in (E.30) and (E.31), respectively. The roots of (E.8) may contain complex roots. The voltage equation for the complex roots is

$$\begin{aligned} V_c(t) &= \frac{1}{CC_2L_\pi}((g_1\ cos\ l_1(t-\tau_{nsat}) + \frac{g_1h_1+f_1}{l_1}sin\ l_1(t-\tau_{nsat}))e^{h_1(t-\tau_{nsat})} \\ &+ D_4e^{d(t-\tau_{nsat})}), \end{aligned} \tag{E.15}$$

where

$$f_1 = \frac{D_4b_1 - h_3}{d}, \tag{E.16}$$

$$g_1 = \frac{D_4a_1 + f_1 - h_2}{d}, \tag{E.17}$$

$$h_1 = \frac{-a_1}{2}, \tag{E.18}$$

$$l_1 = \sqrt{{h_1}^2 + a_1h_1 + b_1}, \tag{E.19}$$

$$a_1 = -2r_1, \tag{E.20}$$

$$b_1 = {r_1}^2 + {I_1}^2, \tag{E.21}$$

$$h_2 = V_{c2}C(C_2R_\pi + L_\pi\gamma_n), \tag{E.22}$$

$$h_3 = \theta_2 + V_{c2}CR_\pi\gamma_n, \tag{E.23}$$

$$D_4 = \frac{\theta_2 + CV_{c2}(dC_2+\gamma_n)(R_\pi + dL_\pi)}{(d-a)(d-b)}, \tag{E.24}$$

$$r_1 = Rl\{a\}, \tag{E.25}$$

$$I_1 = Im\{a\}, \tag{E.26}$$

$$\theta_2 = C_2V_{o2} + CV_{c2}, \tag{E.27}$$

d is the real root and a and b are complex (conjugate) roots. The propagation delay can be determined by numerically solving the nonlinear equation (E.28) to determine $t_{50\%}$.

$$V_c(t_{50\%}) - \frac{V_{dd}}{2} = 0. \tag{E.28}$$

The propagation delay is

$$t_{pd} = t_{50\%} - \frac{t_{rIn}}{2}, \tag{E.29}$$

where t_{rIn} is the transition time of the input signal of the driving gate.

A Laplace transform is used to determined voltage expressions for $V_o(\tau_{nsat})$ and V_{c2}.

$$V_{c2} = \frac{B_d}{2}(\tau_{nsat} - \tau_n)^2 + D_d(\tau_{nsat} - \tau_n) + E_d + F_d e^{-\alpha_3(\tau_{nsat}-\tau_n)} + G_d e^{-\alpha_4(\tau_{nsat}-\tau_n)}, \tag{E.30}$$

$$\begin{aligned} V_o(\tau_{nsat}) &= V_{dd} - \frac{1}{C_2}\Big[\frac{q_d}{2}(\tau_{nsat} - \tau_n)^2 + C\frac{B_d}{2}(\tau_{nsat} - \tau_n)^2 + D_d(\tau_{nsat} - \tau_n) \\ &+ F_d e^{(-\alpha_3(\tau_{nsat}-\tau_n)-1)} + G_d e^{(-\alpha_4(\tau_{nsat}-\tau_n)-1)}\Big], \end{aligned} \tag{E.31}$$

where

$$
\begin{aligned}
B_d &= \frac{-q_d}{L_\pi C_2 C \alpha_{34}}, && \text{(E.32)}\\
D_d &= -B_d \frac{\alpha_{3pls4}}{\alpha_{34}}, && \text{(E.33)}\\
F_d &= \frac{-\theta_1 {\alpha_3}^2 - q_d + {\alpha_3}^3 C_2 C V_{dd}(R_\pi - \alpha_3 L_\pi)}{L_\pi C_2 C \alpha_3^3(\alpha_4 - \alpha_3)}, && \text{(E.34)}\\
G_d &= \frac{-\theta_1 {\alpha_4}^2 - q_d + {\alpha_4}^3 C_2 C V_{dd}(R_\pi - \alpha_4 L_\pi)}{L_\pi C_2 C \alpha_4^3(\alpha_3 - \alpha_4)}, && \text{(E.35)}\\
E_d &= V_{dd} - F_d - G_d, && \text{(E.36)}\\
q_d &= (B_n K - B_p)\frac{V_{dd}}{t_{rIn}} && \text{(E.37)}\\
\theta_1 &= V_{dd}(C_2 + C), && \text{(E.38)}\\
\alpha_{34} &= \alpha_3\,\alpha_4, && \text{(E.39)}\\
\alpha_{3pls4} &= \alpha_3 + \alpha_4, && \text{(E.40)}\\
\alpha_3 &= \frac{\frac{R_\pi}{L_\pi} + \sqrt{(\frac{R_\pi}{L_\pi})^2 - 4\beta}}{2}, && \text{(E.41)}\\
\alpha_4 &= \frac{\frac{R_\pi}{L_\pi} - \sqrt{(\frac{R_\pi}{L_\pi})^2 - 4\beta}}{2}, && \text{(E.42)}\\
\tau_n &= t_{rIn}\frac{V_{tn}}{V_{dd}} && \text{(E.43)}\\
\beta &= \frac{(C_2 + C)}{(L_\pi C_2 C)}, && \text{(E.44)}
\end{aligned}
$$

and B_p is an nth power law transistor parameter [213]. α_3 and α_4 can be complex conjugate poles. For complex poles,

$$\begin{aligned} V_{c2} &= \frac{B_d}{2}(\tau_{nsat}-\tau_n)^2 + D_d(\tau_{nsat}-\tau_n) + E_d \\ &+ (G_2 cos\ l_2(\tau_{nsat}-\tau_n) + F_3 sin\ l_2(\tau_{nsat}-\tau_n))e^{h_4(\tau_{nsat}-\tau_n)}, \end{aligned} \tag{E.45}$$

$$\begin{aligned} V_o(\tau_{nsat}) &= V_{dd} - \frac{1}{C_2}[\frac{q_d}{2}(\tau_{nsat}-\tau_n)^2 + C\frac{B_d}{2}(\tau_{nsat}-\tau_n)^2 + D_d(\tau_{nsat}-\tau_n) \\ &+ (G_2(cos\ l_2(\tau_{nsat}-\tau_n) - 1) \\ &+ F_3 sin\ l_2(\tau_{nsat}-\tau_n))e^{h_4(\tau_{nsat}-\tau_n)}] \end{aligned} \tag{E.46}$$

where

$$F_3 = \frac{G_2 h_4 + F_2}{l_2}, \tag{E.47}$$

$$G_2 = G_d + F_d, \tag{E.48}$$

$$F_2 = F_d \alpha_4 + G_d \alpha_3, \tag{E.49}$$

$$l_2 = \sqrt{{h_4}^2 + a_2 h_4 + b_2}, \tag{E.50}$$

$$h_4 = \frac{-a_2}{2}, \tag{E.51}$$

$$a_2 = 2r_2, \tag{E.52}$$

$$b_2 = {r_2}^2 + {I_2}^2, \tag{E.53}$$

$$r_2 = Rl\{\alpha_3\}, \tag{E.54}$$

$$I_2 = Im\{\alpha_3\}. \tag{E.55}$$

Appendix F

Impedance Parameters of Tapered *RLC* Interconnect

Practically, implementing a continuously shaped line is not precisely possible. However, dividing the line into sections of length $l_1 = \frac{l}{n}$, where n is the number of sections, effectively approximates a continuous shape. As shown in Fig. G.1, the width of the line sections decreases exponentially as the section approaches the far end, producing the optimum shape. For specific geometric dimensions of the signal line and shield lines, the line impedance parameters of the line are expressed as functions of the tapering parameters, q and p.

Expressing the line inductance in terms of the dimensions of the wire structure requires that the current return path be determined. In the coplanar structure shown in Fig. G.1, the return path is assumed to be in the adjacent ground lines. This shield structure is common in important global interconnects such as clock distribution networks or data busses [216]-[230].

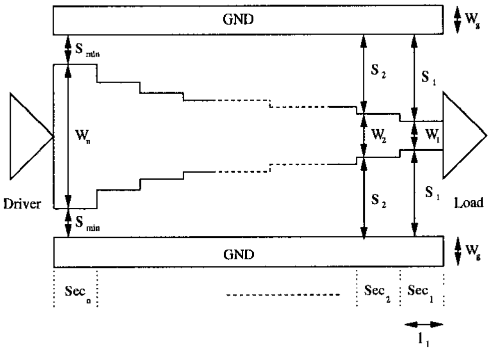

Figure F.1: Coplanar tapered line

For a small number of line sections n, the section length is much larger than the other physical dimensions (such as the section width W_i, the separation between the section and the ground S_i, and the line thickness T). Tapering is more effective in long (global) lines (*e.g.*, $l > 1000$ μm) since the line inductance and resistance are significant. These lines are divided into several sections (*e.g.*, $n < 20$), making the ratio between the section length and the other dimensions large (*e.g.*, $\frac{l_1}{W_i, S_i, T} > 100$). Neglecting skin and proximity effects [?] and for $l_1 \gg S_i, W_i$, and T, the line inductance is

$$\begin{aligned} L_{line}(q,p) &= L_1 \Bigg[n \left(A + \frac{3}{2} B(q,p) \right) \\ &+ \frac{0.22}{l_1} \sum_{i=1}^{n} \frac{1}{W_i(q,p)} - ln \left(\prod_{i=1}^{n} (q e^{(i-1)pl_1} + T) \right) \Bigg], \end{aligned} \tag{F.1}$$

where

$$L_1 = \frac{\mu_0 l_1}{2\pi}, \tag{F.2}$$

$$A = 0.8637 - 0.5ln(W_g + T) + \frac{0.11}{(W_g + 3T)}, \tag{F.3}$$

$$B(q,p) = lnSW_g(q,p) - \frac{SW_g(q,p)}{l_1}, \tag{F.4}$$

$$SW_g(q,p) = 2S_{min} + W_g + qe^{(n-1)pl_1}. \tag{F.5}$$

The width of each line section is

$$W_i(q,p) = \begin{cases} W_{i-1}e^{pl_1} & \text{for i > 1 ,} \\ q & \text{for i = 1 .} \end{cases} \tag{F.6}$$

The inductance of an exponentially tapered line is determined from (F.1) and compared with the inductance extracted by the field solver FastHenry [84]. The error between the two solutions is less than 0.78% for a tapering factor ranging from 0 to 0.8 mm^{-1}.

The total line resistance is

$$R_{line}(q,p) = R_D l_1 \sum_{i=1}^{n} \frac{1}{W_i(q,p)}, \tag{F.7}$$

where R_D is the line resistance per square. The total line capacitance is

$$C_{line}(q,p) = l_1 \sum_{i=1}^{n} C_{Seci}, \tag{F.8}$$

where C_{Seci} is the capacitance of each section i per unit length. A closed form expression for C_{Seci} in terms of $W_i(q,p)$ and $S_i(q,p) = S_{min} + \frac{(W_n - W_i(q,p))}{2}$ is obtained from [140].

Appendix G

Practical Implementation of Exponential Tapering

Implementing a continuously shaped line is not precisely possible. Dividing a line into sections of length l_1, however, can achieve an effective approximation of a continuous shape. As shown in Fig. G.1, the width of the line sections decreases exponentially as the section approaches the far end. For an exponentially tapered interconnect line, the line width satisfies the relation,

$$W_i = W_N e^{-pl_1(N-i)} \ for 1 \leq i \leq N, \tag{G.1}$$

where W_N is the line width at the near end of the line, N is the number of sections, $l_1 = \frac{l}{N}$, and p is the tapering factor.

The number of sections determines the precision of the exponential tapering factor. Using a large number of sections may not increase the precision of the tapering since the minimum line width of a specific technology limits

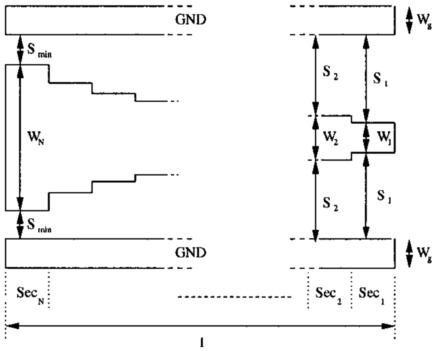
GND
S_{min}
W_N
S_{min}
GND
W_g
S_2
S_1
W_2
W_1
S_2
S_1
W_g
Sec_N
Sec_2
Sec_1
l

Figure G.1: Coplanar exponentially tapered interconnect

the precision. N should satisfy

$$\Delta W < W_{min}\left[e^{pl_{min}(1-\frac{1}{N})} - e^{pl_{min}(1-\frac{2}{N})}\right], \tag{G.2}$$

where l_{min} is the shortest line in the tree, W_{min} is the minimum wire width, and ΔW is the technology dependent precision of the wire width. Closed form expressions for the line impedance parameters (resistance, inductance, and capacitance) are provided in [214].

Appendix H

Pseudocode for the C Program of the Optimum Tapered Lines using First Order Approximation

The pseudocode for the C program which determines the optimum initial interconnect width and tapering factor for minimum power dissipation while maintaining the signal characteristics using the first order approximation is as follows

```
 SumRC_Original = SumRC_Org() ;
C_Original = C_Org() ;
     for each possible $W_{init}$ do
        for each possible $p$ do
         if $W_1 > W_{min}$ then
        SumRC_Taper = SumRC_Taper() ;
```

```
      C_Taper = C_Taper() ;
        if SumRC_Taper $\leq$ SumRC_Original then
          C_Possible = C_Taper ;
        endif
      endif
    endfor
  endfor
C_Min = FindMinC() ;
```

Appendix I

Pseudocode for the C Program of the Optimum Tapered Lines using Second Order Approximation

The pseudocode for the C program which determines the optimum initial interconnect width and tapering factor for minimum power dissipation while maintaining the signal characteristics using the second moment approximation is as follows

```
 m_2-Original = m_2-Org() ;
C_Original = C_Org() ;
    for each possible $W_{init}$ do
        for each possible $p$ do
         if $W_1 > W_{min}$ then
         m_2-Taper = m_2-Taper() ;
        C_Taper = C_Taper() ;
          if m_2-Taper $\leq$ m_2-Original then
           C_Possible = C_Taper ;
            endif
          endif
         endfor
        endfor
C_Min = FindMinC() ;
```

Publications

Book Chapters

1. M. A. El-Moursy and E. G. Friedman, "Design Methodologies for On-Chip Inductive Interconnect," *Interconnect-Centric Design for Advanced SoC and NoC*, J. Nurmi, J. Isoaho, and A. Jantsch (Eds.), Norwell, Massachusetts: Kluwer Academic Publishers, Chapter 4, 2004 (in Press).

2. M. A. El-Moursy and E. G. Friedman, "Optimizing Inductive Interconnect for Low Power," *System-on-Chip for Real-Time Applications*, W. Badawy and G. A. Jullien (Eds.), Norwell, Massachusetts: Kluwer Academic Publishers, Section 9.2, pp. 380-391, 2003.

Journal Papers

1. M. A. El-Moursy and E. G. Friedman, "Wire Shaping of *RLC* Interconnects," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* (in Review).

2. M. A. El-Moursy and E. G. Friedman, "Exponentially Tapered H-Tree Clock Distribution Networks," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* (in Review).

3. M. A. El-Moursy and E. G. Friedman, "Shielding Effect of On-Chip Interconnect Inductance," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 12, No. 10, October 2004.

4. M. A. El-Moursy and E. G. Friedman, "Optimum Wire Sizing of *RLC* Interconnect With Repeaters," *Integration, the VLSI Journal* (in Press).

5. M. A. El-Moursy and E. G. Friedman, "Resistive Power in CMOS Circuits," *Analog Integrated Circuits and Signal Processing* (in Press).

6. M. A. El-Moursy and E. G. Friedman, "Power Characteristics of Inductive Interconnect," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 12, No. 10, October 2004.

7. M. A. El-Moursy and E. G. Friedman, "Optimizing Inductive Interconnect for Low Power," *Canadian Journal of Electrical and Computer Engineering*, Vol. 27, No. 4, pp. 183-187, October 2002.

Refereed Conference Papers

1. M. A. El-Moursy and E. G. Friedman, "Optimum Wire Tapering for Minimum Power Dissipation of RLC Interconnects," *Proceedings of the IEEE International Symposium on Circuits and Systems*, (in Submission).

2. M. A. El-Moursy and E. G. Friedman, "Exponentially Tapered H-Tree Clock Distribution Networks," *Proceedings of the IEEE International Symposium on Circuits and Systems*, Vol. II, pp. 601-604, May 2004.

3. M. A. El-Moursy and E. G. Friedman, "Optimum Wire Shaping of an *RLC* Interconnect," *Proceedings of the IEEE Midwest Symposium on Circuits and Systems*, December 2003.

4. M. A. El-Moursy and E. G. Friedman, "Resistive Power in CMOS Circuits," *Proceedings of the IEEE Midwest Symposium on Circuits and Systems*, December 2003.

5. M. A. El-Moursy, M. Margala, A. El-Moursy, J. Zhang, and W. Heinzelman, "1-V ADPCM Processor for Low-Power Wireless Applications," *Proceedings of the IFIP International Conference on Very Large Scale Integration*, December 2003.

6. M. A. El-Moursy and E. G. Friedman, "Power Characteristics of Inductive Interconnect," *Proceedings of the IEEE International Conference on Electronics, Circuits, and Systems*, December 2003.

7. M. A. El-Moursy and E. G. Friedman, "Inductive Interconnect Width Optimization For Low Power,' *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 5.273- 5.276 May 2003.

8. M. A. El-Moursy and E. G. Friedman, "Optimum Wire Sizing of *RLC* Interconnect With Repeaters," *Proceedings of the IEEE Great Lakes Symposium on VLSI*, pp. 27-32, April 2003.

9. M. A. El-Moursy and E. G. Friedman, "Shielding Effect of On-Chip Interconnect Inductance," *Proceedings of the IEEE Great Lakes Symposium on VLSI*, pp. 165-170, April 2003.

10. M. A. El-Moursy and E. G. Friedman, "Optimum Wire Sizing and Repeater Insertion in Distributed *RLC* Interconnect," *Proceedings of the 26th Annual IEEE EDS/CAS Activities in Western New York Conference*, pp. 6, November 2002.

11. M. A. El-Moursy and E. G. Friedman, "Optimizing Inductive Interconnect for Low Power," *Proceedings of the International Workshop on System-on-Chip for Real-Time Applications*, pp. 206-216, July 2002.

12. M. A. El-Moursy, T. M. Kamel, and H. M. El-Sayed, "Admission Control and Scheduling of Traffic on ATM Switches: Performance Analysis," *Proceedings of SPIE: Asia-Pacific Optical and Wireless Communications*, Vol. 4584, pp. 161-176, November 2001.