Memristors – Not Just Memory

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Abstract

Over the past years, new memory technologies such as RRAM, STT-MRAM, PCM *etc.*, have emerged. These technologies, located in the metal layers of the chip, are relatively fast, dense, and power-efficient and can be considered as *memristors*. Usually, the use of these devices has been limited to flash, DRAM, and SRAM replacement.

This talk is focused on different uses of memristors. For example, memristors can be used as new memory structures, different than the conventional memory hierarchy, opening opportunity to a new era in computer architecture – the era of *Memory Intensive Computing* [1]. An example of a novel memory structure is the Multistate Pipeline Register (MPR) that is used to store multiple states of different threads. MPR enables new microarchitectures such as Continuous Flow Multithreading (CFMT) [2], significantly enhancing performance while reducing energy.

Memristors can also be integrated with CMOS in logic circuits. An example to a hybrid CMOS-memristor logic gates is Memristor Ratioed Logic (MRL) [3], where memristor-based AND and OR logic gates are integrated with CMOS inverters to perform complete logic structure. MRL can further extend CMOS technology.

Alternatively, memristors can be used as a stand-alone logic, suitable to perform logic within the memory and provide opportunity for new computer architectures, different than classical von Neumann. Examples to logic within the memory are memristor-based material implication [4, 5] and Memristor Aided Logic (MAGIC).

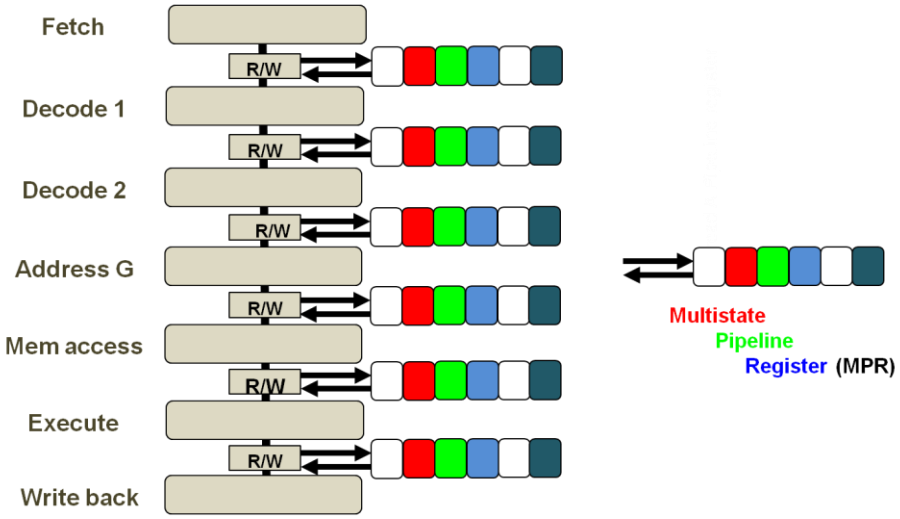

Figure 1. Example of a Continuous Flow Multithreading processor. Instead of conventional pipeline registers, a memristor-based Multistate Pipeline Register is used, eliminating the need to flush the pipeline.

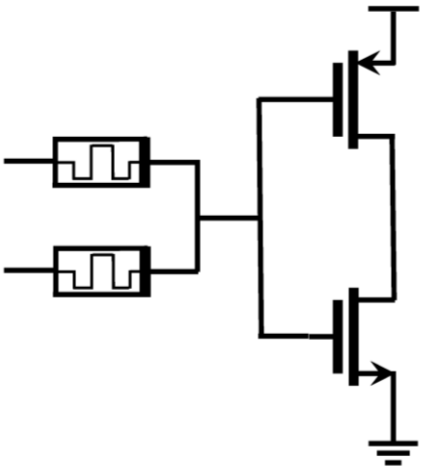

Figure 2. A Memristor Ratioed Logic NAND. The gate consists of memristor-based AND and a CMOS inverter.

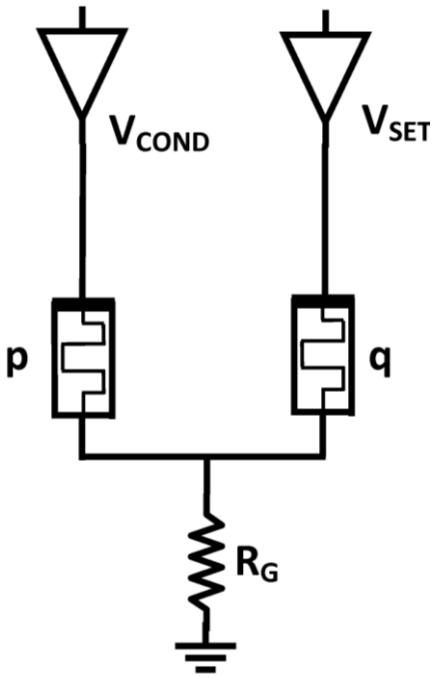

Figure 3. A memristor-based material implication (IMPLY) logic gate.

References

[1] U. Weiser, "Memory Intensive Computing," ISCA 2013 keynote, June 2013.

[2] S. Kvatinsky, Y. H. Nacson, Y. Etsion, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Memristor-based Multithreading," *IEEE Computer Architecture Letters*, 2013 (in press).

[3] S. Kvatinsky, N. Wald, G. Satat, E. G. Friedman, A. Kolodny, and U. C. Weiser, "MRL – Memristor Ratioed Logic," *Proceedings of the International Cellular Nanoscale Networks and their Applications*, pp. 1-6, August 2012.

[4] S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Memristor-based IMPLY Logic Design Flow," *Proceedings of the IEEE International Conference on Computer Design*, pp.142-147, October 2011.

[5] S. Kvatinsky, N. Wald, G. Satat, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Memristor-based Material Implication (IMPLY) Logic: Design Principles and Methodologies," *IEEE Transactions on Very Large Scale Integration (VLSI)*, 2013 (in press).