Microelectronics Journal 43 (2012) 235–243

Contents lists available at SciVerse ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

Multi-aggressor capacitive and inductive coupling noise modeling and mitigation

Victoria Vishnyakov [a,*], Eby G. Friedman [b], Avinoam Kolodny [a]

[a] Electrical Engineering Department, Technion, Haifa, Israel
[b] Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY 14627, USA

ARTICLE INFO

Article history:
Received 24 May 2011
Received in revised form
4 December 2011
Accepted 16 December 2011
Available online 31 January 2012

Keywords:
Crosstalk
Inductive coupling
Multi-aggressor
Modeling
Resistance–inductance–capacitance (RLC) interconnect
On-chip global interconnect

ABSTRACT

Crosstalk noise in on-chip interconnect plays a major role in the performance of modern integrated circuits. Multi-aggressor capacitive and inductive coupling complicates both the modeling and mitigation of the noise. A novel method to model and analyze noise in RLC multi-line structures is proposed in this paper, exhibiting an error of up to 9% as compared to SPICE. This method is physically intuitive since it decomposes the noise produced by each of the aggressors into individual capacitive and inductive noise sources. The proposed model and related layout noise mitigation guidelines are applied to crosstalk noise reduction in multi-line structures.

1. Introduction

Global and semi-global interconnect do not scale with feature size due to increased design complexity, demand for greater integration, and technology constraints. As technology progresses, the effect of the interconnect on the performance of high speed and high density integrated circuits has greatly increased. With shorter transition times and the inability to scale the global wires, inductive effects exhibited in the upper metal layers cannot be neglected. Consequently, long range inductive coupling should be included with the already significant capacitive coupling in global interconnect lines since noise analysis and mitigation is not limited to only the nearest neighbors. Simultaneous capacitive and inductive coupling together with multiple aggressors are significant risks to the signal integrity of the global interconnects.

The primary interconnect structures in the upper metal layers are the clock and power/ground (P/G) distribution networks and wide data busses. The global clock network is usually highly shielded and affected by the self-inductance rather than mutual inductive effects, which greatly simplifies the analysis and optimization process. In P/G networks, the noise is caused by both the self-inductance and mutual inductance. These networks however generally exhibit uniform structures. Random data signals, unshielded clock signals, and wide data busses, as illustrated in Fig. 1, suffer from both self-inductance and mutual inductive coupling and can be affected by numerous aggressors due to the long range nature of inductive coupling. Simultaneous capacitive and inductive coupling and different switching patterns further complicate the modeling and analysis process.

Several authors have addressed modeling and behavioral analysis of noise in multi-line structures in the presence of inductance. In [1], a two line decoupling technique is extended by applying superposition of the fundamental modes to three lines and proposes this technique for N coupled lines. The model is rather general (no limitations on the line parameters) but is complex and requires adjustment for different bus sizes. The use of modal analysis to decouple multiple transmission line (TL) systems is described in [2,3]. These models are valid for identical lines with an identical driver and loads assuming ideal transmission lines and are computationally complex. A TL based model is used in [4], but assumes no capacitive coupling and low loss, which is also assumed in [5]. The TWA method [6] is extended to multi-coupled transmission lines in [7]. The concept of an effective switching factor for multi-line systems is presented in [8] and the differences between multi-line worst case noise patterns for RC and RLC lines are discussed in [9].

These models do not describe the individual noise components—the noise caused by each aggressor and the noise due to both

* Corresponding author. Tel.: +972 544792175
E-mail address: vita.vishnyakov@gmail.com (V. Vishnyakov).

0026-2692/$ - see front matter © 2012 Elsevier Ltd. All rights reserved.
doi:10.1016/j.mejo.2011.12.007

capacitive and inductive coupling. Since methods to mitigate each noise source (inductive, capacitive, different aggressors) can be different and sometimes contradictory, identification of the most critical noise sources and the preferable mitigation method for a specific physical layout and switching pattern are necessary. The conditions and methods to model noise as a combination of the noise caused by each aggressor and noise source (capacitive and inductive), as illustrated in Fig. 2, are described in this paper based on the additivity properties of capacitive and inductive coupling as well as multi-line system behavior in the presence of multiple noise sources.

The paper is organized as follows. In Section 2, the additivity properties of inductive and capacitive noise for a two line coupled system with simultaneous inductive and capacitive coupling are examined. Conditions under which the additivity of the two coupling noise sources can be applied are formulated. The behavior of multi-line systems is examined in the presence of capacitive coupling, inductive coupling, and simultaneous capacitive and inductive coupling in Section 3. The conditions which represent the sum of the noise caused by each aggressor are also described. In Section 4, noise models of multi-line systems are described. In Section 5, layout-based noise mitigation guidelines are presented and together with the proposed models can be used to reduce noise in multi-line systems. The results are summarized in Section 6.

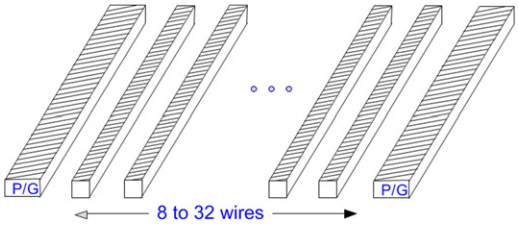

Fig. 1. Typical upper metal routing structure.

2. Additivity of capacitive and inductive coupling noise

Simultaneous capacitive and inductive coupling can occur between adjacent RLC lines. According to [10], capacitive and inductive coupling noise is additive under the low loss approximation, $R_{line} \gg (L_{self}-M)\omega$, where R_{line} and L_{self} are, respectively, the self-resistance and inductance of a line, M is the mutual inductance between the lines, and ω is the switching frequency, $\omega=2/t_r$, where t_r is the signal transition time. Note however that the low loss approximation cannot always be assumed in modern integrated circuits. Therefore, additivity of the two noise sources cannot be assumed in modern integrated circuits. By performing an analysis similar to [10], those regimes where additivity of capacitive and inductive coupling can be assumed, as illustrated in Fig. 3 for a two coupled line system, are established. The additivity property permits the noise components to be broken into noise sources. As a result, the dominant noise source can be identified and a suitable noise mitigation technique can be chosen. This distinction is important since noise reduction techniques for inductive and capacitive coupling are not only different, but often in conflict.

According to transmission line theory [18], coupled lines exhibit two modes of propagation with two different propagation constants and two different line impedances. The even mode represents the case of same direction switching and the odd mode represents opposite direction switching. Any signal in the system can be expressed as the sum of these modes. The characteristic impedance of the even and odd modes for two identical lines is presented in Eqs. (2.1) and (2.2) where R_{11}, C_{11}, and L_{11} are,

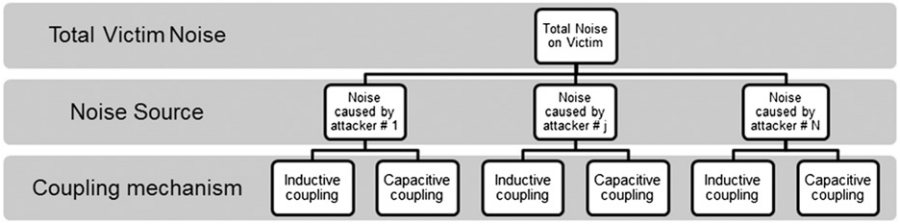

Fig. 2. Types of noise sources and mechanisms.

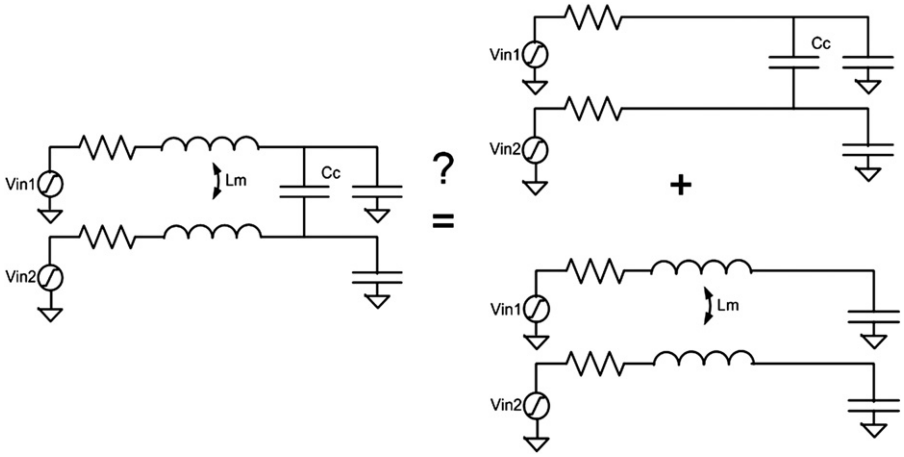

Fig. 3. Decoupling capacitive and inductive noise using additivity.

respectively, the resistance, capacitance, and inductance of the line, and C_{12} and L_{12} are, respectively, the mutual capacitance and inductance. ω is the switching frequency, defined by $\omega \equiv 2/t_r$, where t_r is the signal transition time.

$$Z_{RLC}(even) = \sqrt{\frac{R_{11} + j(L_{11} + L_{12})\omega}{jC_{11}\omega}} \tag{2.1}$$

$$Z_{RLC}(odd) = \sqrt{\frac{R_{11} + j(L_{11} - L_{12})\omega}{j(C_{11} + 2C_{12})\omega}} \tag{2.2}$$

Note that the characteristic impedance of the even mode is not dependent on the capacitive coupling between the lines (C_{12}), and is the same as the characteristic impedance of a system without capacitive coupling

$$Z_{RLC}(even, C_{12} \neq 0) = Z_{RLC}(even, C_{12} = 0) \tag{2.3}$$

Thus, when the lines switch in the same direction, capacitive coupling between the lines does not affect the signal propagation characteristics. The odd mode characteristic impedance, however, is the same as that of a system with no inductive coupling only if the dependence of the impedance on inductive effects can be neglected

$$R_{11} \gg (L_{11} - L_{12})\omega \tag{2.4}$$

In this case

$$Z_{RLC}(odd, L_{12} \neq 0) = Z_{RC}(odd) \tag{2.5}$$

where $Z_{RC}(odd)$ is the impedance of two coupled lines with $L_{11} = L_{12} = 0$. When both Eqs. (2.3) and (2.5) are assumed, the total noise can be expressed as the sum of the noise caused by inductive coupling and the noise caused by capacitive coupling, as shown in (2.6)

$$Vnoise(Total) = Vnoise(even, C_{12} = 0) + Vnoise(odd, L_{11} = L_{12} = 0) \tag{2.6}$$

When inductive coupling is strong ($L_{11} \approx L_{12}$), Eq. (2.4) is satisfied. Another case where Eq. (2.4) is satisfied is the low loss approximation [4,10]. This approximation, however, is not always appropriate in modern semiconductor processes. Another condition that supports approximating the noise as the sum of the inductive and capacitive coupling is weak capacitive coupling, i.e., $C_{12} \ll C_{11}$, or same direction switching. In this case, most of the noise is due to inductive coupling, and $Vnoise(odd)$ is small or non-existent and can be neglected. To summarize, there are three conditions in which additivity of inductive and capacitive coupling can be assumed

1. $R_{11} \gg (L_{11} - L_{12})\omega$—low loss approximation,
2. $L_{11} \approx L_{12}$—strong inductive coupling case,
3. $C_{12} \ll C_{11}$—weak capacitive coupling or same direction switching.

3. Coupling noise in multi-line structures

Capacitive coupling, inductive coupling, and simultaneous inductive and capacitive coupling exhibit different behavior in multi-line structures (see Fig. 4). While capacitive coupling primarily exists between nearest neighbors, inductive coupling is a long range phenomenon and can affect distant wires as well. Furthermore, it is shown in this section that while both capacitive and inductive coupling noise can be expressed as the sum of the noise caused by each aggressor, for simultaneous capacitive and inductive coupling, this is not the case. The ability to separate the noise caused by each aggressor is however important for noise analysis and mitigation. Therefore, in this section, those conditions that express the total noise as the sum of the noise caused by each aggressor are described.

3.1. Inductive coupling in multi-line structures

Capacitive coupling noise (see Fig. 4a) is caused primarily by nearby neighbors and can be expressed as the sum of the noise caused by each of the adjacent aggressors. Inductive coupling, however, is a long range effect, thus non-adjacent neighbors can also couple noise and cannot be neglected. In multi-line structures, inductive coupling among all of the lines may occur (see Fig. 4b).

To analyze inductive coupling noise in multi-line systems, the lines are represented as a lumped RLC model, as described in Eq. (3.1.1), where $V_{in,i}$, R_i, C_i, and L_i are, respectively, the input waveform, resistance, self-capacitance, and self-inductance of each line and M_{ij} is the mutual inductance between lines i and j.

$$V'_{in,i} = R_i * I'_i + L_i * I''_i + \sum_{i \neq j} M_{ij} * I''_j + \frac{1}{C_i} * I_i \tag{3.1.1}$$

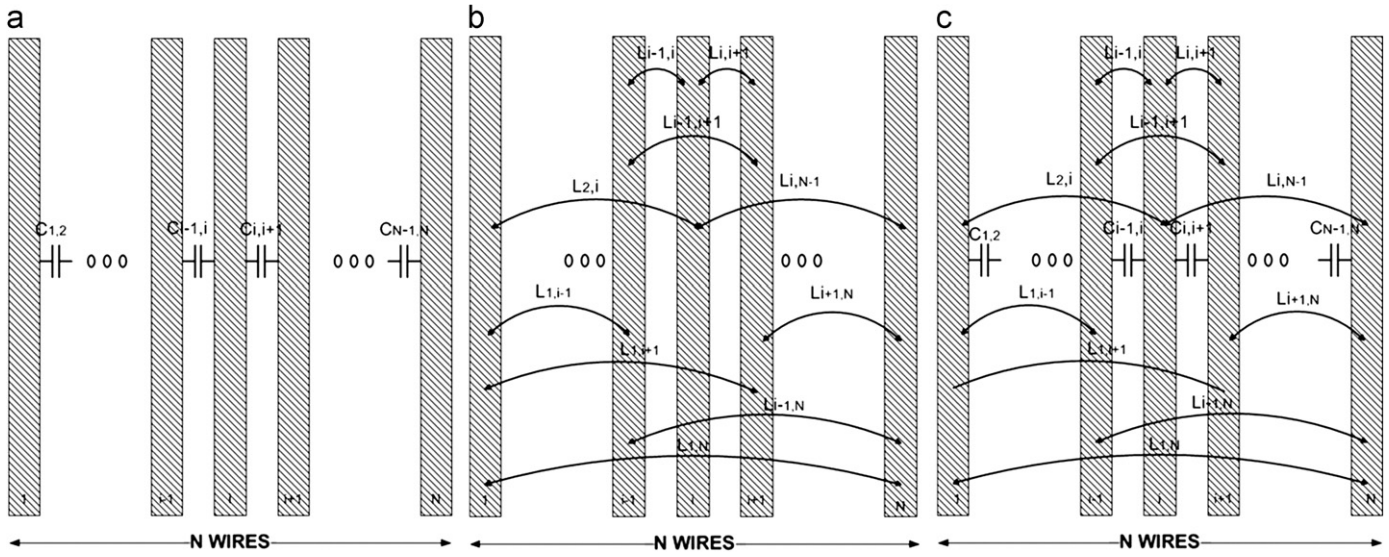

Fig. 4. N coupled lines: (a) capacitive coupling only, (b) inductive coupling only, and (c) capacitive and inductive coupling.

The matrix representation of Eq. (3.1.1) is

$$\begin{bmatrix} V'_{in,1} \\ \vdots \\ V'_{in,i} \\ \vdots \\ V'_{in,N} \end{bmatrix} = \begin{bmatrix} \frac{1}{C_1}+R_1*\frac{d}{dt}+L_1*\frac{d^2}{dt^2} & \cdots & M_{1,j}*\frac{d^2}{dt^2} & \cdots & M_{1,N}*\frac{d^2}{dt^2} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ M_{i,1}*\frac{d^2}{dt^2} & \cdots & \frac{1}{C_i}+R_i*\frac{d}{dt}+L_i*\frac{d^2}{dt^2} & \cdots & M_{i,N}*\frac{d^2}{dt^2} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ M_{N,1}*\frac{d^2}{dt^2} & \cdots & M_{N,j}*\frac{d^2}{dt^2} & \cdots & \frac{1}{C_N}+R_N*\frac{d}{dt}+L_N*\frac{d^2}{dt^2} \end{bmatrix}$$

$$*\begin{bmatrix} I_1 \\ \vdots \\ I_i \\ \vdots \\ I_N \end{bmatrix} = Vin'_{1XN} = A_{NXN}*Iin_{1XN} \tag{3.1.2}$$

The current per line can be expressed as a function of the input switching pattern by inverting A_{NXN}, as shown in Eq. (3.1.3)

$$I_{1XN} = [A_{NXN}]^{-1}*Vin'_{1XN} \tag{3.1.3}$$

By extending Eq. (3.1.3) and assuming $V_{in,i'}=0$ for the non-switching neighbors, it can be observed that the solution for multiple switching aggressors is the sum of the individual solutions with each aggressor switching, as described by Eq. (3.1.4).

$$\begin{bmatrix} I_1 \\ \vdots \\ I_i \\ \vdots \\ I_N \end{bmatrix} = \left[A^{-1}\right]*\begin{bmatrix} V'_{in,1} \\ \vdots \\ V'_{in,i} \\ \vdots \\ V'_{in,N} \end{bmatrix} = \left[A^{-1}\right]*\begin{bmatrix} V'_{in,1} \\ \vdots \\ 0 \\ \vdots \\ 0 \end{bmatrix} + \cdots + \left[A^{-1}\right]*\begin{bmatrix} 0 \\ \vdots \\ V'_{in,i} \\ \vdots \\ 0 \end{bmatrix}$$

$$+ \cdots + \left[A^{-1}\right]*\begin{bmatrix} 0 \\ \vdots \\ 0 \\ \vdots \\ V'_{in,N} \end{bmatrix} \tag{3.1.4}$$

The current per line can be determined by solving Eq. (3.1.2), which can be rewritten in the following form:

$$\begin{bmatrix} L_1 & \cdots & M_{1,j} & \cdots & M_{1,N} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ M_{i,1} & \cdots & L_i & \cdots & M_{i,N} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ M_{N,1} & \cdots & M_{N,j} & \cdots & L_N \end{bmatrix} *\begin{bmatrix} I''_1 \\ \vdots \\ I''_i \\ \vdots \\ I''_N \end{bmatrix} + \begin{bmatrix} R_1 & \cdots & 0 & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & \cdots & R_i & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & \cdots & 0 & \cdots & R_N \end{bmatrix}$$

$$*\begin{bmatrix} I'_1 \\ \vdots \\ I'_i \\ \vdots \\ I'_N \end{bmatrix} + \begin{bmatrix} \frac{1}{C_1} & \cdots & 0 & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & \cdots & \frac{1}{C_i} & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & \cdots & 0 & \cdots & \frac{1}{C_N} \end{bmatrix} *\begin{bmatrix} I_1 \\ \vdots \\ I_i \\ \vdots \\ I_N \end{bmatrix} = \begin{bmatrix} V'_{in,1} \\ \vdots \\ V'_{in,i} \\ \vdots \\ V'_{in,N} \end{bmatrix}$$

$$= L*I'' + R*I' + C^{-1}*I = V \tag{3.1.5}$$

where L, R, and C are, respectively, $N\times N$ matrices of the inductance, resistance, and capacitance, V is an $N\times 1$ vector of the derivative of the input voltages $V'_{in,i}$, and I is the $N\times 1$ vector of the currents. Expression (3.1.5) is a second order differential equation with a well known solution, as presented in Eq. (3.1.6), where y_0 and y_1 are determined by the boundary conditions and α, ω_0, and ω_d are described, respectively, in Eqs. (3.1.7)–(3.1.9).

$$I(t) = \begin{cases} V*C*\left[1-e^{-\alpha t}\left(\frac{\alpha}{\alpha_d}*\sinh(\alpha_d t)+\cosh(\alpha_d t)\right)\right] t < Tr \\ \frac{e^{-\alpha t}}{\alpha_d}\left[(y_1+y_0\alpha)*\sinh(\alpha_d t)+y_0\alpha_d\cosh(\alpha_d t)\right] t > Tr \end{cases} \tag{3.1.6}$$

$$\alpha = 0.5*R*L_{ij}^{-1} \tag{3.1.7}$$

$${\omega_0}^2 = L_{ij}^{-1}C^{-1} \tag{3.1.8}$$

$$\alpha_d = \sqrt{\alpha^2-{\omega_0}^2} \tag{3.1.9}$$

From the form of the solution of Eq. (3.1.6), the noise on each line is the sum of the noise caused by each aggressor, since, for non-switching aggressors, $V(i)=V'_{in,i}=0$.

3.2. Simultaneous capacitive and inductive coupling

When only one coupling effect exists (inductive or capacitive), the total noise for any switching pattern is the sum of the noise caused by each aggressor, as described in Section 3.1. In a multi-line structure, capacitive noise will couple to the nearest neighbors and inductive noise may couple among all of the lines (Fig. 4c). Therefore, for a given victim, interactions with the nearest aggressors will be both capacitive and inductive, and, with the more distant lines, inductive noise will be the primary source of coupling. However, the farther lines which are inductively coupled to the victim are capacitively coupled to the nearest neighbors. Coupling noise on these farther lines are coupled to the far victim by the long range inductive effect. As a result, the overall noise on the victim is also affected by the capacitive coupling noise experienced by the far aggressor and not just inductive coupling. Therefore, simultaneous capacitive and inductive coupling in a multi-line system is not the sum of the noise caused by each aggressor, which significantly increases the complexity of the noise analysis and mitigation process in these structures. To demonstrate the problem, an example three line system is described in Section 3.2.1 and extended to a general N coupled line case in Section 3.2.2. The conditions that allow the noise sources to be summed despite the aforementioned phenomenon are presented in Section 3.2.2.

3.2.1. Example—three coupled lines

To demonstrate this phenomenon, the behavior of three different configurations, as illustrated in Fig. 5, is compared: Three lines with capacitive coupling only, inductive coupling only, and both capacitive and inductive coupling.

Line 1 is the victim and lines 2 and 3 are the aggressors. For simplicity, identical lines with identical coupling are assumed, i.e., $R_1=R_2=R_3$, $C_1=C_2=C_3$, $L_1=L_2=L_3$, $Xcap_1=Xcap_2$ and $M_{12}=M_{23}=M_{13}$. The coupling capacitance and mutual inductance are chosen to maintain the additivity approximation, as described

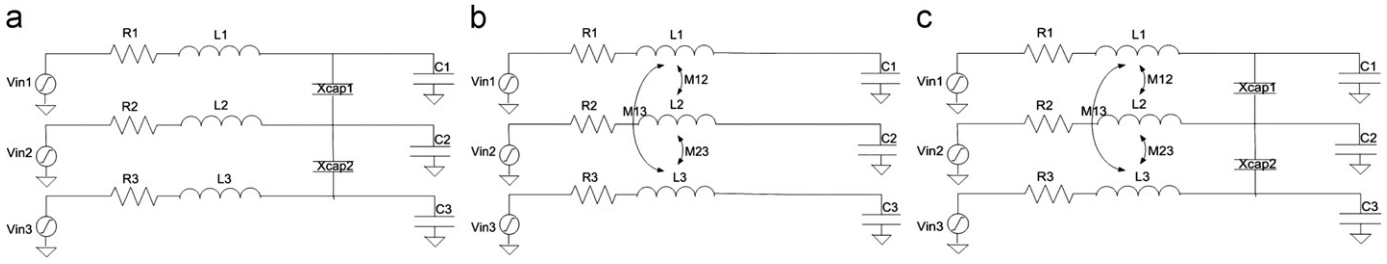

Fig. 5. Three coupled line configuration: (a) capacitive coupling only, (b) inductive coupling only, and (c) both capacitive and inductive coupling.

in Section 2. Consider the noise on the victim (line 1) for three different switching patterns, as listed in Table 1. In pattern ♯ 1, only the nearest neighbor is switching and in patterns ♯ 2 and ♯ 3, both the nearest and the distant neighbors are switching. In pattern ♯ 2, the lines switch in the same direction and in pattern ♯ 3, the lines switch in opposite directions. For the configuration shown in Fig. 5a, the noise on the victim is approximately the same for all three switching patterns since the effect of the distant neighbor is negligible in the case of only capacitive coupling. For the configurations shown in Fig. 5b, according to Section 3.1, the total noise is the sum of the noise caused by each aggressor. Thus, the noise on the victim in pattern ♯ 2 is twice the noise on the victim in pattern ♯ 1. The noise on the victim of pattern ♯ 3 is zero since aggressors ♯ 2 and ♯ 3 cancel.

For the configurations shown in Fig. 5c, based on the additivity properties, the noise on the victim line is equal to the sum of the noise caused by only capacitive coupling, as in the configuration shown in Fig. 5a, and only inductive coupling, as in the configuration shown in Fig. 5b. However, as illustrated in Fig. 6, it is not always the case due to capacitive coupling between distant lines. For pattern ♯ 2 (Fig. 6a), the actual noise, as simulated in SPICE, matches the noise calculated using the additivity properties. For pattern ♯ 3 (Fig. 6b), the noise calculated using the additivity properties is smaller than the actual noise as simulated in SPICE. The reason for the different behavior is that for pattern ♯ 3 there is capacitive coupling between lines 2 and 3, which does not exist in pattern ♯ 2 due to same direction switching. The capacitive coupling noise between lines 2 and 3 is coupled to the victim line through the inductive effect and is added to the total noise.

Several conclusions can be derived from this example that are generalized in the following section. In the case where both capacitive and inductive coupling exists, the total noise cannot always be expressed as the sum of the noise from each aggressor. However, there are cases where this summation is possible; for example, when the capacitive coupling is sufficiently small to be neglected or the lines switch in the same direction.

3.2.2. General case—N coupled lines

Similar to the analysis described in Section 3.1, a lumped RLC model represents a multi-line system in the case of simultaneous capacitive and inductive coupling, as shown in Eq. (3.2.1), where $V_{in,i}$, R_i, C_i, L_i, and M_{ij} are defined in Section 3.1.

$$V'_{in,i} = R_i * I'_i + L_i * I''_i + \sum_{i \neq j} M_{ij} * I_j'' + \frac{1}{C_i} * (I_i + I_{i-1,i} - I_{i,i+1}) \tag{3.2.1}$$

The matrix representation of Eq. (3.2.1) is

$$Vin'_{1XN} = A_{NXN} * Iin_{1XN} + B_{(N-1)XN} * Iij_{1X(N-1)} \tag{3.2.2}$$

where A_{NXN} and $B_{(N-1)XN}$ are described by Eqs. (3.2.3) and (3.2.4)

$$A_{NXN} = \begin{bmatrix} \frac{1}{C_1} + R_1 * \frac{d}{dt} + L_1 * \frac{d^2}{dt^2} & \cdots & M_{1,j} * \frac{d^2}{dt^2} & \cdots & M_{1,N} * \frac{d^2}{dt^2} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ M_{i,1} * \frac{d^2}{dt^2} & \cdots & \frac{1}{C_i} + R_i * \frac{d}{dt} + L_i * \frac{d^2}{dt^2} & \cdots & M_{i,N} * \frac{d^2}{dt^2} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ M_{N,1} * \frac{d^2}{dt^2} & \cdots & M_{N,j} * \frac{d^2}{dt^2} & \cdots & \frac{1}{C_N} + R_N * \frac{d}{dt} + L_N * \frac{d^2}{dt^2} \end{bmatrix} \tag{3.2.3}$$

$$B_{(N-1)XN} = \begin{bmatrix} \frac{1}{C_1} & \cdots & 0 & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & \cdots & \frac{1}{C_i} - \frac{1}{C_i} & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & \cdots & 0 & \cdots & \frac{1}{C_N} \end{bmatrix} \tag{3.2.4}$$

The current per line can be expressed as a function of the input voltages (i.e., switching pattern) by inversing A_{NXN}, as shown in Eq. (3.2.5)

$$I_{1XN} = [A_{NXN}]^{-1} * (Vin'_{1XN} + B_{(N-1)XN} * Iij_{1XN}) \tag{3.2.5}$$

From Eq. (3.2.5), observe that the solution for multiple switching aggressors is not the sum of the solution of each aggressor switching by itself since the current of each line is dependent not only on the input voltage, but also on the currents from the coupling capacitors, as explained in Section 3.2.1. However, by examining Eq. (3.2.5), note that there are cases where the total noise can be expressed as the sum of the noise caused by each aggressor, when $B_{(N-1)XN}$ approaches zero or $|A| \gg |B|$. These conditions translate to either weak capacitive coupling, same direction switching, or strong inductive coupling, according to Eqs. (3.2.3) and (3.2.4). These conditions correspond to the conditions on the additivity of capacitive and inductive coupling, as presented in Section 2

1. $L_i \approx M_{ij}$—strong inductive coupling case,
2. $C_{ij} \ll C_i$—weak capacitive coupling,
3. same direction switching.

To determine the current within the lines, the same method as described in Section 3.1 is applied. First, Eq. (3.2.2) is rewritten in

Table 1
Switching patterns definition for three coupled lines.

	Pattern ♯1	Pattern ♯2	Pattern ♯3
Vin1	'0'	'0'	'0'
Vin2	'↑'	'↑'	'↑'
Vin3	'0'	'↑'	'↓'

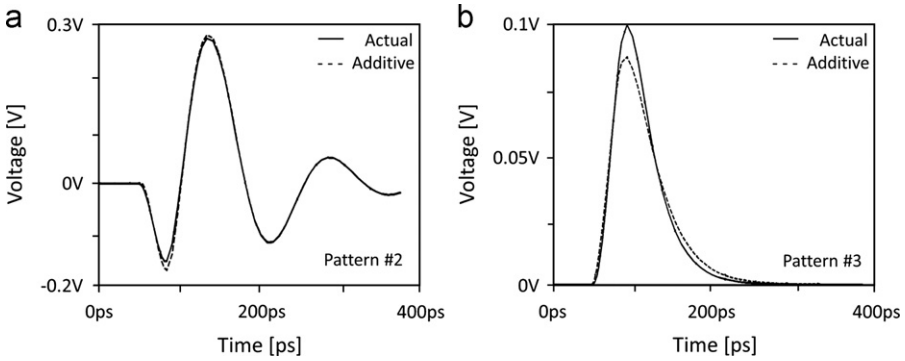

Fig. 6. SPICE vs. additive noise waveform for the configuration shown in Fig. 5c for (a) pattern ♯ 2 and (b) pattern ♯ 3.

the following form:

$$L_{ij} * I'' + R * I' + C^{-1} * I = V \tag{3.2.6}$$

where L_{ij}, R, C, and V are described, respectively, by Eqs. (3.2.7)–(3.2.10)

$$L_{ij} = \begin{bmatrix} M_{1,1}(1+\frac{C_{12}}{C_1}) - M_{2,1}\frac{C_{12}}{C_1} & \cdots & M_{1,j}(1+\frac{C_{12}}{C_1}) - M_{2,j}\frac{C_{12}}{C_1} & \cdots & M_{1,N}(1+\frac{C_{12}}{C_1}) - M_{2,N}\frac{C_{12}}{C_1} \\ \vdots & & \vdots & & \vdots \\ M_{i,1}(1+\frac{C_{i-1,i}+C_{i,i+1}}{C_i}) - M_{i-1,1}\frac{C_{i-1,i}}{C_i} - M_{i+1,1}\frac{C_{i+1,i}}{C_i} & \cdots & M_{i,j}(1+\frac{C_{i-1,i}+C_{i,i+1}}{C_i}) - M_{i-1,j}\frac{C_{i-1,i}}{C_i} - M_{i+1,j}\frac{C_{i+1,i}}{C_i} & \cdots & M_{i,N}(1+\frac{C_{i-1,i}+C_{i,i+1}}{C_i}) - M_{i-1,N}\frac{C_{i-1,i}}{C_i} - M_{i+1,N}\frac{C_{i+1,i}}{C_i} \\ \vdots & & \vdots & & \vdots \\ M_{N,1}(1+\frac{C_{N-1,N}}{C_N}) - M_{N-1,1}\frac{C_{N-1,N}}{C_N} & \cdots & M_{N,j}(1+\frac{C_{N-1,N}}{C_N}) - M_{N-1,j}\frac{C_{N-1,N}}{C_N} & \cdots & M_{N,N}(1+\frac{C_{N-1,N}}{C_N}) - M_{N-1,N}\frac{C_{N-1,N}}{C_N} \end{bmatrix} \tag{3.2.7}$$

$$R = \begin{bmatrix} R_1(1+\frac{C_{12}}{C_1}) & -R_2\frac{C_{12}}{C_1} & \cdots & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & -R_{i-1}\frac{C_{i-1,i}}{C_i} & R_i(1+\frac{C_{i-1,i}+C_{i,i+1}}{C_i}) & -R_{i+1}\frac{C_{i,i+1}}{C_i} & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & \cdots & 0 & -R_{N-1}\frac{C_{N-1,N}}{C_N} & R_N(1+\frac{C_{N-1,N}}{C_N}) \end{bmatrix} \tag{3.2.8}$$

$$C = \begin{bmatrix} \frac{1}{C_1} & \cdots & 0 & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & \cdots & \frac{1}{C_i} & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & \cdots & 0 & \cdots & \frac{1}{C_N} \end{bmatrix} \tag{3.2.9}$$

$$V = \begin{bmatrix} V'_{in,1}(1+\frac{C_{12}}{C_1}) - V'_{in,2}\frac{C_{12}}{C_1} \\ \vdots \\ V'_{in,i}(1+\frac{C_{i-1,i}+C_{i,i+1}}{C_i}) - V'_{in,i-1}\frac{C_{i-1,i}}{C_i} - V'_{in,i+1}\frac{C_{i,i+1}}{C_i} \\ \vdots \\ V'_{in,N}(1+\frac{C_{N-1,N}}{C_N}) - V'_{in,N-1}\frac{C_{N-1,N}}{C_N} \end{bmatrix} \tag{3.2.10}$$

Expression (3.2.6) is a second order differential equation, where the solution is presented in Eq. (3.2.11), y_0 and y_1 are determined by the boundary conditions, and α, ω_0, and ω_d are matrices described, respectively, by Eqs. (3.2.12), (3.2.13), and (3.2.14).

$$I(t) = \begin{Bmatrix} V * C * \left[1 - e^{-\alpha t}\left(\frac{\alpha}{\alpha_d} * \sinh(\alpha_d t) + \cosh(\alpha_d t)\right)\right] t < Tr \\ \frac{e^{-\alpha t}}{\alpha_d}\left[(y_1 + y_0\alpha) * \sinh(\alpha_d t) + y_0\alpha_d \cosh(\alpha_d t)\right] t > Tr \end{Bmatrix} \tag{3.2.11}$$

$$\alpha = 0.5 * R * L_{ij}^{-1} \tag{3.2.12}$$

$$\omega_0{}^2 = L_{ij}^{-1} C^{-1} \tag{3.2.13}$$

$$\alpha_d = \sqrt{\alpha^2 - \omega_0{}^2} \tag{3.2.14}$$

From the form of Eq. (3.2.9) and vector V (see Eq. 3.2.10), note that the noise on each line cannot be expressed as the sum of the noise caused by each aggressor as in the purely inductive case.

Note that matrix α_d can be either real, equal to zero, or complex depending upon the line parameters. When α_d is real, Eq. (3.2.11) maintains the original form and this regime is referred to as overdamped, where the transient response is a decayed current without oscillation, similar to the waveform of pattern ♯ 3 shown in Fig. 6b. The critically damped response ($\alpha_d = 0$) represents the circuit response that decays in the fastest possible time without oscillating. For complex values of α_d, or the underdamped regime, Eq. (3.2.11) includes sinusoidal functions rather than hyperbolic functions and the waveform is in the form of decaying oscillations, similar to the waveform of pattern ♯ 2 shown in Fig. 6a.

4. Modeling multi-aggressor noise

In Section 3, closed-form expressions, (3.2.11)–(3.2.14), for modeling noise in capacitively and inductively coupled multi-line structures are presented. These expressions, however, do not provide physical intuition describing the noise sources (capacitive or inductive, different aggressors). In this section, an alternative model that enables decomposing the noise sources is presented, permitting the noise in coupled multi-line systems to be estimated.

In previous sections, the conditions that express the total noise as a sum of the noise caused by each aggressor and each coupling effect (capacitive and inductive) are presented. In the case of strong inductive coupling ($L_i \approx M_{ij}$), weak capacitive coupling ($C_{ij} \ll C_i$), or same direction switching, it is possible to express the noise of a victim as a sum of the noise caused by each aggressor. The regime that satisfies these conditions is referred to here as the "Linear Regime". If none of these conditions is satisfied, the regime is referred to here as the "Non-Linear Regime", and the additivity approximation cannot be made. In the multi-line scenario, where the primary concern is the long range inductive coupling effect, the linear regime is also the worst case noise scenario.

V_{noise} is the peak total noise of the victim and $V_{noise}(aggressor_i)$ is the peak noise of the victim caused by aggressor i. In the linear regime, the total noise is

$$V_{noise} = \sum_{i=1}^{N} V_{noise}(aggressor_i) \tag{4.1}$$

For adjacent aggressors, the noise is caused by both capacitive coupling ($V_{noise,xcap}$) and inductive coupling ($V_{noise,M}$). For distant aggressors, the noise is caused primarily by inductive coupling. The noise caused by capacitive coupling from non-adjacent aggressors is small and is assumed to be negligible to maintain the simplicity of the model and analysis process. Thus, Eq. (4.1) can be rewritten as

$$V_{noise} = \sum_{i=1}^{N-1} V_{noise,M}(aggressor_i) + \sum_{j=1}^{2} V_{noise,xcap}(aggressor_j) \tag{4.2}$$

To validate this model, the noise, as calculated from Eq. (4.2) using additivity, is compared to the noise as simulated by SPICE for a variety of switching patterns and circuit parameters within an eight line structure. As listed in Table 2, the noise exhibits a maximum error of 9% as compared to SPICE.

By analyzing the range of error of the different experiments listed in Table 2, it can be seen that for stronger inductive coupling as compared to capacitive coupling, the smaller is the error. For any switching pattern and linearity condition, the error decreases with increasing inductive coupling coefficient K (experiments 1 vs. 2 and 4 vs. 5 in Table 2). A decrease in the ratio of coupling capacitance vs. self-capacitance ($Xcap/Cline$) lowers the error (experiments 5 vs. 6, 12 vs. 13, and 25 vs. 26 in Table 2). The resistance satisfies the first linearity condition (low loss approximation)—the larger the resistance, the smaller the error due to suppression of ringing (experiment 14 vs. 15 in

Table 2
Model verification for the linear regime.

Linearity condition	Exp.#	Circuit parameters					Noise peak for line # 1		
		Switching pattern	R_{line} [Ω]	C_{line} [pF]	X_{cap} [pF]	K	Exact (Spice) [V]	Using additivity [V]	Error [%]
Strong inductive coupling	**1**	**0**0R0R0RR	60	0.1	0.15	0.9	0.324	0.325	−0.04
	2	**0**0R0R0RR	60	0.1	0.15	0.5	0.277	0.282	1.70
	3	**0**0R0R0RR	120	0.2	0.15	0.5	0.120	0.121	−1.25
	4	**1**00FRF0R	60	0.1	0.15	0.5	1.019	1.002	1.74
	5	**1**00FRF0R	60	0.1	0.15	0.9	1.007	1.001	0.61
	6	**1**00FRF0R	60	0.2	0.15	0.9	1.003	1.000	0.31
	7	**1**10FR000	60	0.1	0.15	0.5	1.017	1.006	1.10
	8	**1**10FR000	120	0.2	0.15	0.5	1.004	1.003	0.01
	9	**R**RFFR000	60	0.1	0.15	0.9	1.106	1.109	−0.20
	10	**R**RFFR000	60	0.1	0.15	0.5	1.154	1.177	−1.92
Weak capacitive coupling	**11**	**0**0R0R0RR	60	0.1	0	0.3	0.281	0.281	0.05
	12	**0**0R0R0RR	60	0.1	0.15	0.3	0.225	0.236	−4.72
	13	**0**0R0R0RR	60	0.2	0.15	0.3	0.196	0.197	−0.56
	14	**1**00FRF0R	60	0.2	0.05	0.3	1.002	1.000	0.22
	15	**1**00FRF0R	120	0.2	0.05	0.3	1.001	1.001	0.01
	16	**1**10FR000	60	0.1	0	0.5	1.000	1.000	0.00
	17	**1**10FR000	60	0.2	0.05	0.3	1.002	1.000	0.21
	18	**R**RFFR000	60	0.1	0	0.3	1.155	1.155	−0.02
	19	**R**RFFR000	120	0.2	0.05	0.3	1.026	1.050	−2.41
Same direction switching	**20**	**R**RRRRRRR	60	0.1	0.15	0.9	1.668	1.673	−0.26
	21	**R**RRRRRRR	60	0.1	0.15	0.5	1.586	1.657	−4.44
	22	**R**RRRRRRR	120	0.2	0.15	0.5	1.243	1.292	−3.96
	23	**F**FFFFFFF	60	0.1	0.15	0.9	−0.668	−0.673	−0.65
	24	**F**FFFFFFF	60	0.2	0.15	0.9	−0.591	−0.594	−0.37
	25	**R**RRRRRRR	60	0.1	0.15	0.3	1.511	1.636	−8.26
	26	**R**RRRRRRR	60	0.2	0.15	0.3	1.431	1.502	−5.01

Pattern: R—switching '0'→'1'; F—switching'1'→'0'; 0/1—constant '0' or '1'.
R_{line}, C_{line}, X_{cap}—Line resistance, line capacitance, and coupling capacitance.
K—Inductive coupling coefficient L_i/L_{ij}.

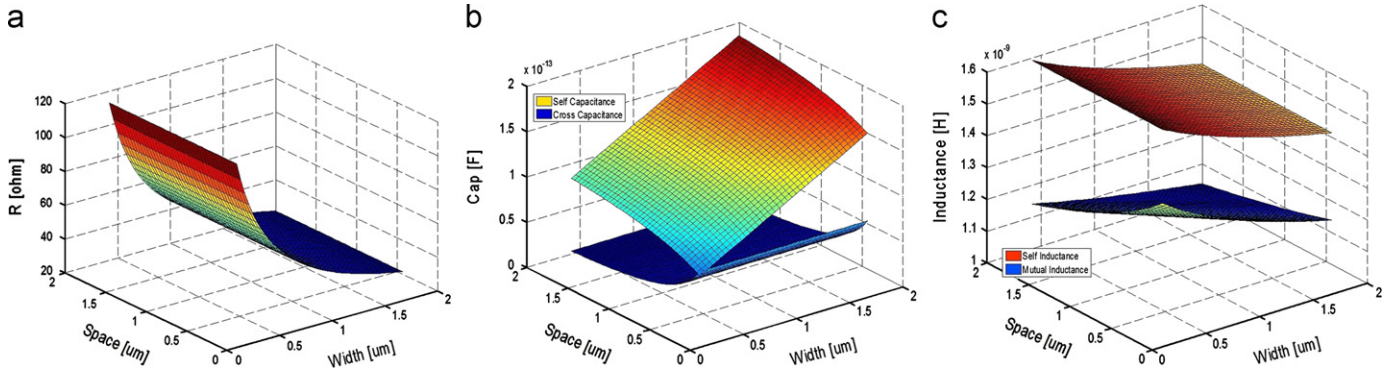

Fig. 7. Line parameters as a function of line width and spacing: (a) resistance as a function of line width and spacing, (b) self-capacitance and cross-capacitance as a function of line width and spacing, and (c) self-inductance and mutual inductance as a function of line width and spacing.

Table 2). These observations are in agreement with the definition of the linearity conditions.

5. Application to noise mitigation through layout optimization

The model presented in Section 4 can be used to evaluate the criticality of each noise source (capacitive vs. inductive, noise caused by different aggressors), permitting the most effective noise mitigation method to be applied. In this section, analysis of the dependence of the noise on the physical layout parameters is presented, followed by a formulation of layout based mitigation guidelines. The noise mitigation guidelines are demonstrated on a case study using the model described in Section 4.

5.1. Dependence of coupling noise on layout parameters

The topology of global and semi-global interconnects is generally determined by floorplan constraints. Consequently, the primary noise mitigation techniques, in addition to shield lines, modify layout properties such as the line width and spacing between adjacent lines. Capacitive and inductive coupling noise typically exhibits different and sometimes contradictory layout dependencies [13,14], which directly affect the noise mitigation techniques for capacitive coupling, inductive coupling, and simultaneous capacitive and inductive coupling. To better understand the dependence of each coupling effect on the layout parameters, the line parameters as a function of line width and spacing are examined, as illustrated in Fig. 7, based on closed-form expressions for the line resistance, capacitance, and inductance [11,12].

The criticality of the capacitive coupling is determined by the ratio of the coupling and self-capacitance, where an increase in the ratio results in increased capacitive coupling noise [15]. The maximum ratio occurs for narrow and close lines (see Fig. 7b). For inductive coupling, the noise peak is determined by the ratio of the mutual and self-inductance. Since the sensitivity of the mutual inductance to the line width and spacing is low, this ratio remains approximately constant over a wide range of layout configurations (see Fig. 7c). However, the line resistance, which exhibits high sensitivity to the line width (see Fig. 7a), has a substantial effect on the noise caused by coupling effects, where an increase in the resistance results in a lower peak noise.

To analyze the dependence of the coupling noise on layout parameters, the analytic solution (without the additivity approximation), as described in Eq. (3.2.11), is combined with the closed-form expressions of the line resistance, capacitance, and inductance [12] for a two line coupled system. Inductive and capacitive coupling noise as a function of line width and spacing is illustrated in Fig. 8. Note that the capacitive coupling noise is affected by both the line width and spacing due to the effect of the line width on the self-capacitance, while inductive coupling noise is primarily dependent on the line width due to the strong dependence on the line resistance.

To reduce capacitive coupling noise, increasing either or both the space or the line width is effective [16,17]. Spacing the lines results in lower coupling capacitance and widening the lines increases the self-capacitance which decreases the noise. Both techniques are similarly effective, as shown in Fig. 8a, however note that both spacing and widening are effective only over a limited range. For lines wider than twice the minimum width and farther than twice the minimum space, neither technique reduces the noise. To mitigate inductive coupling, narrow lines are more effective. This result is expected since increasing the space between the lines decreases the coupling capacitance and has little effect on the mutual inductance; thus, this method is only effective for mitigating capacitive coupling noise. Widening the lines, however, reduces the line resistance, increases the self-capacitance of the line, and has a small effect on the inductance. As a result, there is a contradictory effect on the capacitive and inductive coupling noise. Inductive coupling noise will increase due to a decrease in the line resistance, while capacitive coupling noise will decrease due to an increase in the line self-capacitance. The implication is that in the presence of simultaneous inductive and capacitive coupling, the appropriate noise mitigation method should be chosen based on the criticality of the coupling effect as well as timing and power constraints. If capacitive coupling is more critical, increasing the space between the lines should be considered. Widening the lines should be considered only if the inductive coupling is negligible, since while the capacitive coupling noise will decrease, the inductive coupling noise will increase. However, if inductive coupling is dominant, increasing the space between the lines will have a negligible effect on the noise and the lines should be made more narrow [14]. Dominant capacitive coupling is expected between narrow and close lines since the small distance between the lines increases the coupling capacitance, and a narrow width results in high resistivity which decreases the inductive effects. Due to the strong dependence of the line resistance and inductive effects on the width, for wide, low resistance lines, inductive coupling is expected to dominate.

5.2. Case study

To demonstrate the model described in Section 4 for noise analysis and mitigation, a bus composed of eight parallel lines in a 32 nm CMOS process [11] is examined. The layout parameters are chosen to coincide with the linear regime, thus the model proposed in the previous section can be applied. The noise on line 3 of an eight bit wide bus caused by each aggressor as well as the interconnect impedances are listed in Table 3, where line 3 is a quiet victim and four different switching neighbors (lines 2, 4, 6, and 8) are aggressors. Based on Eq. (4.2), the peak noise of the victim line is

$$V_{noise}(line\#3) = \sum_{i=2,4,6,8} V_{noise,M}(aggressor_i) + \sum_{j=2,4} V_{noise,xcap}(aggressor_j) \tag{5.1}$$

Note the contribution of each aggressor to the total noise is almost identical. Inductive effects are therefore more dominant than capacitive coupling and nearest neighbors are not more dangerous than a distant aggressor. In addition, long range inductive coupling cannot be neglected for any bit within a bus. The most effective noise mitigation technique is to not increase the space between the lines, but rather the lines should be made more narrow to increase the line resistance and, as a result, decrease the peak noise.

Table 3
Noise breakdown for a typical 8 bit bus.

Aggressor	Noise
2	0.092 V
4	0.098 V
6	0.104 V
8	0.104 V
All (using additivity)	0.398 V
All (exact-SPICE)	0.372 V

Switching pattern: 0R0R0R0R, R—switching '0'→'1'; 0—constant '0'.
Line parameters: length=1000 μm, width=0.79 μm, space=0.394 μm.
Extracted circuit parameters: resistance 57.26 Ω, line capacitance 76.2 fF, coupling capacitance 55.6 fF, and inductive coupling coefficient K between 0.6 and 0.85.

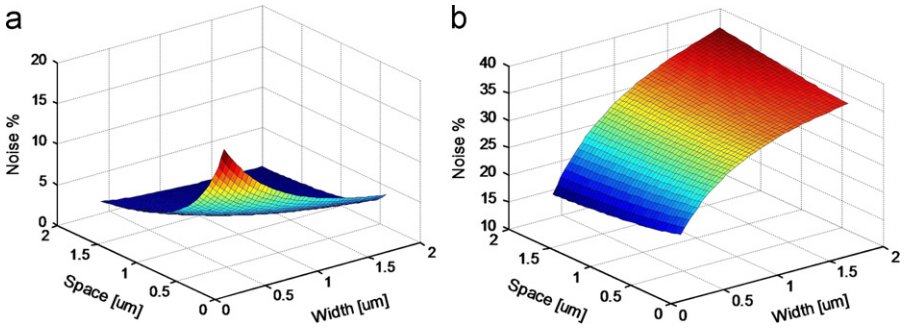

Fig. 8. Coupling noise as a function of line width and spacing: (a) peak noise due to capacitive coupling, and (b) peak noise due to inductive coupling.

6. Conclusions

A method based on modeling the additive properties of capacitive and inductive coupling noise is proposed for analyzing multiple lines systems in the presence of simultaneous inductive and capacitive coupling. The method can be used to estimate the criticality of each noise source. It is shown that capacitive and inductive coupling noise is not always additive and that although each of the coupling effects can be modeled as the sum of the noise caused by each aggressor, when both effects exist this approach is not always accurate. The conditions that allow expressing the total noise as the sum of the noise caused by each aggressor and noise source are based on an analysis of a multiple line system. These conditions coincide with the critical noise scenarios of a multi-line structure in the presence of simultaneous inductive and capacitive coupling. The analytic method is compared to SPICE and a maximum error of 9% is demonstrated for a variety of switching patterns and circuit parameters. Layout guidelines are provided for reducing noise in coupled RLC interconnects and, together with the proposed models, noise reduction in multi-line structures is demonstrated.

References

[1] T. Kim, Y. Eo, Analytic CAD models for the signal transients and crosstalk noise of inductance-effect-prominent multicoupled RLC interconnect lines, IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. 27 (7) (2008) 1214–1227.
[2] G. Chen, E.G. Friedman, An RLC interconnect model based on Fourier analysis, IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. 24 (2) (2005) 170–183.
[3] S. Tuuna, J. Isoaho, H. Tenhunen, Analytical model for crosstalk and intersymbol interference in point-to-point buses, IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. 25 (7) (2006) 1400–1411.
[4] A. Naeemi, J.A. Davis, J.D. Meindl, Compact physical models for multilevel interconnect crosstalk in gigascale integration (GSI), IEEE Trans. Electron Dev. 51 (11) (2004) 1902–1912.
[5] S.H. Choi, B.C. Paul, K. Roy, Dynamic noise analysis with capacitive and inductive coupling, in: Proceedings of the IEEE Asia and South Pacific Design Automation Conference, January 2002, pp. 65–70.
[6] Y. Eo, J. Shim, W.R. Eisenstadt, A traveling-wave-based waveform approximation technique for the timing verification of single transmission lines, IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. 21 (6) (2002) 723–730.
[7] S. Shin, Y. Eo, W.R. Eisenstadt, Analytic models and algorithms for the efficient signal integrity verification of inductance-effect-prominent multicoupled VLSI circuit interconnects, IEEE Trans. Very Large Scale Integration (VLSI) Syst. 12 (4) (2004) 395–407.
[8] Y. Cao, X. Yang, X. Huang, D. Sylvester, Switch-factor-based loop RLC modeling for efficient timing analysis, IEEE Trans. Very Large Scale Integration (VLSI) Syst. 13 (9) (2005) 1072–1078.
[9] J. Chen, L. He, Worst-case crosstalk noise for nonswitching victims in high-speed buses, IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. 24 (8) (2005) 1275–1283.
[10] J.E. Lorival, D. Deschacht, Y. Quere, T. Le Gouguec, F. Huret, Additivity of capacitive and inductive coupling in submicronic interconnects, Proc. IEEE Des. Test Integr. Syst. Nanoscale Technol. (2006) 300–304.
[11] International Technology Roadmap for Semiconductors, 2010, 〈http://www.itrs.net〉.
[12] Predictive Technology Model, 〈http://ptm.asu.edu/〉.
[13] K. Agarwal, D. Sylvester, D. Blaauw, Modeling and analysis of crosstalk noise in coupled RLC interconnects, IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. 25 (5) (2006) 892–901.
[14] Y. Massoud, S. Majors, J. Kawa, T. Bustami, D. MacMillen, J. White, Managing on-chip inductive effects, IEEE Trans. Very Large Scale Integration (VLSI) Syst. 10 (6) (2002) 789–798.
[15] K.T. Tang, E.G. Friedman, Delay and noise estimation of CMOS logic gates driving coupled resistive–capacitive interconnections, Integration, VLSI J. 29 (2) (2000) 131–165.
[16] T. Xue, E.S. Kuh, Y. Qingjian, A sensitivity-based wiresizing approach to interconnect optimization of lossy transmission line topologies, in: Proceedings of the IEEE Multi-Chip Module Conference, February 1996, pp. 117–122.
[17] K. Chaudhary, A. Onozawa, E.S. Kuh, A spacing algorithm for performance enhancement and cross-talk reduction, in: Proceedings of the IEEE International Conference on Computer-Aided Design, November 1993, pp. 697–702.
[18] R.E. Collin, Foundations for Microwave Engineering, Wiley-IEEE Press, 2001. (Chapter 4, pp. 220–302).