Microelectronics Journal 45 (2014) 133–143

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

2T–1R STT-MRAM memory cells for enhanced on/off current ratio ☆

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ARTICLE INFO

Article history:
Received 19 September 2013
Received in revised form
21 November 2013
Accepted 26 November 2013
Available online 31 December 2013

Keywords:
MRAM
VLSI
Resistive memories

ABSTRACT

Novel spin torque transfer magnetic tunnel junction (STT-MTJ) based memory cell topologies are introduced to improve both the sense margin and the current ratio observed by the sense circuitry. These circuits utilize an additional transistor per cell in either a diode connected or gate connected manner and maintain leakage current immunity within the data array. An order of magnitude increase in the current ratio over a traditional 1T–1R structure is observed. This improvement comes at a cost of 61% and 117% increase in area, respectively, for the diode and gate connected cells.

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1. Introduction

Spin torque transfer magnetoresistive RAM (STT-MRAM) has emerged as a competitive CMOS compatible technology, capable of replacing traditional on-chip CMOS memory. With the features of non-volatility, no static power consumption, and nearly unlimited write endurance, STT-MRAM has unique advantages over traditional memory circuits. The Achilles heel of STT-MRAM, however, is the small on/off resistance ratio. This limitation requires sophisticated read circuitry which leads to greater sensitivity to noise.

To address these limitations, two memory cells are proposed that significantly improve the output read ratio. These memory cell variants utilize additional CMOS transistors within the cell to enhance the observed on/off resistance ratio of the MTJ device leading to a shorter read delay. Additional transistors are added in either a gate connected or diode connected manner to the adjacent metal lines that interface with the sense circuitry. Each cell exhibits an order of magnitude increase in the current ratio as compared to a traditional 1T–1R structure while requiring more area and delivering comparable energy efficiency under high bias. This improvement in current ratio yields a 29% and 81% reduction in memory sensing delay as compared, respectively, to the standard 1T–1R STT-MRAM memory cell and a 8T-SRAM.

Background on STT-MTJ devices is presented in Section 2. Prior art in STT-MRAM memory is presented in Section 3. Each cell type is introduced in Section 4. Methods for modeling STT-MRAM arrays along with an evaluation of the sense margin and sense ratio for each cell are presented in Section 5. Some conclusions are offered in Section 6.

2. Background

Spin torque transfer magnetic tunnel junctions (STT-MTJs), the storage elements in STT-MRAM, are two terminal devices that operate on the principle of spin-dependent conduction through magnetic domains [1–4]. The device is structured as a stack of thin films where a thin oxide layer separates two, typically CoFeB, ferromagnetic layers [5]. Of these ferromagnetic layers, one has a fixed spin polarity (the *fixed* layer) that passes electrons of the same spin direction and reflects electrons with the opposite spin; the other layer (the *free* layer) has a bistable magnetic polarity that is affected by the spin of the incoming electrons. By controlling the direction of the current through the device, either the passing electrons or the reflected electrons influence the free layer. Applying large bias currents to the STT-MTJ (approximately 35–300 μA) switches the polarity of the device [1,6,7].

STT-MTJs are structured to ensure that the polarity of the free layer is always either parallel or anti-parallel to the polarity of the fixed layer. The tunneling current through the MTJ, *i.e.*, the resistance of the device, is lower in the parallel state (R_{on}) and higher in the anti-parallel state (R_{off}). In the parallel state, the electrons passing through the fixed layer have the same spin as the free layer, which decreases the device resistance. Alternatively, anti-parallel alignment causes the current from the polarizer to be reflected off the free layer. This reflection is manifested as an increase in resistance. The key figure of merit of an STT-MTJ characterizing the change in resistance is the tunneling magneto-resistance ratio (*TMR*):

$$TMR_0 = \frac{R_{off} - R_{on}}{R_{on}}, \tag{1}$$

where R_{on} and R_{off} describe the minimum and maximum resistance of an MTJ, respectively. An STT-MTJ typically exhibits a peak *TMR* ratio between 80% and 150%, corresponding to roughly a 100% (or

☆This research is supported in part by Grants from Qualcomm, Cisco Systems, and Samsung.

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http://dx.doi.org/10.1016/j.mejo.2013.11.015

$2\times$) change in resistance. The peak *TMR* is determined with a near zero voltage bias across the MTJ, which decreases with increasing voltage across the device [8]. The primary goal of the proposed memory cell variants is to increase the current ratio (I_{on}/I_{off}), where I_{on} and I_{off} correspond to the current observed by the sense circuitry when the MTJ is, respectively, in the on or off state. This objective is achieved by adding an additional transistor to the memory cell.

An STT-MTJ, however, cannot be treated as an ideal resistor. These devices maintain a voltage dependent resistance that significantly lowers R_{off} with increasing bias. This effect is modeled by the effective *TMR*:

$$TMR(V_{MTJ}) = \frac{TMR_0}{1+\frac{V_{MTJ}^2}{V_h^2}}, \quad (2)$$

where V_{MTJ} is the voltage across the device, and V_h is the voltage bias on the MTJ where the *TMR* is reduced by 50% [9]. The bias degradation in the *TMR* is primarily observed when the device is in the anti-parallel state (R_{off}); therefore, R_{on} is assumed to be constant [10]. This basic model captures the DC operation of the MTJ and is valid in all cases where V_{MTJ} is less than the minimum write voltage of a device. Due to this bias dependence, the sense margin is degraded as compared to the ideal case. Notably, the transient characteristics of an MTJ have little effect on the observed sense margin. The switching process of the MTJ is a discrete event where the resistance settles to either R_{on} or R_{off}. As such, the MTJ remains in either the on or off state during reads, and the switching operation of the device can be ignored.

2.1. Comparison with CMOS memory technology

Unlike CMOS SRAM and DRAM, STT-MRAM is a passive non-volatile storage technology with no leakage current within the data array. A reduction in the threshold voltage of the access transistor therefore exhibits two beneficial effects. First, a smaller transistor may be used to supply sufficient write current to the device. For the same sized transistor, a larger current can be supplied in excess of the minimum switching current to further reduce the write energy and latency. Second, the resistance of the access transistor is reduced, further improving both the voltage and current sense margins. Additional benefits of the proposed cell topologies are discussed in Section 4.

3. Prior art

Research in STT-MRAM and other resistive memory devices has typically focused on three distinct fields—device modeling of the individual MRAM elements, innovation in sensing circuitry, and technological improvements. The two thrusts of MTJ technological innovation have focused on increasing the device TMR and reducing the write current while maintaining thermal stability, the criterion determining the non-volatility of the device. Perpendicular magnetic anisotropy, a key innovation, was first experimentally observed in [11] and demonstrated in several subsequent prototypes [2,12]. This device structure enables a significant reduction in write current while maintaining the target of 10 year non-volatility. Significant research has since been devoted to improving these technological characteristics through additional material systems and by refining existing fabrication processes [2,13–15].

From a circuit design perspective, several groups have demonstrated compact models that accurately fit device operation [16,9]. Each of these models incorporates the spin dependent conduction process and dynamic spin torque mechanism required for switching. Building on these efforts, recent models have incorporated statistical aspects to the switching process [17]. These refinements, while more accurate, have introduced additional complexity when analyzing STT-MRAM circuits.

Novel sense circuits have been developed to enhance the signal integrity of STT-MRAM caches. These schemes utilize traditional SRAM sense amplifiers with redundant dummy MTJs or resistors to generate a reference signal for sensing [18]. In [19], the authors presented a self-referenced sensing scheme to determine a cell state tolerant to variations in the device resistance. In these schemes, additional circuitry, placed at the periphery of the array, ensures that the available sense margin is sufficient for operation.

The primary contribution of this work addresses the issue of low device TMR to enhance sensing. This objective is achieved by two memory cell topologies that use an additional CMOS transistor per cell.

4. STT-MTJ memory cells

Three basic cell types are described for use in STT-MTJ memories. The standard 1T–1R memory cell is described in Section 4.1, followed by the proposed 2T–1R cell variants in Section 4.2, and a discussion of the effects of technology on the memory array write current in Section 4.3.

4.1. 1T–1R cell

The 1T–1R cell, the basic building block of resistive memory arrays (see Fig. 1(a)), must satisfy several design constraints to operate correctly. At full bias, the internal cell transistor and access circuitry must supply sufficiently high current to ensure that the MTJ switches (I_c); however, currents in excess of this amount are typically required for high speed switching. For reads, a cell current must remain sufficiently below the critical current to mitigate the potential for erroneous writes to the device. Moreover, each transistor isolates a selected memory cell from any peripheral cells to maintain the required sense margin. For this purpose, the read operation biases the access transistor within the linear region; a reverse bias would needlessly reduce the sense margin.

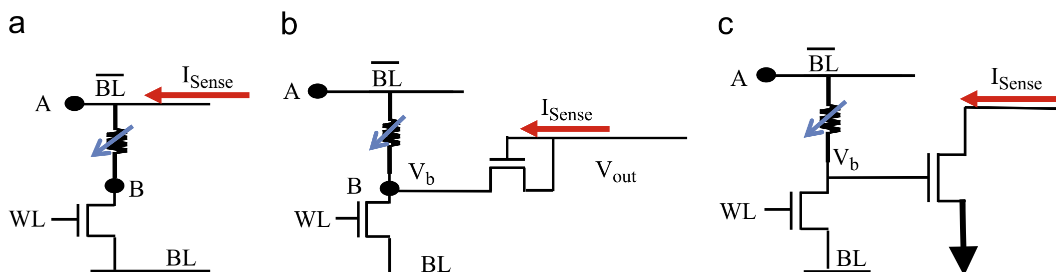

Fig. 1. Circuit diagram of STT-MTJ memory cells: (a) standard 1T–1MTJ, (b) 2T–1MTJ diode cell, and (c) 2T–1MTJ gate cell.

A 1T–1R cell is the simplest memory cell topology for typical STT-MRAM technologies. The sense margin of the device is observed as a voltage or current proportional to the TMR of the device.

4.2. 2T–1R cells

Alternate memory cell topologies utilizing an additional transistor can produce voltage and current amplification without sacrificing immunity to leakage current within the MRAM array.

Diode connected transistor read port: A diode connected transistor incorporated into a memory cell, as shown in Fig. 1(b), amplifies the voltage of the internal node of the memory cell (node B) to produce a current and voltage signal at the transistor output. The maximum amplification occurs when node B is biased to ensure that the R_{on} and R_{off} states produce a voltage, respectively, above and below the threshold of the transistor.

Gate connected transistor read port: A gate connected memory cell, as shown in Fig. 1(c), achieves the same amplification as the diode connected transistor and operates at a similar maximum voltage. This topology, however, differs in several key aspects. First, the gate connected transistor is electrically isolated from node B, facilitating the addition of multiple gate connected read ports. Second, the source of the transistor is connected to ground, eliminating any source body voltage bias, improving the conductance of the transistor. Third, the output current margin is a function of transistor width which can be increased to improve the sense margin.

4.3. Effect of technology on write current

Given that the writes in both the standard 1T–1R cell and the 2T–1R memory cells occur in the same manner, a reduction in the threshold voltage can increase the available write current for a given CMOS technology. The source current as a function of transistor device width and threshold voltage is shown in Fig. 3. As expected, the write current increases with decreasing threshold voltage. In the reverse write current case, the cell transistor exhibits a threshold drop due to the inability of an NMOS transistor to pass a full voltage swing. Threshold voltage reduction shortens the minimum width of the NMOS transistor needed to provide sufficient current to write to the MTJ. This voltage drop is the primary limitation to sourcing a sufficiently high write current in standard CMOS technologies. As shown in Fig. 3, a 60% reduction in the threshold current allows a minimum sized device to supply the required 35 μA. Under forward bias, the maximum current is only limited by the total resistance of the write lines and memory cell. A reduction in the threshold voltage has a smaller effect on the on-resistance of the cell transistor within the linear region as compared to the saturation region. A reduced threshold voltage under forward bias therefore exhibits a smaller increase in the transistor write current than in the reverse bias case. The current saturates to approximately twice I_c despite an increased transistor size and reduced threshold voltage. This result shows that as the threshold voltage is reduced, the array size and not the cell transistor becomes the primary constraint to supplying sufficient write current to the device.

Table 1
MTJ parameters.

R_{ON}	5 kΩ
R_{OFF}	12.5 kΩ
TMR	150%
I_c	35 μA

5. Memory array model of STT-MRAM

The following section evaluates each of the cell types with respect to current margin and current ratio. The simulation setup is described in Section 5.1. The circuit models used to evaluate the current margin and current ratio for each of the memory cells are discussed in Section 5.2.

5.1. Simulation setup

Each memory cell type is evaluated for size and bias conditions to enhance the sense margin. The evaluation is based on the device parameters listed in Table 1 [4]. The MTJ is modeled by (A.3), where the MTJ half bias voltage (V_h) is inferred from the Slonczewski expression for TMR [20]. This expression describes the 50% bias point at the switching current of an MTJ. SPICE simulations of the MOS transistors are based on the predictive technology model (PTM) at the 22 nm node [21]. The initial circuit characteristics are determined from the procedure described in Appendix A.

The layout of each of the three STT-MRAM cells is depicted in Fig. 2, and is based on the FreePDK45 design kit [22]. The cell density for the 1T–1R, 2T–1R diode connected, and 2T–1R gate connected is, respectively, 46.6F^2, 75.6F^2, and 101.5F^2. Note that the size of the memory cells is much larger than a state-of-the-art STT-MRAM, which typically exhibits a 6F^2 cell area. These smaller area circuits, however, are typically created in a standalone memory process flow where layout regularity and technological focus facilitate the use of more aggressive design rules.

For the physical layout shown in Fig. 2, the width of each transistor is 2.2*F*. Any transistor width smaller than this dimension does not decrease the area of either 2T–1R memory cell. This limit is due to minimum sizing rules for contact and transistor spacing; in a practical setting for memories, rules could be tighter to improve density. Design rules specific to memories, however, were

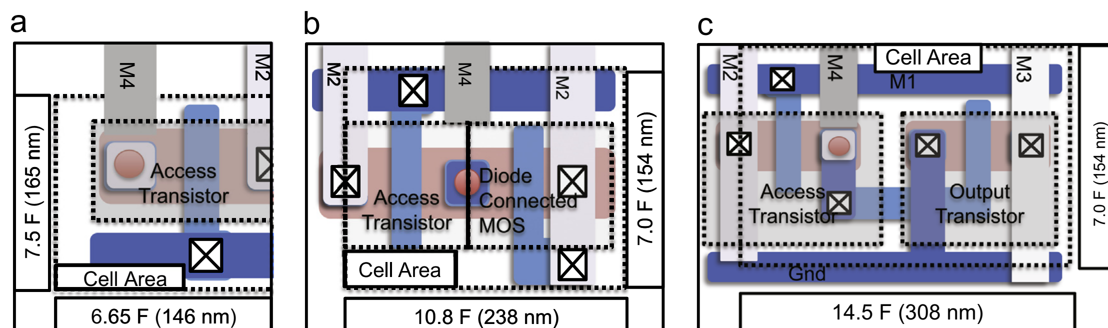

Fig. 2. Physical layout of STT-MTJ memory cells: (a) standard 1T–1MTJ, (b) 2T–1MTJ diode cell, and (c) 2T–1MTJ gate cell. The physical layout is based on the FreePDK45 where *F* represents the feature size of the technology [22].

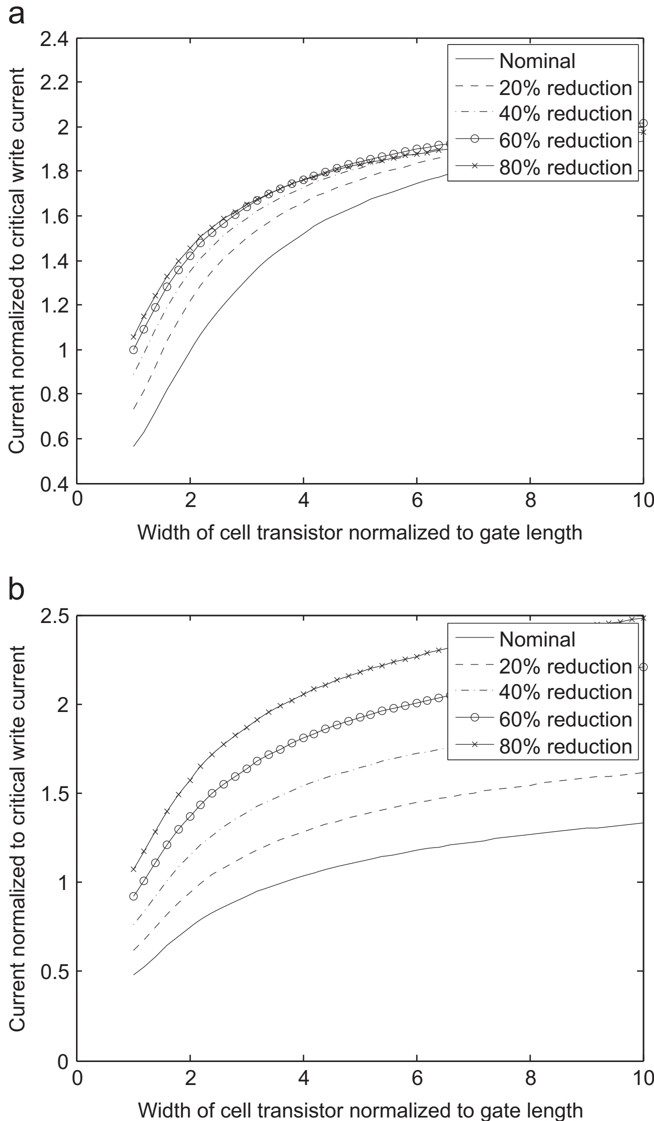

Fig. 3. Write current for 1T–1R cell versus gate length of access transistor and threshold reduction in the CMOS transistor. (a) Forward write current, and (b) reverse write current.

not available so design rules tailored for logic circuits are used for these layouts.

5.2. Modeling approach

An STT-MRAM array can be modeled as a voltage divider. The subsequent discussion describes this model and the response of the sense margin and current ratio to the array voltage bias, array size, threshold voltage, and device width of the NMOS transistors within the data array. The current margin is the difference between the off current and the on current for an MTJ cell under bias. The current ratio is the on current divided by the off current for a cell under bias.

5.2.1. 1T–1R data array

The circuit model is shown in Fig. 4(a), where R_{tp} is the resistance of the PMOS transistor, R_{tc} is the resistance of the NMOS cell access transistor, R_{bl} is the resistance of the bitline, R_{tn} is the column access transistor, and R_{mtj} is the resistance of the STT-MTJ. The sense node A is the observable voltage on the network.

The voltage bias (V_{Bias}) applied to the data array directly controls the magnitude of the signal detected by the sense circuitry. In the case of the 1T–1R memory cell, however, there is a diminishing return with a larger bias as the current ratio drops off.

This degradation, shown in Fig. 5, depicts a contour map of the current margin and current ratio for varying NMOS transistor sizes within the array and voltage biases. The standard 1T–1R cell exhibits a peak current ratio of approximately two for a 0.1 V bias. This ratio is 0.6 less than the expected 2.5 predicted by an ideal MTJ device due to the nonlinear voltage drop across the access transistors and the reduction in device TMR with larger voltage bias. Additionally, the voltage dependence of the TMR ensures that increasing the voltage bias of the array further reduces the current ratio. At full V_{DD}, the peak current ratio drops to approximately 1.4.

These peak current ratios occur with large access transistor sizes. For smaller NMOS transistor sizes, more practical in high density memories, a reduced current ratio as compared to the peak ratio is noted. At low bias (0.1–0.4 V), the current margin remains relatively constant for increasing NMOS device size. This behavior indicates that low voltage, large transistors are preferable to increase the bias voltage when improving the sense margin of a 1T–1R array.

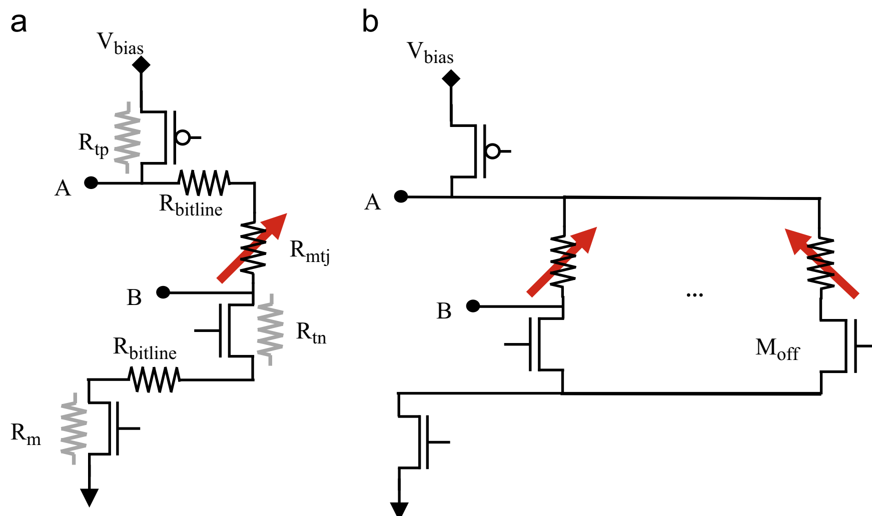

Fig. 4. Circuit diagram of STT-MRAM array. (a) Memory cell sensing model and (b) data array model.

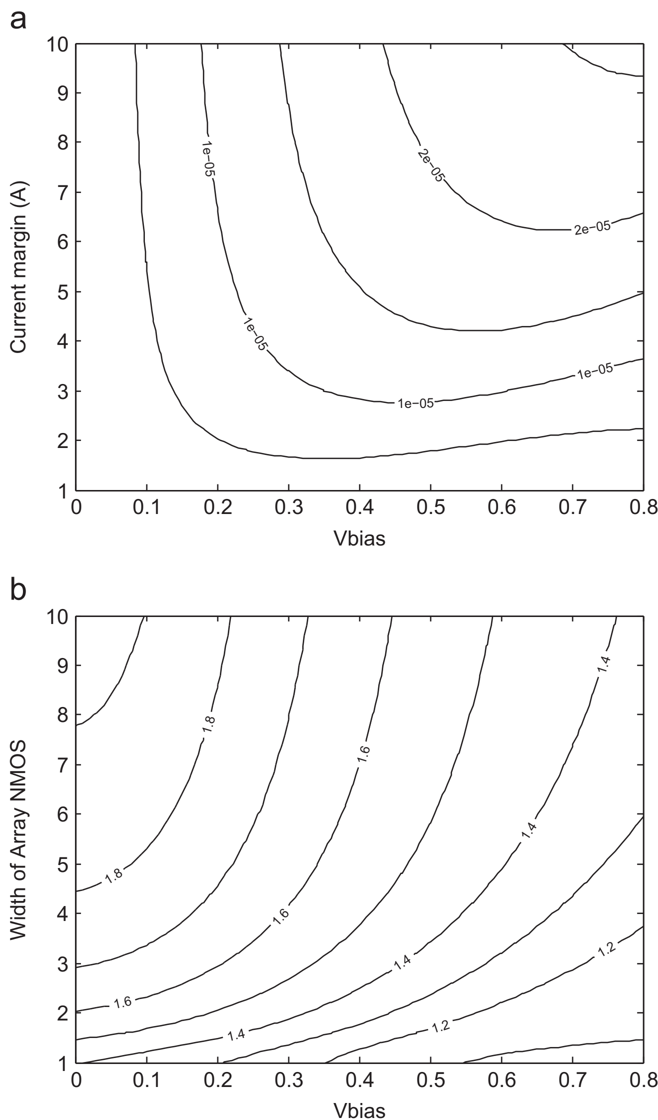

Fig. 5. Design space of 1T–1R memory cell at nominal threshold, (a) current margin and (b) current ratio.

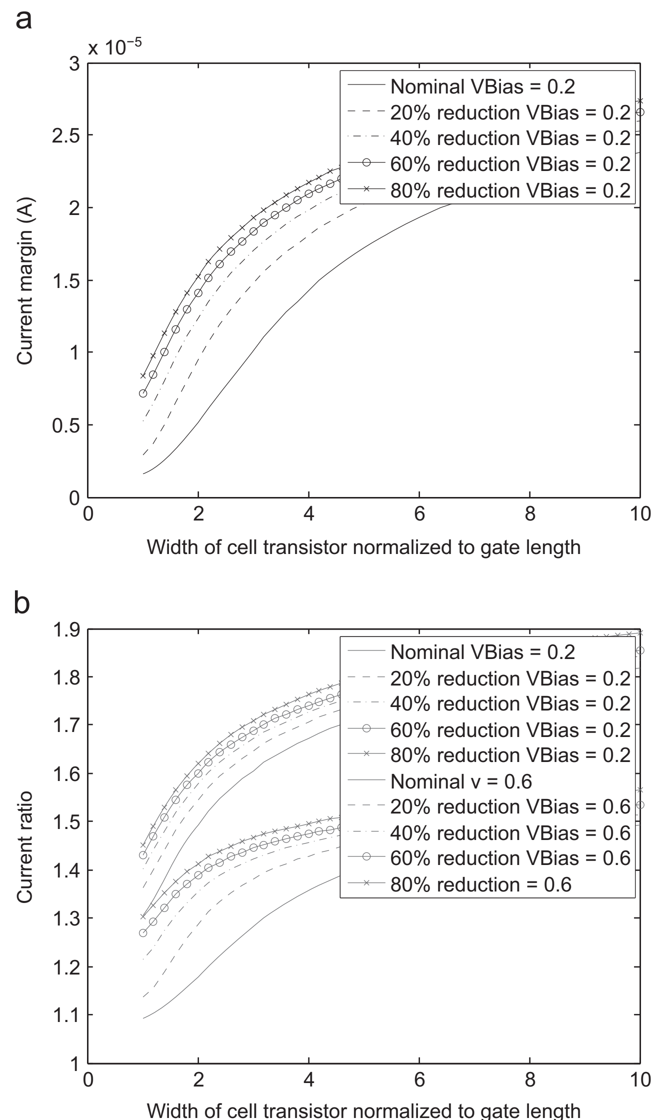

Fig. 6. Effect of reduced threshold voltage of 1T–1R memory cell for increasing size of data array transistors. (a) Current margin and (b) current ratio.

The effect of a reduced array threshold voltage for a 1T–1R cell is shown in Fig. 6 for a high voltage bias (0.6 V) and low voltage bias (0.2 V) array. Note that the reduction in threshold voltage has a limited effect on the current margin at low bias voltages. The sense margin is approximately invariant with the threshold voltage of the transistors in the data array. In contrast, the current ratio increases by approximately 0.2 over a nominal threshold voltage due to an 80% reduction in threshold voltage. A reduction in the transistor threshold voltage in low voltage, small transistor 1T–1R memory cells is therefore desirable.

A reduction in the threshold voltage, however, also degrades the isolation of the data array. The decreased current margin and switching ratio for increasing array size are shown in Fig. 7. At increasing array size, the current margin and current ratio decrease as the threshold voltage is reduced. This effect occurs despite that reduced threshold voltages will improve the current ratio and current margin for a single 1T–1R cell due to the smaller threshold voltages affecting the transistor off-current more than the on-current. The reduced transistor off current results in additional active leakage through the unselected cells, causing both the current ratio and current margin to degrade as a function of array size. As the array size approaches 1024 rows, the current ratio drops to unity, indicating that the change in resistance of the MTJ is negligible.

5.2.2. 2T–1R diode connected memory cell

Unlike the 1T–1R cell, where only the signal on the MTJ is sensed, this cell amplifies the internal voltage of the cell. Each of the 2T–1R cell topologies utilizes an external port to read the cell state. Both cells are connected to the MTJ at node B (see Fig. 1(b)). The increasing voltage difference observed at node B increases the sense margin observed at the output.

Current ratio: The current ratio of the diode connected memory cell is shown in Fig. 8(b) for a nominal threshold voltage. The array voltage bias has a strong effect on the current ratio. Increasing both the voltage bias and the width of the NMOS transistors within the array increases the current ratio to 151. However, operating at this point is close to writing to the MTJ and provides a small current margin. With a minimum current margin of at least 1 μA, the maximum achievable current ratio is 127, 1.4 μA/11 nA. Note that a relatively high resistance for the read circuitry is assumed as compared to the write driver circuitry to mitigate inadvertent writes within the data array.

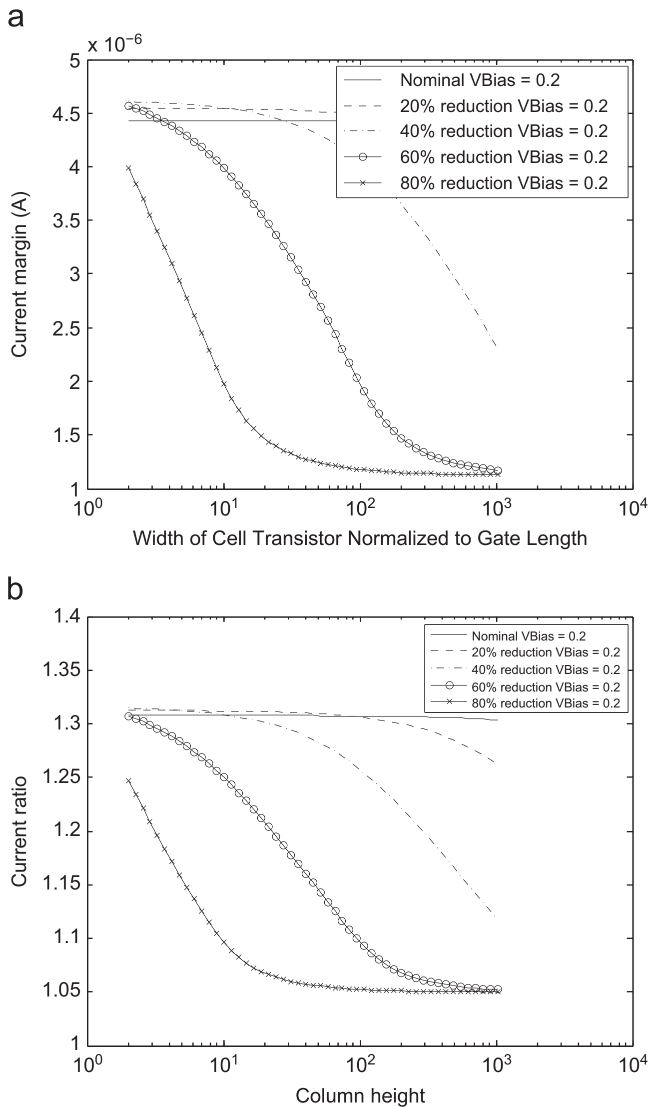

Fig. 7. Effect of increased data array size on 1T–1R memory cell at multiple threshold voltages. (a) Current margin and (b) current ratio.

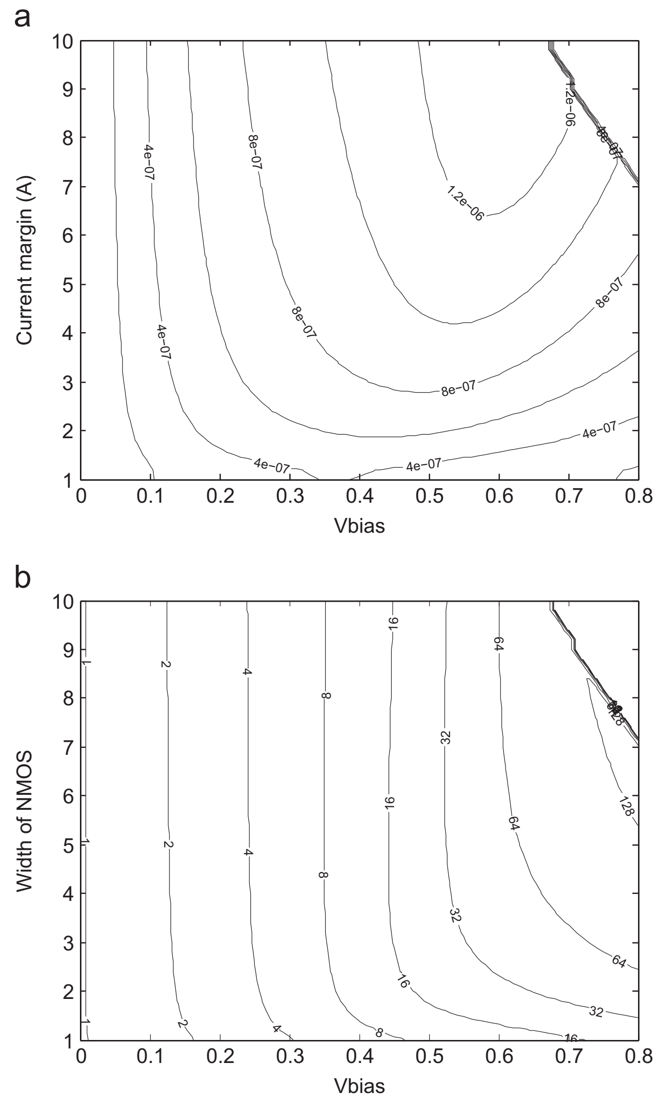

Fig. 8. Design space for 2T–1R diode connected cell at nominal threshold, (a) current margin and (b) current ratio.

The size of the data array transistor has little effect on the output current ratio or current margin. Only at high bias (above 0.4 V) does the current margin increase with transistor size. The diode connected cell is therefore more tolerant to transistor variations than the 1T–1R cell. Additionally, the density advantage can be exploited while producing a higher current ratio. At a relatively small size (2*F*), the diode connected cell achieves a peak current ratio of 50.3. This advantage, however, is achieved at a low current margin of 0.35 μA. In this case, I_{off} falls at a faster rate than I_{on}; however, the magnitude of both currents decreases, causing a reduction in current margin with an increase in the current ratio.

Current margin: The current margin, however, can be further improved by reducing the threshold voltage of the data array transistors, as shown in Fig. 9(a). A 20% reduction in the threshold voltage doubles the current margin for a minimum sized device. At larger device widths, the current margin is greater than 1 μA while suffering minimal loss in current ratio. A 40% reduction is sufficient to allow a 2*F* transistor to supply a 1 μA current margin while maintaining a current ratio of 8.

Array size: Similar to the 1T–1R memory cell, there is a penalty associated with reducing the threshold voltage. For a 60% reduction in threshold voltage, an array column height of 1024 bits produces a drop in current ratio from 6.7 × to 3.3 ×, as shown in Fig. 10. Unlike the 1T–1R memory cell, the current margin is relatively independent of the size of the array and increases by 0.5 μA with a 60% reduction in threshold voltage. Moreover, for both 20% and 40% reductions in threshold voltages, both the current ratio and current margin remain relatively constant (below 0.2% variation) with increasing array size. The reduced threshold voltage does not affect the voltage signal, as in the case of the 1T–1R cell.

Tradeoff between current margin and current ratio: Note the tradeoff between the current ratio and current margin. The diode connected cell alternates between cutoff and saturation. Increasing the internal voltage (node B, shown in Fig. 4(a)) increases the gate bias for the on state MTJ and the current through the diode connected transistor. The higher voltage, however, also increases the voltage at node B in the MTJ off state. Since the current in cutoff is an exponential function of the transistor bias, and only quadratic in saturation, the current ratio drops.

5.2.3. 2T–1R gate connected memory cell

As previously mentioned, the external port of the 2T–1R cells separates the read operation from the write operation. Similar to the diode connected cell, the circuit depends on the internal cell

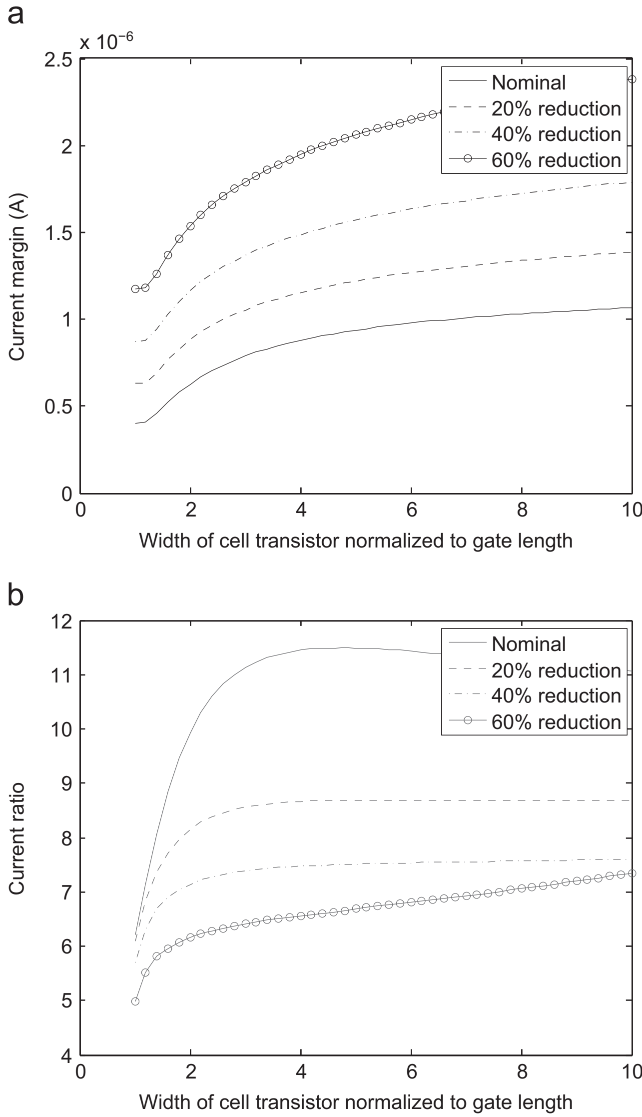

Fig. 9. Effect of reduced threshold voltage on 2T–1R diode connected cell for increasing size of data array transistors. (a) Current margin and (b) current ratio.

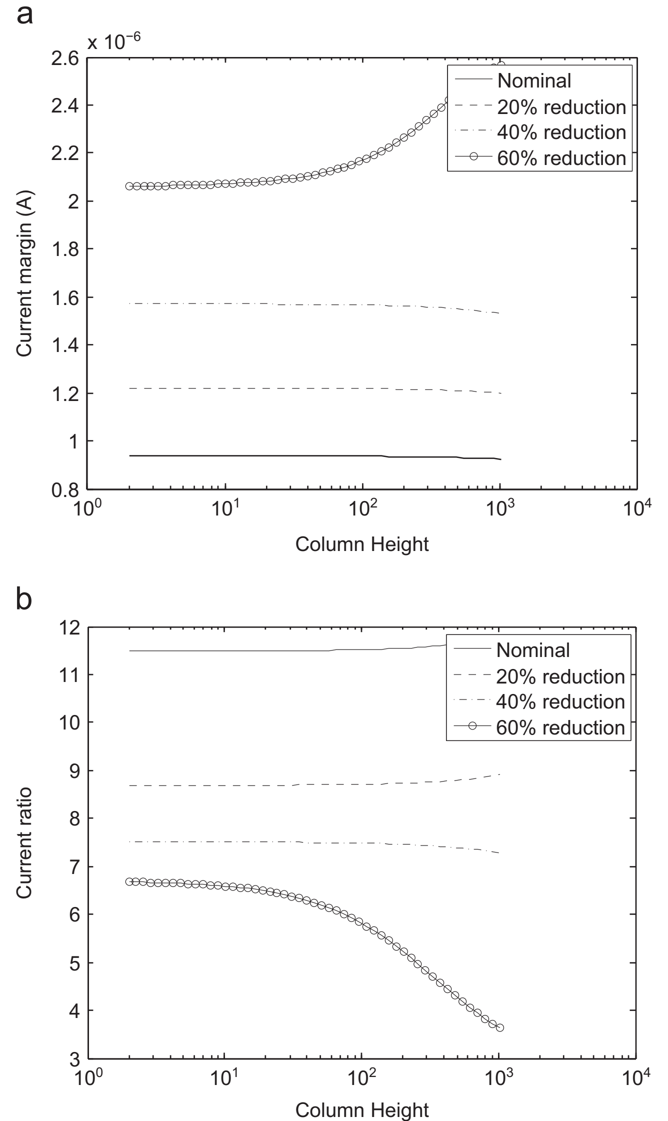

Fig. 10. Effect of array size on 2T–1R diode connected cell for reduced threshold voltage of data array transistors. (a) Current margin, and (b) current ratio.

voltage at node B. Correct operation of the 2T–1R gate connected cell requires the transistor gate voltage to be sufficiently large to switch the transistor between the two MTJ resistive states.

The current ratio and current margin for a gate connected memory cell is shown in Fig. 11 for varying access transistor sizes and array biases. Unlike the 1T–1R case, increasing the array bias has a strong effect on the current ratio. For full bias, the gate connected transistor achieves a current ratio of 2.2. Counterintuitively, increasing the cell transistor size reduces the current ratio. This behavior is due to the dependence of the internal voltage of the cell (node B) on the voltage drop across the transistor. A linear reduction in transistor size leads to a reduced voltage drop and voltage change at node B (see Fig. 4(a)).

The effect of a reduced threshold voltage is depicted in Fig. 12. A reduction in the threshold voltage enhances the current margin. For example, a 40% reduction in the threshold current is sufficient to increase the current margin above 1 μA. This reduction lowers the current ratio from a peak of 1.7 to 1.4 at 2*F* transistor sizing.

Similar to the 2T–1R diode cell, the gate connected cell is independent of the array size as a function of technology, as depicted in Fig. 13. This characteristic occurs since the gate connected transistor is always grounded at the source terminal and electrically isolated from the MTJ.

5.3. Comparison of current margin and ratio across memory cells

Both the gate connected cell and the diode connected cell improve the current ratio (or margin) observed at the sense circuity by providing additional read ports. The diode connected cell produces the largest increase in current ratio. The current margin of the diode connected cell is limited by the large on-resistance of the diode connected transistor. This issue can be addressed, however, by reducing the threshold voltage of the devices within the data array. This reduction in threshold voltage provides additional current at high bias conditions, either decreasing the switching times or improving density through smaller access transistors. Moreover, this reduction does not degrade the current ratio or current margin with increasing array size as with the 1T–1R memory cell. Intuitively, the target current can be linearly increased by widening the gate connected transistor while maintaining the same width of the access transistor.

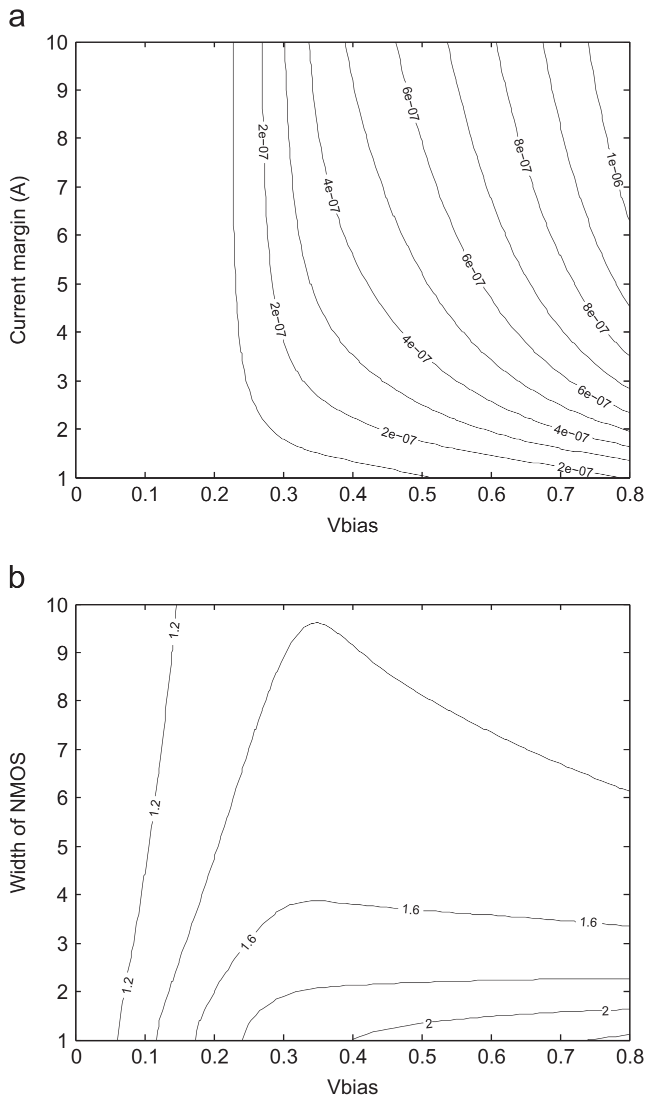

Fig. 11. Design space of 2T–1R gate connected cell for nominal threshold 2T–1R gate connected cell. (a) Current margin and (b) current ratio.

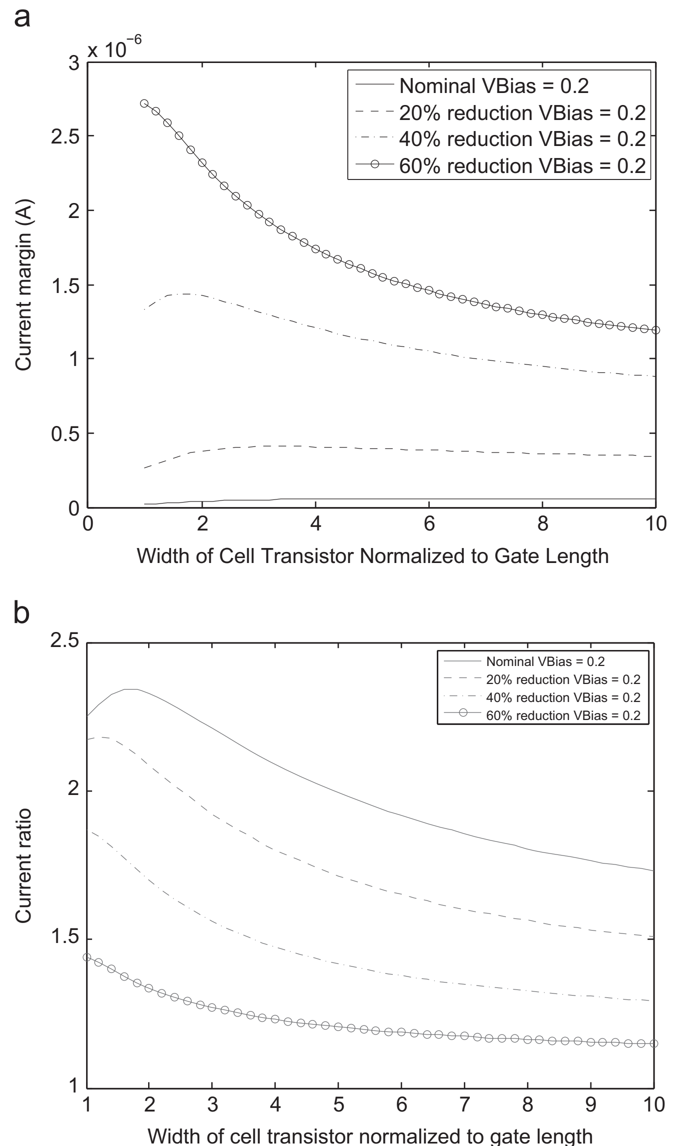

Fig. 12. Effect of reduced threshold voltages on 2T–1R gate connected cell for increasing data array transistor width. (a) Current margin and (b) current ratio.

5.4. Comparison of SRAM and STT-MRAM memory cells

A comparison of 8T SRAM with STT-MRAM memory cells in terms of read delay, read energy, and physical area is listed, respectively, in Tables 2, 3 and 4. The SRAM read ports (RP) and write–read ports (WRP) are evaluated for both memory specific high density (HD) and logic process (Logic) design rules [23]. Note that the 8T SRAM is selected as the benchmark due to the use of 8T SRAM for high performance caches in sub-45 nm technologies [24]. The wordline energy associated with a 8T SRAM cell is negligible as compared to the bitline power. Each memory cell and the associated parasitic impedances are scaled to the 22 nm technology node in the same manner as described in Section 5.1. The 8T SRAM read port (RP) is sensed using a standard single-ended inverter sense amplifier [25]. The SRAM write–read port is sensed using a standard dynamic latch sense amplifier [26]. Each of the STT-MRAM cells is sensed using a clamped bitline sense amplifier [27]. The array sizes are typical of an on-chip cache array.

Delay metrics for square array sizes ranging from 128 to 2048 bits are listed in Table 2. STT-MRAM arrays exhibit significantly less delay than the SRAM counterparts. At array sizes of 2048 cells, the delay of SRAM and STT-MRAM is dominated by the wordline delay. The STT-MRAM has an advantage over SRAM since only one transistor is required to select the cell. Additionally, the reduced length of the wordline further reduces the delay. The write–read port of the 8T SRAM cell is sensed differentially and thus compensates this increased delay. This effect is more clearly observed at the smaller SRAM arrays where the singled-ended read port delays are a factor of three longer than the write–read port read time. Each of the STT-MRAM memory cells is also read in a single ended manner. As compared to the single ended SRAM read port, the delay of each STT-MRAM memory cell type is smaller by a factor of 3.9, 4.6, and 5.37, respectively, for the 1T–1R, 2T–1R gate connected, and 2T–1R diode connected memory cells. Both the gate and diode connected cells exhibit an area overhead larger than the 1T–1R cell but overcome this issue through an improved current ratio which reduces the delay.

The energy consumption of each of the cell types is listed in Table 3. Each of the cell types exhibits a significant reduction in energy consumption with a smaller data array. The gate connected and diode connected cells plateau at an energy compatible to SRAM arrays at smaller sizes. This behavior is due to the additional bias required to drive the internal node of the cell. The 1T–1R cell does not require an additional bias, enabling more energy efficient

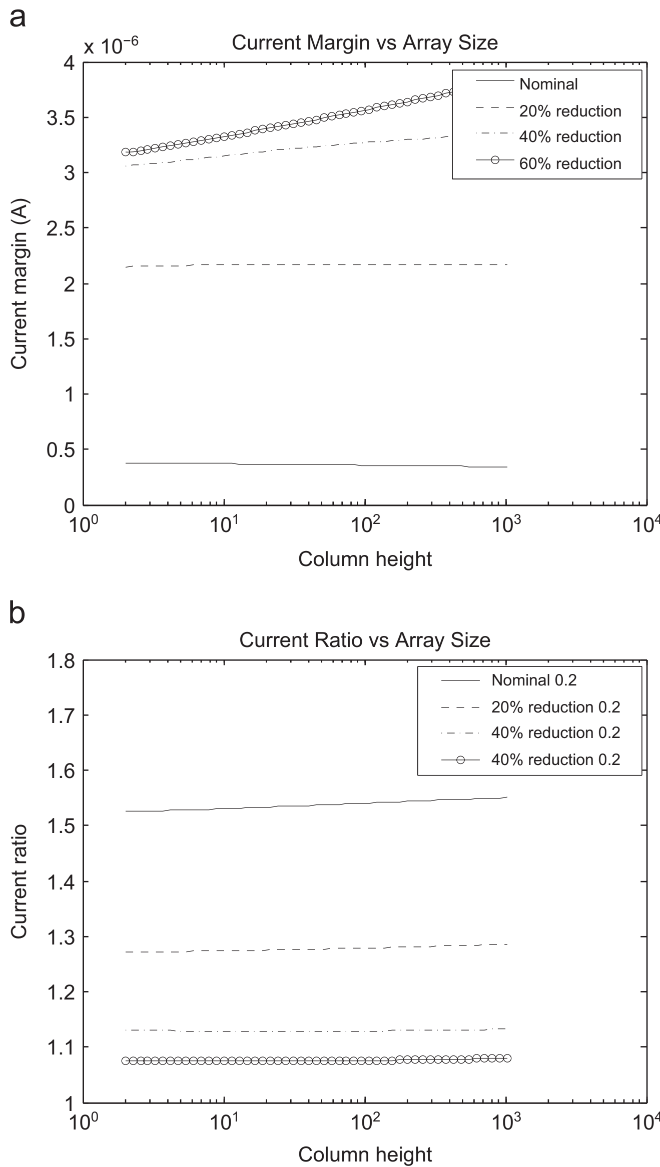

Fig. 13. Effect of array size on 2T–1R gate connected cell for reduced threshold voltages. (a) Current margin, and (b) current ratio.

reads than the other memory cell types. At larger array sizes, the 2T–1R cell variants require more energy than the other cell types. The additional area occupied by the logic version of the 8T SRAM cell has little effect on the per bit energy. The word line energy is spread over the length of the row during accesses. This effect can also be observed between the diode and gate connected cells, as the gate connected cell is more energy efficient than the diode connected cell despite the larger area of the diode connected cell.

Between each of the memory types, the SRAM requires longer delays and greater energy than the STT-MRAM memory. In general, the 1T–1R outperforms SRAM for all array sizes. Both the 2T–1R cells require more energy at large array sizes, indicating that each topology is better suited to small active on-chip caches where speed is paramount. At these sizes, the 2T–1R topology exhibits the fastest read operation of any memory cell type at a energy consumption comparable to SRAM.

6. Conclusions

Two topologies are proposed to complement the standard 1T–1R topology commonly used in STT-MTJ based memories. The diode-connected memory cell demonstrates greater than an order of magnitude improvement in the output current on/off ratio. The diode cell, due to the small area and high output current ratio, is therefore the most effective at increasing the current ratio as compared to the other cell topologies. The gate connected cell can, however, be more easily expanded into a multi-port cache structure due to electrical isolation between the internal node of the memory cell and the output port. Furthermore, the current margin of the gate connected cell can be increased irrespective of cell bias by increasing the size of the gate connected transistor. The relative importance of the current margin as compared to the current ratio determines the applicability of each cell for a particular data array. A comparison of each of the memory cells to an 8T SRAM cell

Table 4
Area comparison.

Cell Characteristics	SRAM 8T HD	SRAM 8T logic	1T–1R	2T–1R diode	2T–1R gate
Cell height (***F***)	8	8	7	7	7
Cell width (***F***)	31.6	45.4	6.65	10.8	14.5
Density (F^2)	252	363.2	46.55	75.6	101.5

Table 2
Single bit access delay (ns).

Number of bits	SRAM 8T HD RP	SRAM 8T HD WRP	SRAM 8T logic RP	SRAM 8T logic WRP	1T–1R	2T–1R gate	2T–1R diode
2048	14.879	14.708	25.793	26.927	3.106	4.200	3.762
1024	4.471	3.716	7.189	6.754	0.718	1.242	0.969
512	1.537	0.960	2.219	1.721	0.265	0.377	0.295
256	0.626	0.273	0.800	0.466	0.127	0.139	0.111
128	0.306	0.094	0.352	0.145	0.078	0.067	0.057

Table 3
Single bit access energy (fJ).

Number of bits	SRAM 8T HD RP	SRAM 8T HD WRP	SRAM 8T logic RP	SRAM 8T logic WRP	1T–1R	2T–1R gate	2T–1R diode
2048	31.182	28.529	31.197	28.561	5.382	50.285	98.113
1024	19.144	18.243	19.175	18.274	1.081	26.014	39.430
512	12.093	12.014	12.124	12.045	0.568	12.559	17.441
256	6.047	6.235	6.078	6.266	0.370	6.250	7.891
128	2.736	2.973	2.767	3.004	0.284	3.170	3.620

shows that these additional cell topologies are advantageous in small area high speed on-chip caches.

Appendix A. Parameter selection

An STT-MRAM array can be modeled as a simple two resistor circuit. This discussion describes this two resistor model and presents expressions to maximize the sense margin. The linear resistor model is applied to produce an initial design for the 2T–1R cells.

A.1. Two resistor model

A data array can be modeled as a two resistor model where the sense node (node S) is used for sensing, as shown in Fig. 14. In this structure, R_{bot} toggles between the two resistance states, $R_{bot_{on}}$ and $R_{bot_{off}}$. In a manner analogous to the TMR of an MTJ, the switching ratio (SR) of R_{bot} is defined as

$$SR \equiv \frac{R_{bot_{off}} - R_{bot_{on}}}{R_{bot_{on}}}. \quad (A.1)$$

The sense margin (ΔV_A) for this structure is the change in the maximum voltage at node S:

$$|\Delta V_A| = V_A|_{R_{bot_{off}}} - V_A|_{R_{bot_{on}}}. \quad (A.2)$$

This difference produces the largest swing at node S, which in the aforementioned model represents the voltage detected by the sense circuitry. The maximum change in voltage, *i.e.*, the maximum sense margin [28], occurs under the constraint:

$$R_{top} = \sqrt{(R_{bot_{on}})(R_{bot_{off}})}. \quad (A.3)$$

From (A.3), the voltage sense margin can be expressed as

$$|\Delta V_A| = \frac{\sqrt{1+SR}-1}{\sqrt{1+SR}+1} V_{bias}. \quad (A.4)$$

For current sensing, the sense margin ΔI is the change in current passing through the MTJ, where

$$|\Delta I| = I_{R_{top}}|_{R_{bot_{on}}} - I_{R_{top}}|_{R_{bot_{off}}} = \frac{R_{bot_{on}}(SR)V_{bias}}{R_{bot_{on}}^2 + 2R_{bot_{on}}R_{top} + R_{top}^2 + (R_{bot_{on}}^2 + R_{bot_{on}}R_{top})SR}. \quad (A.5)$$

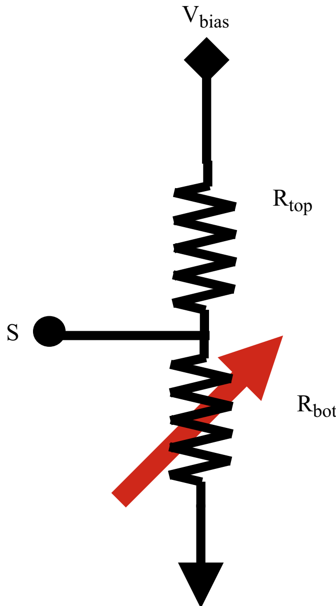

Fig. 14. Two resistor model of an STT-MRAM array.

Intuitively, increasing the voltage through the network increases the voltage sense margin by increasing the voltage drop across the switching resistor. Reducing the resistance of R_{top} monotonically improves the current sense margin through the path. A 2T–1R data cell, however, produces current through an adjacent read port. Maximizing the voltage margin at node B in Fig. 4(a), therefore, produces the largest current ratio and margin.

2T–1R *data array*: The voltage margin of the 2T–1R cell is increased by substituting the resistances illustrated in Fig. 4(a) into R_{top} and R_{bot}:

$$R_{top} = R_{tp} + R_{bl} + R_{mtj}, \quad (A.6)$$

$$R_{bot} = R_{bl} + R_{tn} + R_{m}, \quad (A.7)$$

$$SR = \frac{R_{on}TMR}{R_{on} + R_{tp} + R_{bl}}. \quad (A.8)$$

These expressions maximize the voltage difference at node B, the central node within the memory cell (rather than the bitline at node A, as in the case of the 1T–1R data array). By maximizing the voltage difference at node B, the additional gain produced at the output of both the diode connected and the gate connected cell read ports is greatly increased.

A.2. Design parameter selection

The target MTJ write current is specified by the MTJ technology along with the on-resistance of the write drivers determined from the CMOS technology parameters. The expression

$$R_{total} = \frac{V_{dd}}{I_c} = R_{mtj} + R_{tp} + R_{tn} + R_{m}, \quad (A.9)$$

describes the constraint placed by the MTJ write current on the cell size. The size of the transistors is determined from (A.2) to (A.9). These expressions produce the greatest change in output current for both types of 2T–1R cells. For the 2T–1R diode connected cell, the output port voltage exceeds the voltage at node B in Fig. 4(a) by the threshold voltage of the diode connected transistor. This higher voltage ensures that the diode switches between the on and off states when the MTJ is, respectively, off and on. A sweep of the bias voltage can be conducted to determine the location where the current ratio is maximum. The gate connected cell does not exhibit this limitation.

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