between driver drain region and load drain region for MOS FETs in SOS CMOS inverter structure.

As a consequence, SOS CMOS devices with N^- drain junction using double SPE technology for thin SOS films should be the most promising technology for 1μm high-speed, highly reliable and low power dissipation VLSI, when other essential SOS features, such as latch-up free operation, high soft error tolerance and good radiation hardness, are considered.

Radiation-hard CMOS/SOS: an ideal technology for the space environment

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1. Introduction

Recent breakthroughs in the radiation-hardened (rad-hard) CMOS/SOS (silicon-on-sapphire) technology at RCA now make possible the consistent manufacture of a broad spectrum of devices tolerant of all critical radiation: neutron, transient, total dose, and cosmic ray. Among these devices are 4k RAMs (1024×4 and 4096×1) that are total-dose hardened to greater than 100,000 rads (Si), that provide cosmic-ray upset immunity to less than 2×10^{-9} erros/bit day, and that are not upset by transient doses of up to 1×10^{11} rads/sec.; SOS devices cannot latch up at any level. These RAMs and other rad-hard devices are specifically designed for advanced spacecraft computers and control instrumentation.

Many additional CMOS/SOS devices have been manufactured by means of the rad-hard process, including processors, controllers, a multiplier, ROMs, and gate arrays. Performance and reliability data for these devices will be reviewed.

2. Acknowledgment

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A two level metal, software compatible, CMOS/SOS gate array family

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A family of radiation hardened CMOS/SOS gate arrays consisting of three chip types has been designed and processed, utilising two self-aligning silicon gate technologies. The gate

arrays employ complementary MOS devices on a sapphire substrate with two levels of metal, providing both high performance and low power consumption. These gate arrays are configured with three programmable mask layers (metal 1, via, and metal 2), are compatible with in-house automatic placement and routing software, and each has a comprehensive macrocell library.

All three of these configurable gate arrays have a similar structure, each being made up of rows of two-input gates separated by routing channels. Since most logic configurations in gate arrays tend to concentrate in the centre of the die, additional interconnect area is allocated in the central channels with progressively less track capacity toward the perimeter. The I/O buffers surrounding the internal array can be configurated into nine different kinds of interface circuits.

The first chip, a 1K gate array with 112 I/O buffers, utilises a 3.5 micron technology. Two additional gate arrays, a 1K and a 2K with 84 and 128 I/O buffers respectively, employ a 2.5 micron technology. Many chip implementations have been designed for various internal Hughes systems with utilisations approaching 80% of the programmable cells. The circuit functions range in diversity from a 24-bit barrel shifter to a 10-stage 4-bit synchronous counter. High functional yields have been achieved with signal frequencies ranging between 5 and 30MHz.

The detailed characteristics of the gate array topology will be described as well as an analysis of the effect of the variable channel regions on routing efficiency. This will be described in terms of an empirical analysis of track density versus gate-to-pin ratio and compared to real examples. Simulated and experimental characterisations of the two SOS technologies will be discussed.

The double level metal process will be described, particularly the effect of the additional step inherent in air-isolated SOS structures. Finally, the automated design system's compatibility with the gate array family will be described in terms of both the generic and general input requirements.