A system for critical path analysis based on back annotation and distributed interconnect impedance models

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This paper describes a VLSI CAD system that automatically selects optimal interconnect impedance models and embeds them into circuit simulation files each identified as a critical worst case timing path. The CAD system initially identifies pre-layout critical timing paths and back annotates these paths with post-layout interconnect impedances. Accurate post-layout resistive and capacitive interconnect impedances are automatically extracted, their magnitudes are compared to the path specific device dependent RC loads of each cell-to-cell node, and an appropriate RC lumped model is selected to optimally model the distributed nature of the RC interconnect impedance of that particular cell-to-cell node. These interconnect RC impedance models are then back annotated into a SPICE formatted circuit simulation file for the precise determination of the timing behaviour of these critical paths. Therefore, timing accuracy and CPU efficiency are optimised on a node by node basis. This analysis system is tailored to support high performance circuits while maintaining automated layout database independence and maximal design flexibility.

1. Introduction

Comprehensive detailed circuit analysis has traditionally been an important bottleneck in VLSI circuit design for two main reasons. The first is the large amount of time required for manually identifying all possible critical signal paths from among thousands of total paths that can exist in a VLSI circuit. The second is the tedious construction of a circuit simulation file and the use of manually operated iterative optimisation techniques for accurately analysing these critical signal paths. Many papers have been published which individually discuss timing analysis[1-4], interconnect parasitic extraction[5,6], distributed interconnect parasitic impedances[7], and back annotation[8]. Other papers on VLSI design systems and their methodologies[9-12] discuss the relative importance and utility of these capabilities. However, minimal work has been performed to automatically embed optimal circuit netlist models into detailed circuit simulation files based on back annotation of accurately modeled interconnect impedances. This paper presents a CAD system which identifies pre-layout critical timing paths, annotates these paths with post-layout interconnect impedances which are modeled in an optimally accurate fashion, and inserts these RC impedances into circuit simulation files developed for each critical path. This system has been specifically tailored to support high performance VLSI complexity circuits while maintaining automated layout database independence and maximal design flexibility.

2. System overview

This integrated timing analysis system is composed of two tools that work in concert with each other to generate multiple circuit simulation files accurately representing a circuit's

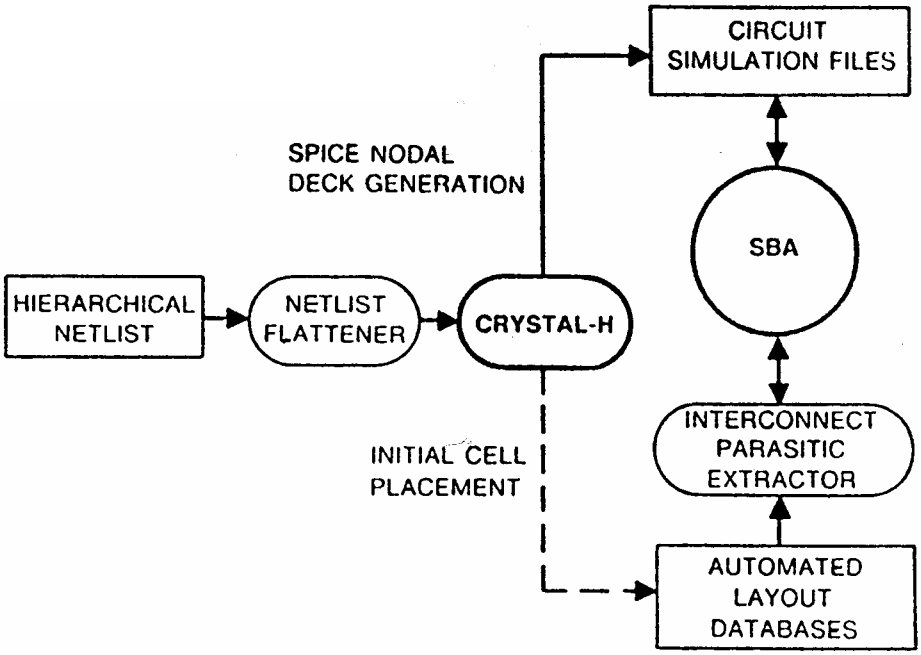

Fig. 1 Iterative performance optimisation environment based on back annotation of interconnect impedances

critical timing paths. This CAD system utilises a unified data structure, thereby making it compatible with virtually any existing automated layout systems. Fig. 1 illustrates the use of the system in a VLSI circuit design and analysis environment.

2.1 Generation of a critical path's circuit simulation file

In order to determine which paths in a VLSI circuit are constrained by their timing behaviour, a timing analyser is used to identify critical paths. The timing analyser used is Crystal-H, a modified version of the University of California at Berkeley's timing analyser program[13], Crystal-2. It performs CMOS transistor level pre-layout worst case path selection based on user defined inputs. The critical signal paths identified by Crystal-H are formatted into nodal decks in SPICE format, each containing a worst case critical timing path. All unused input pins of branch cells along the critical circuit path are automatically grounded while all output pins not belonging to the circuit path are tied to predefined load capacitors.

2.2 Automatic back annotation of interconnect parasitic impedances

In order to analyse accurately the effect of interconnect impedances on circuit performance, a CAD system for automatically extracting parasitic interconnect impedances and embedding them into a circuit simulation file predefined by Crystal-H has been developed. This tool is our Simulation Back Annotation (SBA) program. SBA accepts multiple nodal decks formatted by Crystal-H and invokes an in-house developed Parasitic Extraction program[5] to determine accurate parasitic resistive and capacitive interconnect impedances for each intercellular net. The Parasitic Extractor program references an automated layout database to determine the specific technology dependent interconnect parasitic impedances for the specific nets along the critical path. These lumped interconnect parasitic

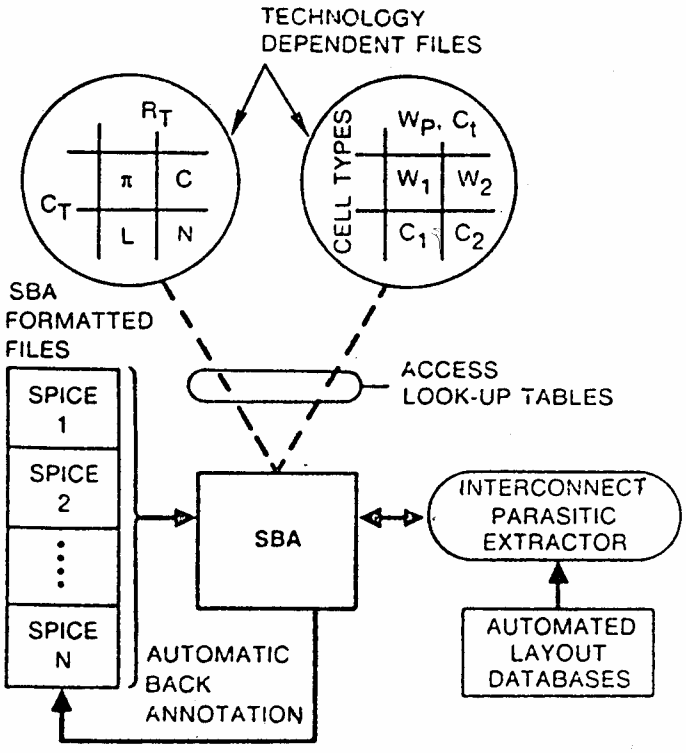

Fig. 2 Automatic back annotation based on optimal selection of lumped interconnect models

impedances, R_W and C_W, are used to compute the ratios, $R_T = \frac{r_t}{R_W}$ and $C_T = \frac{C_t}{C_W}$, after accessing one of two technology specific look-up tables, as shown in Fig. 2. r_t and C_t represent the device dependent output resistance and load capacitance and are defined below. These ratios are used to select one of seven different lumped interconnect impedance networks, π3, π2, π1, L, R, C, or N (see Fig. 3) for each RC load from the second technology specific look-up table, as depicted in Fig. 2. Once the impedance network is optimally selected, SBA automatically back annotates the SPICE nodal decks with the appropriate interconnect impedance network configuration. Distributed impedance model selection and back annotation can be iteratively changed as the layout's routing is optimised. Fig. 2 illustrates the total SBA environment.

3. Circuit analysis

It is common practice within the industry to use a lumped one-section ladder network to model distributed RC transistor interconnect load impedances. This lumped network guarantees an upper bound (i.e., worst case) time delay for critical path timing analysis and a minimum number of nodes for CPU computational efficiency. However, this upper bound can lead to appreciable circuit over-design which increases with the relative magnitude of the interconnect delay between register elements in a data path. Thus, a more accurate representation of the interconnect delay will permit the design of higher performance circuits. Therefore, the design technique described within this paper is directly oriented to high speed and high precision VLSI circuit design.

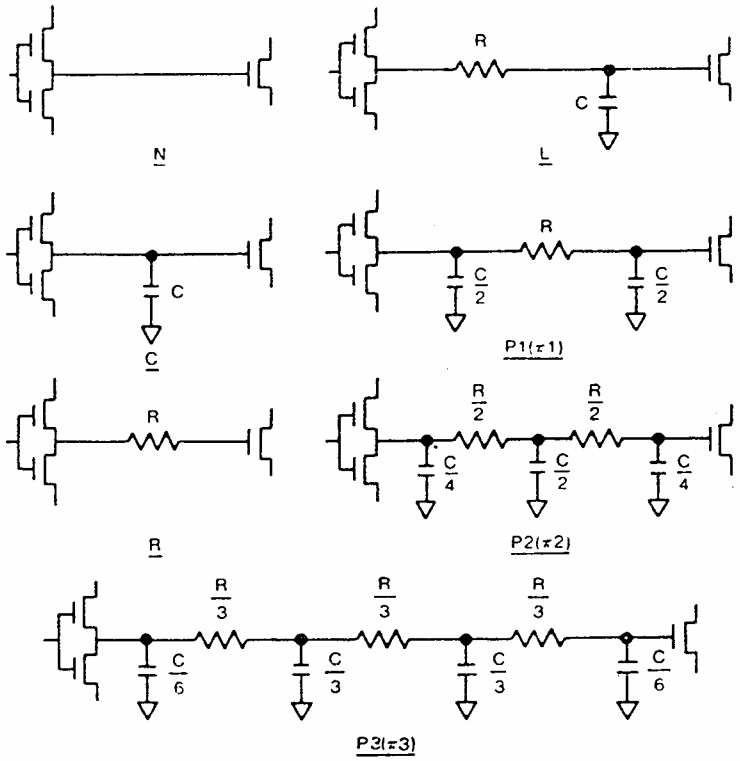

Fig. 3 Lumped circuit models used to approximate distributed RC interconnect impedance

3.1 Definition of symbols

W_p : PMOS transistor width (micrometres)
R_w : Lumped wire resistance (ohms)
C_w : Lumped wire capacitance (femtofarads)
r_t : Lower bound transistor output impedance, $\left(\frac{1}{\text{max drain conductance}}\right)$ (ohms)
C_t : Lumped transistor input capacitance (femtofarads)
V_{in} : MOS transistor input voltage (volts)
V_{tp} : PMOS transistor threshold voltage, negative for enhancement devices (volts)
V_{dsp}, V_{dsn} : PMOS and NMOS transistor source-drain voltages, respectively (volts)
V_{DD} : Power supply voltage (volts)
α : Relative Modulation Factor between r_t and W_p (dimensionless)
β_p : PMOS transistor gain factor $\left(\frac{\text{farads}}{\text{volt-second}}\right)$

$C_T = \frac{C_t}{C_w}$, ratio of the transistor input capacitance to the lumped wire capacitance

$R_T = \frac{r_t}{R_w}$, ratio of the transistor output resistance to the lumped wire resistance

3.2 Calculation of CMOS output impedance

The output impedance of a driver is a complex relationship among several factors such as a device's process parameters, the shape of the input transient waveform, the output resistive and capacitive loading, the circuit environmental conditions, and the layout design style. Lower r_t bounds are used in this design technique since they are more sensitive to capacitive interconnect impedances and thereby require greater accuracy of the distributed interconnect impedance models.

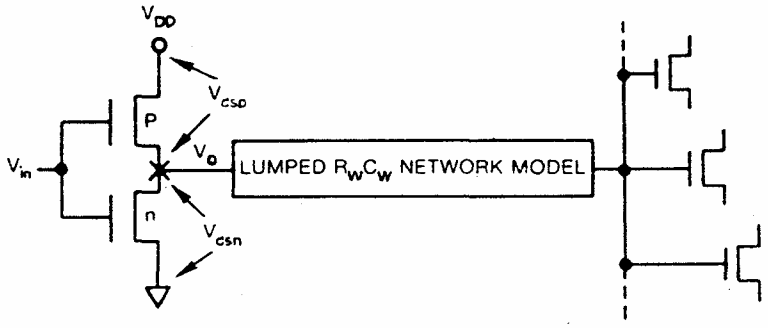

Fig. 4 CMOS ratioed buffer driving interconnect and device loads

The drain current equations of a typical ratioed buffer represented in Fig. 4 which correspond to a minimum PMOS output impedance are defined below[15]:

$$I_{dsp} = -\beta_p [(V_{in} - V_{DD} - V_{tp})(V_{dsp}) - \tfrac{1}{2}V^2_{dsp}] \quad \left.\begin{array}{l} V_o \leqslant V_{in} - V_{tp} \\ 0 \leqslant V_{in} \leqslant V_{tn} \end{array}\right\} \quad (1)$$

$$I_{dsn} = 0 \quad \left.\begin{array}{l} \\ |V_{tp}| \leqslant V_o \leqslant V_{DD} \end{array}\right\} \quad (2)$$

where,

$$\beta_p = \frac{W_p}{L_p} \mu_p C_{ox} \quad (3)$$

The above equations define the drain current of a PMOS transistor when operating in the linear mode and the drain current of a NMOS transistor when operating in the cutoff mode. Since the PMOS and NMOS devices are assumed to be geometrically ratioed, the drain-to-source current is equivalent for both devices when operating in the same I-V region. As the input voltage V_{in} and the drain voltage V_{dsp} approach zero, the PMOS lower bound output impedance will approach r_t as described in equations (4) and (5) below.

$$(r_t)^{-1} = \lim_{V_{in},\, V_{dsp} \to 0} \frac{dI_{dsp}}{dV_{dsp}} = \beta_p (V_{DD} + V_{tp}) \quad (4)$$

Therefore,

$$r_t = \frac{1}{\beta_p (V_{DD} + V_{tp})} \quad (5)$$

The transconductance of a device, $(r_t)^{-1}$, is linearly dependent upon its width as described by equations (3) and (5). The larger the device width, the greater its transconductance. This relationship between device output impedance and geometric width is shown in equation (6). Thus, for a given value of α, process parameters, and bias conditions, r_t can be determined directly from W_p.

$$r_t = \frac{1}{\beta_p (V_{DD} + V_{tp})} = \alpha \frac{1}{\beta_p V_{DD}} = \alpha \frac{1}{W_p} \frac{L_p}{\mu_p Cox} \frac{1}{V_{DD}} \tag{6}$$

where,

$$\alpha = \frac{V_{DD}}{V_{DD} + V_{tp}} \text{ and } \beta_p V_{DD} \text{ is described in reference 16.} \tag{7}$$

α is always larger than one for a typical enhancement PMOS device since V_{tp} is negative. Thus, one can determine the device output impedance directly from a given device geometric width under a given set of environmental conditions.

The Relative Modulation Factor α is sensitive to the circuit environment as depicted in Table 1 since both V_{DD} and V_{tp} can change. V_{tp} is depicted in Table 1 as an implicit function of temperature and process parameters. This table has been calibrated for an in-house CMOS technology. The dependence of V_{tp} on α and V_{DD} can be explicitly described and this relationship is defined in equation (8) below.

$$V_{tp} = V_{DD} \left(\frac{1-\alpha}{\alpha} \right) \tag{8}$$

Thus, precharacterised data from Table 1 provide a precise measure of the effect of various environmental conditions on the magnitude of the P-channel threshold voltage. Values of r_t have been determined by Sakurai[7] with the added sophistication of considering the effect of varying circuit environmental conditions on the value of α. Thus, for a given value of α, an estimate of the output resistance of a ratioed buffer can be made and this value can be used to optimally model that output node's interconnect impedance.

TABLE I Values of the relative modultation factor α as a function of circuit environmental conditions

V_{DD}(V)	TEMP (°C)	PROCESS PARAMETERS	α
4.5	27	BEST	1.50
4.5	85	NOMINAL	2.23
4.5	125	WORST	2.92
5.0	27	BEST	1.34
5.0	85	NOMINAL	2.01
5.0	125	WORST	2.61
5.5	27	BEST	1.22
5 5	85	NOMINAL	1.83
5.5	125	WORST	2.37

3.3 Determination of optimal interconnect impedance network

For each cell type in a given cell library, the input capacitive load and the output drive resistance described in terms of P-channel device width is defined in a look-up table, exemplified by Table 2. From these values of r_t and C_T, each node's interconnect impedances (R_w and C_w), and a user defined value for α, SBA computes the ratios R_T and C_T. These ratios represent the relative magnitude of the transistor impedance, r_t and C_t, to its interconnect impedance, R_w and C_w, as described in equations (9) and (10) below.

$$R_T = \frac{r_t}{R_w} \tag{9}$$

$$C_T = \frac{C_t}{C_w} \tag{10}$$

TABLE II Lumped interconnect circuit models used by SBA to model distributed RC interconnect impedance

C_T \ R_T	0	0.1	0.2	0.3	0.75	1.5	2	5	20	100
0.1	π3	π3	π3	π2	π1	π1	L	C	C	
0.2	π3	π2	π2	π1	π1	π1	L	C	C	
0.5	π2	π2	π1	π1	L	L	L	C	C	
1	π1	π1	π1	π1	L	L	L	C	C	
2	π1	π1	π1	L	L	L	L	C	C	
3	π1	L	L	L	L	L	L	C	C	
5	L	L	L	L	L	L	L	C	C	
20	R	R	R	R	R	R	R	C	C	
100	R	R	R	R	R	R	R	C	N	

After computing R_T and C_T, SBA accesses a second look-up table, as described in Table 2, to select an optimum lumped network model for each net under study. Table 2 was constructed based on the relative error of the signal transition time between a one-section ladder network and a one-section π network[17] for various values of R_T and C_T. Table 2 assumes that an L network is chosen over a one-section network when the relative signal transistion error is less than 10%. When the relative error is between 10% and 35%, a two-section π network is chosen while a three-section network is chosen for larger errors. Thus, a favourable compromise position between circuit accuracy and computational efficiency is maintained.

The choice of error breakpoint is both technology and design style dependent and can be

TABLE III SBA VAX 11/750 CPU time benchmarks which include parasitic database read-in time. Each delay stage requires a lumped RC network annotation

NUMBER OF CRITICAL PATHS	NUMBER OF DELAY STAGES	CPU TIME (MINUTES)
5	74	02:25
10	130	03:39
25	273	06:32
50	649	12:38

varied for different design constraints. The relative error describes the percentage improvement in accuracy that one can achieve when using a more accurate interconnect impedance model. A π network is used instead of a T network since it utilises fewer nodes and is therefore more computationally efficient since the computational efficiency of SPICE is directly dependent upon the size of its nodal matrix. For values of R_T and C_T greater than 5, relative errors between L, R, C, and N networks less than 10% dictate the selection of a simple R, C, or N network model. For large values of R_T, the interconnect resistance is of negligible consequence and the interconnect model can be represented as a simple capacitor. For large values of C_T, the interconnect model can be represented as a simple resistor. For large values of both R_T and C_T, no RC interconnect impedance model is necessary and this is symbolically represented as an N network model. Thus, the user defined factor combined with the two technology dependent look-up tables, Tables 2 and 3, define an appropriate RC network for modelling a wire's distributed interconnect impedance which accurately represents the distributed RC load for specific R_T and C_T ratios.

4. Illustration of results

This system has been used to interface to two automated layout databases, an in-house developed system, HAL (Hughes Automated Layout) and a commercially developed system, SDA (Silicon Design Automation). The input to Crystal-H is a netlist in TDL (TEGAS Design Language) format. The outputs are SPICE files formatted by SBA where each file contains a critical path identified by Crystal-H. Fig. 5 shows an example of an SBA format-

```
RESERVED  SOURCE      SOURCE          TARGET      TARGET CELL   RESISTANCE     NET        CAPACITANCE    NET
WORD      CELL        CELL INSTANCE   CELL        INSTANCE      NAME TO BE     NAME       NAME TO BE     NAME
          EQUIVALENT  NAME            EQUIVALENT  NAME          ANNOTATED                 ANNOTATED
*(SBA)      X2  =  TMD1.J        X3  =  TMNA8.J      RR2 = XSIG59.J      CC3 = XSIG59.J
X2        X 4   X  7  43  VSDF1C00
RR2         43       8   39
CC3         8        0   195FF

*(SBA)      X3  =  TMNA8.J       X4  =  XCMP93.AX    RR3 = TMLDIN.J      *CC4 = TMLDIN.J
X3          8    1   44  1   VSNA2B00
RR3         44       10  39
CC4         10       0   7FF
X4          10       45  1   VSGB1N00

*(ASSIGN) X6 = TMNO1.J
X6          8    0   12  1   VSINO2B00
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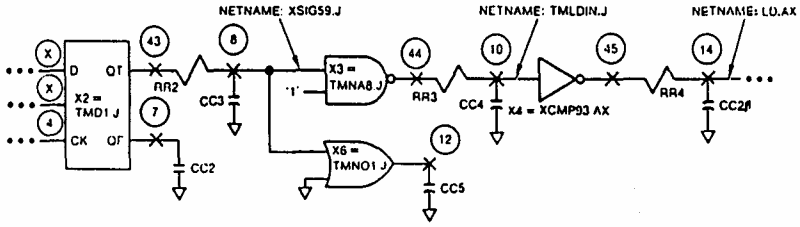

Fig. 5 An SBA formatted SPICE file and its schematic circuit diagram

ted SPICE file and its corresponding schematic circuit. These files also contain cross reference tables to associate the SPICE nodal numbers with their TDL netlist. Each file contains an ordered printout of the critical path instance names and cell types along with all of the branches of the paths to assist the designer during circuit analysis. Crystal-H also performs instance name assignments to assure correct syntax of the generated SPICE files.

SBA accepts automatically generated SPICE files, identifies a path's source-target-net instance names, invokes the parasitic extractor, accesses the two look-up tables, selects the optimal distributed impedance network, and performs back annotation into the predefined SPICE files. Fig. 6 shows a schematic of a typical circuit with $\pi 2$, $\pi 1$, L, R, N, and C lumped interconnect networks chosen in a locally optimal fashion. In Fig. 6(a), dummy RC variables are placed on each cell-to-cell node and are consequently redefined by SBA as shown in Fig. 6(b). The nodes marked 'x' are defined by the circuit designer based on the path's specific functionality. Table 3 depicts SBA benchmarks run on a VAX 11/750.

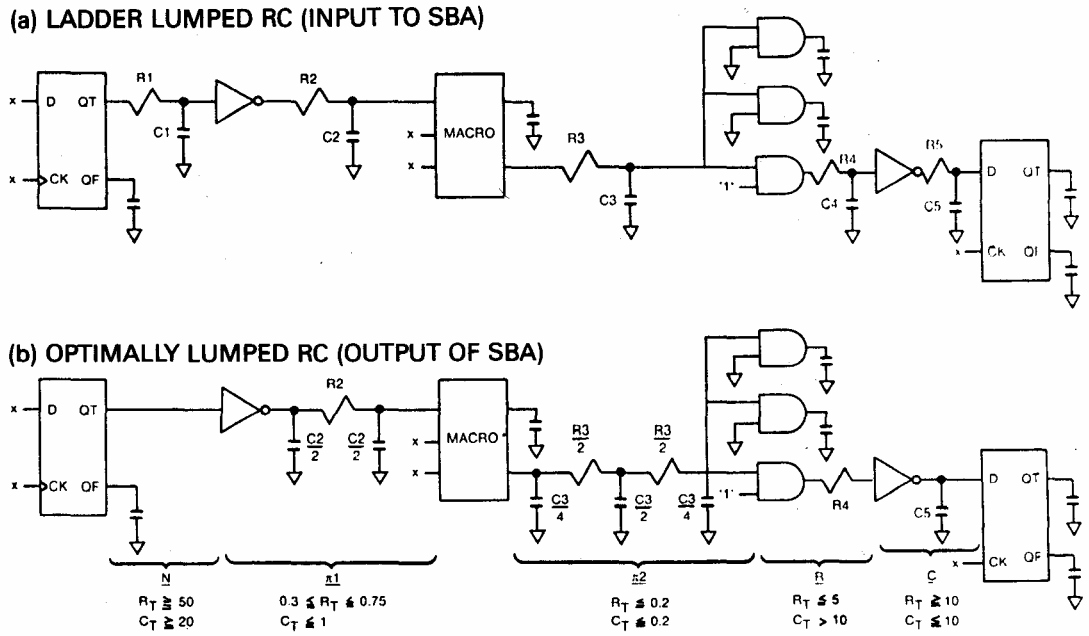

Fig. 6 Typical circuit input to SBA: (a) Input to SBA, (b) Output of SBA

5. Conclusions

A tool for accurately and automatically analysing critical worst case paths in large VLSI circuits has been described. Accurate post-layout resistive and capacitive interconnect impedances are automatically extracted, modeled in a technology dependent optimal fashion, and back annotated into a SPICE formatted circuit simulation file for the precise determination of the timing behaviour of each critical path. An algorithm for 1) determining a device's output impedance from a technology circuit environment and 2) choosing an optimal RC network which accurately models a wire's interconnect impedance based on technology specific look-up tables has been described. These algorithms have been integrated with existing in-house and commercial CAD tools and merges the accuracy required to design high performance VLSI circuits with the automation necessary in today's competitive digital marketplace.

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