optimizing clock trees, especially for high-speed circuits. Our approach provides a useful guideline to a designer; by user-specified parameters, three of these tradeoffs will be provided in this paper. (1) First, to provide a "good" tradeoff between skew and wire length, a new clock tree routing scheme is proposed. The technique is based on a combination of hierarchical bottom-up geometric matching and minimum rectilinear Steiner tree. Our experiments complement the theoretical results. (2) For high-speed clock distribution in the transmission line mode (e.g. multichip modules) where interconnection delay dominates the clock delay, buffer congestion might exist in a layout. Using many buffers in a small wiring area results in substantial interline crosstalks as well as wirability, when the elongation of the imbalanced subtrees is necessary. Placing buffers evenly (locally or globally) over the plane at the minimum impact on wire length increase helps avoiding buffer congestion and results in less crosstalk between clock wires. Thus, an effective technique for buffer distribution will be proposed. Experimental results verifies the effectiveness of the proposed algorithms. (3) Finally, a postprocessing step constraining on phase-delay is also proposed. The technique is based on a combination of hierarchical bottom-up geometric matching and bounded radius minimum spanning tree. The proposed algorithm has an important application in MCM clock net synthesis as well as VLSI clock net synthesis.

Interconnect design with VLSI CMOS. R. F. SECHLER. *IBM Journal of Research and Development.* **39**(1/2), 23 (January/March 1995). Historically, high-performance logic circuit interchip design has focused on bipolar emitter-coupled logic (ECL) circuits and signals, but VLSI CMOS has attained performance levels at which problems unique to its characteristics must be addressed for design optimization. In this paper, CMOS interchip circuit models are applied to develop packaging and wiring constraints for synchronous communication.

Design and realization of high-performance wave-pipelined 8 × 8 b multiplier in CMOS technology. DEBABRATA GHOSH and S. K. NANDY. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **3**(1), 36 (March 1995). Wave pipelining is a design technique for increasing the throughput of a digital circuit or system without introducing pipelining registers between adjacent combinational logic blocks in the circuit/system. However, this requires balancing of the delays along all the paths from the input to the output which comes the way of its implementation. Static CMOS is inherently susceptible to delay variation with input data, and hence, receives a low priority for wave pipelined digital design. On the other hand, ECL and CML, which are amenable to wave pipelining [1], lack the compactness and low power attributes of CMOS. In this paper we attempt to exploit wave pipelining in CMOS technology. We use a single generic building block in Normal Process Complementary Pass Transistor Logic (NPCPL) [2], modeled after CPL [3], to achieve equal delay along all the propagation paths in the logic structure. An 8 × 8 b multiplier is designed using this logic in a 0.8 μm technology. The carrysave multiplier architecture is modified suitably to support wave pipelining, viz., the logic depth of all the paths are made identical. The 1 mm × 0.6 mm multiplier core supports a throughput of 400 MHz and dissipates a total power of 0.6 W. We develop simple enhancements to the NPCPL building blocks that allow the multiplier to sustain throughputs in excess of 600 MHz. The methodology can be extended to introduce wave pipelining in other circuits as well.

C-4/CBGA comparison with other MLC single chip package alternatives. KARL J. PUTTLITZ and WILLIAM F. SHUTLER. *IEEE Transactions on Components, Packaging and Manufacturing Technology, Part B*, **18**(2), 250 (May 1995). Future applications will require higher I/O counts, more densification, lower cost, and greater performance. This paper demonstrates why area-array based chip-to-substrate and substrate-to-card interconnections are strategic, particularly solder bump flip chips (SBFC or C-4) and ceramic ball or column grid arrays (CBGA/CCGA), respectively. That is, SBFC are capable of high pin counts coupled with high yields, performance, and reliability. Moreover, recently introduced CBGA/CCGA interconnections provide substantial benefits over standard pin grid array (PGA) packages. Also, CBGA/CCGA packages possess the highest density achievable at the card level when utilized in conjunction with SBFC-mounted die.

A unified design methodology for CMOS tapered buffers. BRIAN S. CHERKAUER and EBY G. FRIEDMAN. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **3**(1), 99 (March 1995). In this paper, the various disparate approaches to CMOS tapered buffer design are unified into an integrated design methodology. Circuit speed, power dissipation, physical area, and system reliability are the four performance criteria of concern in tapered buffers, and each places a separate, often conflicting, constraint on the design of a tapered buffer. Enhanced short-channel tapered buffer design equations are presented for propagation delay and power dissipation, as well as a new split-capacitor model of hot-carrier reliability of tapered buffers and a two-component physical area model. Each performance criterion is individually investigated and analyzed with respect to the number of stages and tapering factor, and the interaction of the four criteria is examined to develop both a qualitative and a quantitative understanding of the various design tradeoffs. The creation of process dependent look-up tables for optimal buffer design is described, and a methodology to apply these look-up tables to application-specific tapered buffers for both unconstrained and constrained systems is developed. Summarizing, the methodology described in this

paper simultaneously considers the interrelated issues of circuit speed, power dissipation, physical area, and system reliability, permitting the efficient design of tapered buffers.

MCM substrate with high capacitance. ROKURO KAMBE *et al. IEEE Transactions on Components, Packaging and Manufacturing Technology, Part B*, **18**(1), 23 (February 1995). It is well established that thin film capacitors have good electrical characteristics; for that reason they are often used in high frequency applications. We have investigated planarization of bottom capacitive electrodes which must make direct contact with a co-fired ceramic surface, and adjustment and control of the Thermal Coefficient of Expansion (TCE) difference between high dielectric constant material and the base MCM ceramic substrate. Combining thin film capacitors with MCM substrates can result in high frequency decoupling capacitors (with 100× the capacitance of comparable co-fired thin layer alumina constructions), space savings, and significant improvement in performance over conventional discrete chip capacitors.

Corrosion in plastic packages—sensitive initial delamination recognition. OTMAR SELIG, PETER ALPERN and ARAINER TILGNER. *IEEE Transactions on Components, Packaging and Manufacturing Technology, Part B*, **18**(2), 353 (May 1995). The interface between the molding compound (MC) and the chip surface is of considerable interest for failure analysis on plastic-packaged chips. Scanning acoustic microscopy (SAM) is widely used for nondestructive evaluation in this field. Prior research of stressed components has shown that some delaminations containing microbridges, or "spongy" elements, are undetectable by SAM. Corrosion proves to be a sensitive mechanism for detecting these failures. In certain cases corrosion can be detected quasinondestructively by IR microscopy, while conventional destructive physical analysis and optical microscopy remain the easiest way to assess it. Degradation of the interface molding compound and chip is detectable by SAM at a later stage.

MCM-LD: large area processing using photosensitive - BCB. ANDREW J. G. STRANDJORD *et al. IEEE Transactions on Components, Packaging and Manufacturing Technology, Part B*, **18**(2), 269 (May 1995). This paper demonstrates how laminate based printed-wiring-board technology (PWB) and thin film deposited dielectric technology (MCM-D) can be combined to form a low-cost solution for microelectronic interconnect schemes which require high density circuitry. A multilayer telecommunications module was fabricated to demonstrate the feasibility of this MCM-LD concept. Standard copper-clad laminates were processed using conventional PWB techniques to form the first level of metal interconnects (75 μm lines and spaces). A photosensitive benzocyclobutene layer was coated onto the boards and patterned to form 50 μm × 200 μm nested vias down to the metal lines. A second metal interconnect layer was formed from a sputtered seed layer and plated up copper. Chip interconnection was carried out using gold wirebonding. Several large-area-processing (LAP) techniques were evaluated to determine the compatibility of the two interconnect technologies and to demonstrate the cost advantages of manufacturing large panels at high throughput levels. Spin coating, spray coating, meniscus coating, and extrusion coating were compared as dielectric deposition options and an in-line belt furnace was used to cure the dielectric layers on the laminate boards (rapid thermal curing). Laminate materials which were evaluated include: FR-4 (epoxy), BT (bismaleimide-triazine), PI (polyimide) and CE (cyanate ester).

7. SEMICONDUCTOR INTEGRATED CIRCUITS, DEVICES AND MATERIALS

In-situ low temperature cleaning of silicon surfaces using hydrogen atoms. A. CROSSLEY *et al. Vacuum*, **46**(7), 667 (1995). In this work we discuss in-situ cleaning of Si (100) and Si (111) using a hydrogen atom source, with particular reference to carbon and oxygen removal and the quality of the substrate surface after treatment. It is shown that hydrogen atoms are effective at surface carbon removal at temperatures around 350°C and may contribute to lowering the thermal desorption temperature of thin oxides. Exposure of the substrate to hydrogen atoms at high temperature (~750°C), though successful at removing oxide, caused significant damage to the silicon surface.

Preparation and characterization of germanium substrates for MIS electronic devices. Z. BENAMARA and B. GRUZZA. *Vacuum*, **46**(5/6), 477 (1995). For electronic and optoelectronic devices on germanium substrates, it is necessary to analyse, to understand and to control the surface properties of the samples. In this work, surface samples have been investigated by Auger electron spectroscopy under high vacuum conditions. The germanium oxide which is hygroscopic and unstable has been removed. The decrease in the oxide contents is correlated with the evolution of the intensity of the oxygen Auger peak. The adsorption of nitrogen atoms on the surface does not give a stable insulating film when the sample is heated. That is not the case for alumina film condensed on a substrate previously cleaned by cycles of proton sputtering (t = 20 mn, E_0 = 500 eV, $J_0 = 3\ \mu A\ cm^{-2}$). The electrical measurements of the MIS structure ($Ge/Al_2O_3/Hg$) indicate a high density of states which induces the Fermi level pinning observed for different polarizations. These results can be connected with the damage to the surface by the energetic proton beam. On the other hand, better results have been obtained on the same type of structures but realized on substrates prepared by thermal effect. The measured