TOPIC: Optical Microsystems and Devices

ON-CHIP OPTICAL INTERCONNECTS: CHALLENGES AND CRITICAL DIRECTIONS

Guoqing Chen[1], Hui Chen[1], Mikhail Haurylau[1], Nicholas A. Nelson[1], David H. Albonesi[2], Philippe M. Fauchet[1], and Eby G. Friedman[1]

[1]*University of Rochester, Rochester, New York USAy*
[2]*Cornell University, Ithaca, New York USA*

Interconnect has become a primary bottleneck in the integrated circuit design process. As CMOS technology is scaled, the design requirements of delay, power, bandwidth, and noise due to the on-chip interconnects have become increasingly stringent. New design challenges are continuously emerging, such as delay uncertainty induced by process and environmental variations. It has become increasingly difficult for conventional copper interconnect to satisfy these design requirements. On-chip optical interconnect has been considered as a potential substitute for electrical interconnect.

Predictions of the performance of CMOS compatible optical devices are described in this paper. Device models of both electrical and optical interconnect are presented. Based on these models, electrical and optical interconnects are compared for various design criteria at different technology nodes. The opto-electrical modulator is determined as the key component in an optical interconnect-based system. Wavelength division multiplexing (WDM) technology is required in optical interconnect to improve the bandwidth density. The critical dimensions beyond which optical interconnect becomes advantageous over electrical interconnect are shown to be approximately one tenth of the chip edge length at the 22 nm technology node.