Buffer Sizing for Crosstalk Induced Delay Uncertainty

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Abstract. On-chip feature size scaling has aggravated the importance of crosstalk among interconnect lines. The effect of crosstalk on the delay of signals propagating along interconnect lines is investigated in this paper. It is shown that delay uncertainty is proportional to the amount of coupling among interconnect lines. A methodology to reduce delay uncertainty by increasing the size of interconnect buffers is presented. In addition, the effect of increasing buffer size on the power dissipation is discussed. A power efficiency metric is introduced that characterizes the trade off between the reduction in delay uncertainty and the increase in power dissipation.

1 Introduction

The rapid scaling of on-chip geometric dimensions supports the system-on-chip integration of multiple subsystems, greatly increasing the functionality of an integrated circuit. The continuous quest for higher circuit performance has pushed clock frequencies deep into the gigahertz frequencies range, reducing the period of the clock signal well below a nanosecond. These strict timing constraints require tight control on the delay of signals within a high speed synchronous integrated circuit. The deviation of a signal delay from a target value can cause incorrect data to be latched within a register, resulting in a system malfunctioning. These variations in signal delay are described as *delay uncertainty*. The sensitivity of a circuit to delay uncertainty has become an issue of fundamental importance to the design of high performance synchronous systems.

Significant research effort has therefore been focused on characterizing and reducing delay uncertainty [1, 2]. A primary research target is the statistical characterization [3, 4] of process parameter variations and delay uncertainty in order to specify the minimum timing constraints for synchronizing high speed circuits [5,6]. In addition, design methodologies for clock distribution networks [7] have been developed to reduce uncertainty in the clock signal delay [8–10].

Another important effect that introduces delay uncertainty is crosstalk among interconnect lines [11–13]. Scaled on-chip feature size reduces the distance between adjacent interconnect lines. In addition, the thickness-to-width wire aspect

ratio has increased with each technology generation [14]. These effects result in a significant increase in coupling capacitance and crosstalk among interconnect lines [15–18]. The effect of interconnect crosstalk however, has been primarily described as variations in the voltage and current rather than uncertainty in the signal propagation delay.

The effects of interconnect crosstalk on the signal delay are investigated in this paper. It is shown that uncertainty in the signal delay is introduced due to variations in the effective capacitive load of an interconnect line. The effect of these variations on signal delay can be alleviated by increasing the size of a buffer driving a critical delay line, as described in Section 2. Increasing coupling among interconnect lines increases the delay uncertainty, as discussed in Section 3. It is demonstrated in this paper, that the delay uncertainty due to increased coupling can be reduced by increasing the size of the interconnect buffer. In Section 4, the effect of increased buffer size on power dissipation is discussed. A power efficiency metric is introduced to describe the trade off between delay uncertainty and power dissipation. Finally, some conclusions are presented in Section 5.

2 Effects of buffer size on delay uncertainty

Capacitive coupling among interconnect lines introduces uncertainty in the effective capacitive load of the buffers driving these lines. The variation in effective load creates uncertainty in the delay of a signal that propagates along a buffer and an interconnect line. An example of a pair of capacitively coupled interconnects is shown in Fig. 1. The propagation delay from point A to point C along the *victim line* shown in Fig. 1 is affected by the switching of the capacitively coupled *aggressor line*. The signal propagation delay on the victim line can be divided into two parts: the buffer delay from point A to point B, as shown in Fig. 1, and the interconnect delay between points B and C.

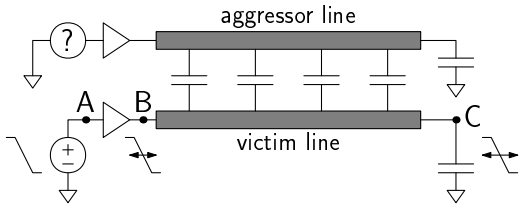


Fig. 1. Model for capacitive coupling between two interconnect lines

The uncertainty of the switching activity of the aggressor line shown in Fig. 1 introduces delay uncertainty in the overall signal propagation along the victim line. Possible signal transitions of the aggressor line during a signal switching on the victim line are:

i) switch in phase (*i.e.*, the same direction) with the victim line.
ii) switch out of phase (*i.e.*, the opposite direction) with the victim line.
iii) no switching (*i.e.*, remain at a steady state, either high or low).

Any uncertainty in the signal transition of the aggressor line introduces uncertainty in the effective capacitive load of the buffer driving the victim line. A relationship describing the delay of an inverter driving an effective capacitive load C_L is presented in [19],

$$t_D = \left(\frac{1}{2} - \frac{1 - v_T}{1 + \alpha}\right) t_T + \frac{C_L V_{DD}}{2 I_{D0}}, \tag{1}$$

where

$$v_T = \frac{V_{TH}}{V_{DD}}, \tag{2}$$

and t_D is the signal propagation delay, α is the velocity saturation index [19], t_T is the transition time of the signal at the input of the inverter, and V_{DD} is the supply voltage. V_{TH} is the threshold voltage of the active transistor during a signal transition and I_{D0} is the drain current flowing through that transistor (defined at $V_{GS} = V_{DS} = V_{DD}$). I_{D0} is often used as an index of the *drive strength* of a MOSFET transistor and depends upon the transistor width W.

The delay uncertainty of a signal propagating along a buffer due to variations in the effective capacitive load can be determined by differentiating (1) with respect to C_L,

$$\partial t_D = \frac{V_{DD}}{2 I_{D0}} \partial C_L. \tag{3}$$

As shown in (3), the variation in delay ∂t_D is proportional to the variation in the effective load of the buffer ∂C_L. In addition, it is shown in (3) that increasing the size of a buffer (*i.e.*, increasing I_{D0}) reduces the effect of variations in the capacitive load on the signal propagation delay.

In order to evaluate the delay uncertainty of a signal on the victim line, a coupled pair of interconnect lines is simulated using Spectre®simulator⋆ for any possible switching activity of the aggressor line. The interconnect structure being evaluated is illustrated in Fig. 2.

- Metal layer : m1
- Feature size $\lambda = 0.09\mu m$
  - minimum line width $W_{min} = 3\lambda = 0.27\mu m$
  - minimum line spacing $S_{min} = 3\lambda = 0.27\mu m$
- Line length $L = 400\mu m$
- Line resistivity $R_L = 296\mu\Omega/\mu m$
- Line capacitance:

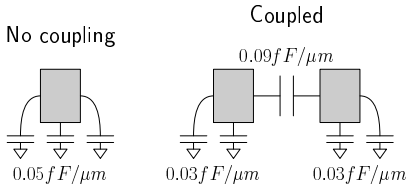
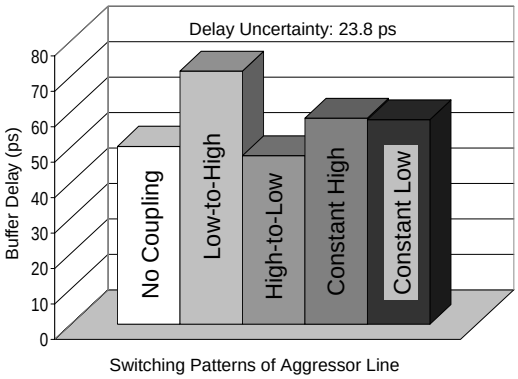


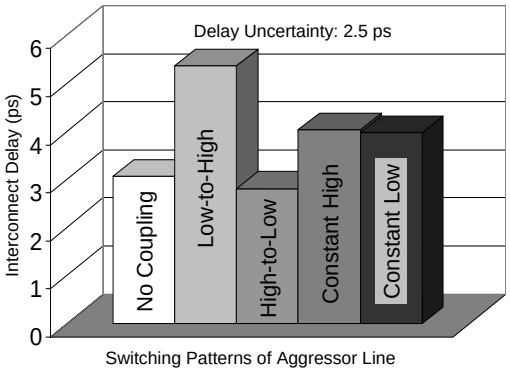
Fig. 2. Simulation setup of capacitively coupled interconnect lines

⋆ Spectre® is a registered trademark of Cadence Design Systems.

The uncertainty in the signal propagation delay along the buffer and the interconnect wire of a victim line is shown in Fig. 3 for different switching patterns of the aggressor line. In the example shown in Fig. 3, the signal at the input of the driver of the victim line switches from high-to-low. The size of the driving buffer for both the victim and the aggressor line is the same. The two lines are coupled along $\frac{1}{4}$ of their total length. The uncertainty of the signal propagation delay along the buffer of the victim line is 23.8 picoseconds as shown in Fig. 3(a). In addition, the uncertainty of the signal delay along the interconnect of the victim line is 2.5 picoseconds, as illustrated in Fig. 3(b). The corresponding delay along the buffer and interconnect wire for an uncoupled line is also shown in Figs. 3(a) and 3(b) for comparison.



(a) Uncertainty in the signal delay along the interconnect buffer

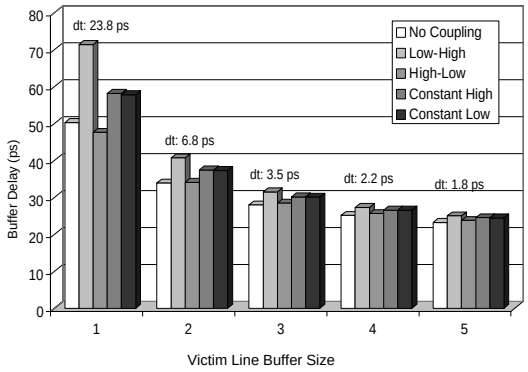


(b) Uncertainty in the signal delay along the interconnect wire

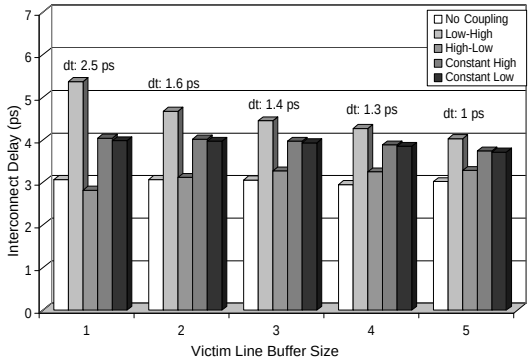
Fig. 3. Uncertainty of the signal delay propagation along the victim line due to different switching activities of the aggressor line

As described in (3), increasing the buffer size reduces the sensitivity of the buffer delay to variations in the load capacitance. This effect is demonstrated in Fig. 4(a), where the size of the aggressor line buffer equals one while the size of the victim line buffer is increased by up to five times. In addition, as shown

in Fig. 4(b), the increased current flowing through the driver buffer reduces the delay uncertainty of a signal propagating along the wire of the victim line (between points B and C as shown in Fig. 1), for the same increase in the size of the victim line buffer.



(a) Reduction in delay uncertainty of the buffer driving the victim line with increasing buffer size



(b) Reduction in delay uncertainty of the interconnect line with increasing buffer size

Fig. 4. Reduction in delay uncertainty along the victim line with increased buffer size

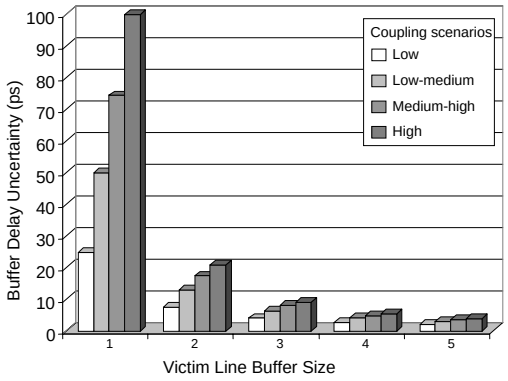
3 Effects of coupling on delay uncertainty

As described in the previous section, the uncertainty in the signal delay along the interconnect lines depends upon the relative size of the buffers driving these lines. It is demonstrated that increasing the size of an interconnect buffer reduces the effects of variations in the effective load. However, the effective capacitive load is increased with increasing coupling between the interconnect lines. Variations of the effective load due to uncertain switching activity of the aggressor line can therefore introduce a greater amount of delay uncertainty on the victim line.

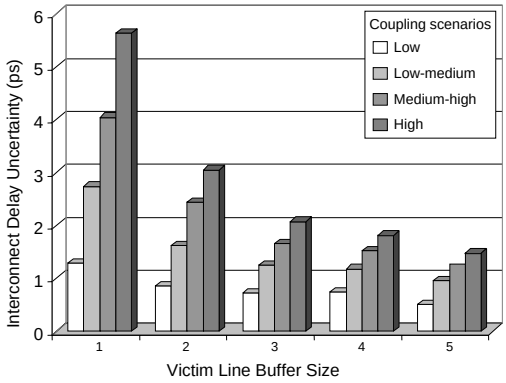
The simulation setup illustrated in Fig. 2 is used to investigate this effect. Four different coupling scenarios are considered, depending upon the amount of coupling between the interconnect lines:

1. Low coupling: the lines are coupled along $\frac{1}{4}$ of the total length.
2. Low-medium coupling: the lines are coupled along $\frac{1}{2}$ of the total length.
3. Medium-high coupling: the lines are coupled along $\frac{3}{4}$ of the total length.
4. High coupling: the lines are coupled along the entire wire length.

Investigating these coupling scenarios demonstrates that the effect of reducing the delay uncertainty by increasing the buffer size becomes more significant as the coupling between the aggressor and victim line increases. As shown in Fig. 5(a), the uncertainty of the signal propagation delay along the buffer driving the victim line increases proportionally with increasing capacitive coupling between the two lines. The delay uncertainty, however, is reduced exponentially



(a) Change in delay uncertainty of the driving buffer with increasing coupling and buffer size



(b) Change in delay uncertainty of the interconnect line with increasing coupling and buffer size

Fig. 5. Delay uncertainty increases proportionally with capacitive coupling between the lines

with increasing buffer size. Similar trends in the delay uncertainty of the signal propagation delay along the interconnect line are illustrated in Fig. 5(b). The delay uncertainty increases proportionally with increased coupling between the lines and is reduced with increasing buffer size.

4 Power dissipation trade offs

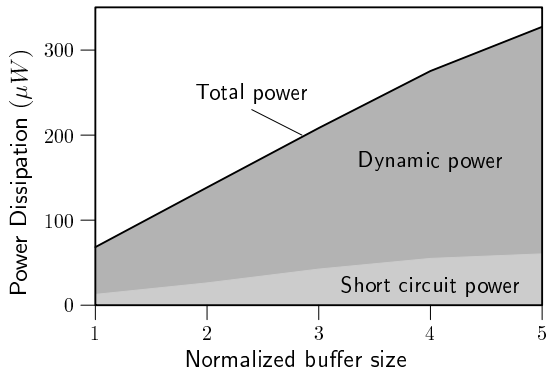
Increasing the size of an interconnect buffer reduces the delay uncertainty introduced due to crosstalk between interconnect lines. Increasing buffer size, however, also increases the buffer area and power dissipation. With increasing die area and the scaling of on-chip feature size, the requirement for increased buffer area is not of primary concern. The increase in power dissipation, however, is a significant effect that imposes practical constraints on the buffer size. In this section, design trade offs between power dissipation and delay uncertainty are discussed.

The effect of the buffer size on power dissipation is listed on Table 1. In the second and third columns of Table 1, the sizes of the NMOS and PMOS transistors are listed for different buffer sizes. The power dissipation for a signal transition cycle between high-to-low and low-to-high is listed in columns four and five. The dynamic power is dissipated while charging and discharging the transistor gates. The short-circuit power is dissipated due to the current that flows directly from V_{dd} to ground during a signal transition, when both the PMOS and NMOS transistors are on. The increase in short-circuit and dynamic power with buffer size is illustrated in Fig. 6(a). The leakage power listed in column six of Table 1 represents the power dissipated due to leakage current flowing through the buffer transistors while the buffer input is at a steady state voltage. The increase in leakage power with larger buffer size is illustrated in Fig. 6(b). The total power dissipation is listed in column seven of Table 1 and is illustrated in Fig. 6(a).

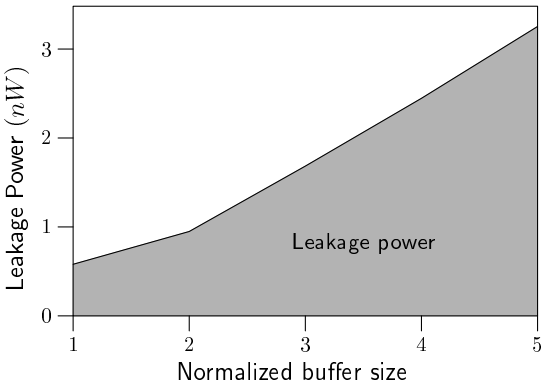
A qualitative trade off between the reduction in delay uncertainty and increased power dissipation with increasing buffer size can be described by the *Power-Delay-uncertainty-Product* (PD_UP). The PD_UP is introduced to compare the rate of *decreasing* delay uncertainty with respect to the rate of *increasing* power dissipation, as the buffer size is increased. Decreasing PD_UP with

Table 1. Transistor size and power dissipation components for different buffer sizes.

Buffer Size	NMOS tran. size	PMOS tran. size	Dynamic power (μW)	Short circuit power (μW)	Leakage power (nW)	Total power (μW)
1	0.9 μm	2.34 μm	55.5	12.7	0.5	68.2
2	1.8 μm	4.68 μm	112.2	26.2	0.9	138.4
3	2.7 μm	7.02 μm	165.5	42.7	1.6	208.2
4	3.6 μm	9.36 μm	220.3	55.0	2.4	275.3
5	4.5 μm	11.7 μm	266.9	60.3	3.2	327.2



(a) Short-circuit, dynamic, and total power dissipation with increasing buffer size



(b) Increase in leakage power with increasing buffer size

Fig. 6. Increase in power dissipation with buffer size

increasing buffer size indicates that the reduction in delay uncertainty is higher than the increase in power dissipation. Alternatively, an increase in PD_UP with increasing buffer size demonstrates a faster increase in power dissipation than the decrease in delay uncertainty. The PD_UP with increasing buffer size is illustrated in Fig. 7 for the delay uncertainty introduced due to capacitive coupling among interconnects. As shown in Fig. 7, increasing the buffer size is a power efficient way to reduce delay uncertainty due to interconnect coupling, since decreasing PD_UP indicates that the power dissipation increases slower than the delay uncertainty is reduced.

5 Conclusions

The uncertainty in the signal delay due to crosstalk among interconnect lines is investigated. In addition, the effect on the delay uncertainty of different switching patterns among capacitively coupled lines is evaluated. It is shown that delay

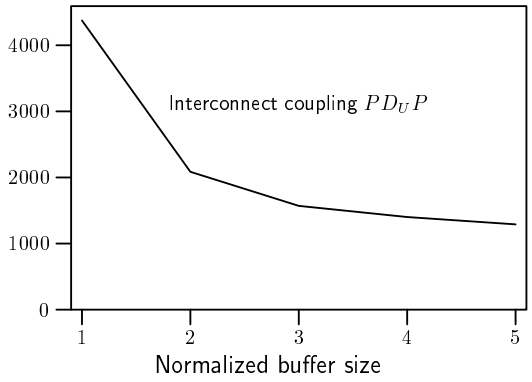


Fig. 7. Power-Delay uncertainty Product (PD_UP) for different sizes of victim line drivers

uncertainty increases with coupling among the lines and decreases with increasing buffer size. The effect of increasing the buffer size on the power dissipation is also examined. A power efficiency metric, the Power-Delay-uncertainty-Product (PD_UP), is introduced to quantify the trade off between delay uncertainty and power dissipation. It is shown that increasing buffer size is a power efficient method to reduce delay uncertainty due to capacitive coupling among interconnects.

References

1. P. Zarkesh-Ha, T. Mule, and J. D. Meindl, "Characterization and Modeling of Clock Skew with Process Variations," *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 441–444, May 1999.
2. S. R. Nassif, "Modeling and Analysis of Manufacturing Variations," *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 223–228, May 2001.
3. M. Orshansky, J. C. Chen, and C. Hu, "Direct Sampling Methodology for Statistical Analysis of Scaled CMOS Technologies," *IEEE Transactions on Semiconductor Manufacturing*, Vol. 12, No. 4, pp. 403–408, November 1999.
4. V. Mehrotra, S. L. Sam, D. Boning, A. Chandrakasan, R. Vallishayee, and S. Nassif, "A Methodology for Modeling the Effects of Systematic Within-Die Interconnect and Device Variation on Circuit Performance," *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 172–175, June 2000.
5. S. Zanella, A. Nardi, A. Neviani, M. Quarantelli, S. Saxena, and C. Guardiani, "Analysis of the Impact of Process Variations on Clock Skew," *IEEE Transactions on Semiconductor Manufacturing*, Vol. 13, No. 4, pp. 401–407, November 2000.
6. S. Sauter, D. Schmitt-Landsiedel, R. Thewes, and W. Weber, "Effect of Parameter Variations at Chip and Wafer Level on Clock Skews," *IEEE Transactions on Semiconductor Manufacturing*, Vol. 13, No. 4, pp. 395–400, November 2000.
7. I. S. Kourtev and E. G. Friedman, *Timing Optimization Through Clock Skew Scheduling*, Kluwer Academic Publishers, Norwell Massachusetts, 2000.

8. J. L. Neves and E. G. Friedman, "Optimal Clock Skew Scheduling Tolerant to Process Variations," *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 623–628, June 1996.
9. M. Nekili, C. Bois, and Y. Savaria, "Pipelined H-Trees for High-Speed Clocking of Large Integrated Systems in Presence of Process Variations," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 5, No. 2, pp. 161–174, June 1997.
10. D. Velenis, M. C. Papaefthymiou, and E. G. Friedman, "Reduced Delay Uncertainty in High Performance Clock Distribution Networks," *Proceedings of the IEEE Design Automation and Test in Europe Conference*, pp. 68–73, March 2003.
11. K. T. Tang and E. G. Friedman, "Interconnect Coupling Noise in CMOS VLSI Circuits," *Proceedings of the ACM International Symposium on Physical Design*, pp. 48–53, April 1999.
12. A. Vittal, L. H. Chen, M. Marek-Sadowska, K.-P. Wang, and S. Yang, "Crosstalk in VLSI Interconnections," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 18, No. 12, pp. 1817–1824, December 1999.
13. S. S. Sapatnekar, "A Timing Model Incorporating the Effect of Crosstalk on Delay and its Application to Optimal Channel Routing," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 19, No. 5, pp. 550–559, May 2000.
14. X. Huang, Y. Cao, D. Sylvester, S. Lin, T.-J. King, and C. Hu, "RLC Signal Integrity Analysis of High Global Interconnects," *Proceedings of the IEEE International Electron Devices Meeting*, pp. 731–734, December 2000.
15. K. T. Tang and E. G. Friedman, "Delay and Noise Estimation of CMOS Logic Gates Driving Coupled Resistive-Capacitive Interconnections," *Integration, the VLSI Journal*, Vol. 29, No. 2, pp. 131–165, September 2000.
16. J. Cong, D. Z. Pan, and P. V. Srinivas, "Improved Crosstalk Modeling for Noise Constrained Interconnect Optimization," *Proceedings of the ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, pp. 14–20, December 2000.
17. M. Kuhlmann and S. S. Sapatnekar, "Exact and Efficient Crosstalk Estimation," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 20, No. 7, pp. 858–866, July 2001.
18. T. Sakurai, "Closed-Form Expressions for Interconnection Delay, Coupling and Crosstalk in VLSI's," *IEEE Transactions on Electron Devices*, Vol. 40, No. 1, pp. 118–124, January 1993.
19. T. Sakurai and A. R. Newton, "Alpha-Power Law MOSFET Model and its Applications to CMOS Inverter Delay and Other Formulas," *IEEE Journal of Solid State Circuits*, Vol. 25, No. 2, pp. 584–593, April 1990.