# Transmission Lines in VLSI Complexity Single Flux Quantum Systems

**Tahereh Jabbari and Eby G. Friedman**
Department of Electrical and Computer Engineering
University of Rochester, Rochester, New York 14627, USA

**Abstract**— Superconductive electronics based on Josephson junctions (JJ) is a promising cryogenic alternative technology to complementary metal oxide semiconductor (CMOS) technology for ultra-low energy, high speed stationary applications. For complex superconductive systems, the automated routing process determines the topology and methodology to connect cells while satisfying design constraints. On-chip signal routing has become an issue of growing importance in modern superconductive technologies; particularly, single flux quantum (SFQ) systems. Specialized routing methods for these systems are required. These routing methods include passive transmission lines (PTLs) and Josephson transmission lines (JTLs) behaving as interconnects. A primary issue within a long SFQ interconnect is the effects of resonance due to the imperfect match between the PTLs and Josephson junctions. A repeater insertion methodology to reduce and manage these resonance effects is required for driving long and short interconnect in VLSI complexity SFQ systems. Permissible interconnect lengths are suggested to ensure the reflections do not affect the returning signals. The microwave behavior of the interconnect striplines is also considered to accurately estimate the surface inductance of the lines. A closed-form expression describing the dependence of the surface inductance of a stripline on the line thickness, magnetic field, and current density is discussed. Another primary issue within SFQ circuits is coupling noise between transmission striplines, degrading performance and decreasing margins. Inductive and capacitive coupling noise between the routing layers, for the MIT LL SFQ5ee process, is described. An analysis of inductive and capacitive coupling noise can determine the minimum physical spacing between lines to enhance the automated routing process in large scale systems. The increasing complexity of modern SFQ circuits has also made the issue of flux trapping of growing importance. The use of wide striplines for signal routing has exacerbated this issue. Trapped residual magnetic fields within the striplines damage the operability of superconductive circuits. Area efficient topologies for striplines are introduced to manage flux trapping in large scale SFQ circuits. These topologies are composed of several narrow lines rather than a single wide stripline. The first approach is a narrow parallel line topology in series with small resistors where each narrow line is connected to a single small resistor and via. The resistors in the parallel line topology remove any trapped fluxons and break any loops while requiring additional vias. The second topology is a fingered narrow line topology. The fingered narrow line topology enhances the scalability of SFQ systems while not requiring additional area and vias. These proposed topologies require significantly less area while preventing flux from being trapped within wide superconductive striplines and reducing coupling noise between striplines. These methodologies and techniques are intended as guidelines to enable robust routing with superconductive interconnects. With these and other advances in design methodologies for superconductive electronics, the complexity of SFQ circuits is expected to greatly increase.

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## 1. INTRODUCTION

Superconductive single flux quantum (SFQ) technology is one of the most promising beyond-CMOS technologies for ultra-high speed and ultra-low power digital applications [1]. Significant advances in fabrication technology and electronic design automation (EDA) of superconductive electronics for prospective exascale computing systems have led to device densities exceeding $4.2 \times 10^6$ Josephson junctions (JJs) per $cm^2$ with a minimum feature size of 350 nm [2]. An important characteristic of SFQ circuits is absolute zero DC resistance interconnects. SFQ circuits utilize two distinct types of interconnect-active Josephson transmission lines (JTL) and passive transmission lines (PTL), composed of a microstrip or stripline with a matched driver and receiver [3, 4]. A comparison of the energy dissipated by interconnects for CMOS and SFQ is shown in Figure 1. The energy of a 16 nm CMOS interconnect technology is evaluated with an RLC model. The energy of the passive superconductive interconnect is approximately six orders of magnitude less than the energy dissipated by CMOS interconnects [4, 5].

SFQ pulses propagate along a PTL at approximately one-third the speed of light without dissipation [6]. This feature motivates SFQ logic as a strong candidate for VLSI complexity ultra-high

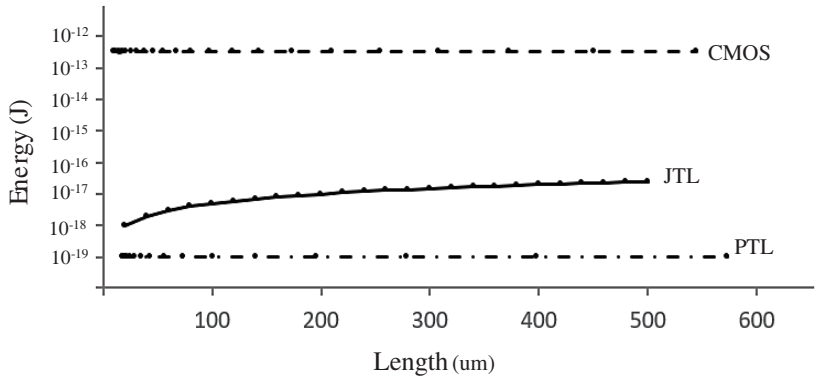


Figure 1. Energy vs. length of CMOS (dash line), JTL (solid line), and PTL with one Josephson junction in the receiver (dash-dotted line) [5].

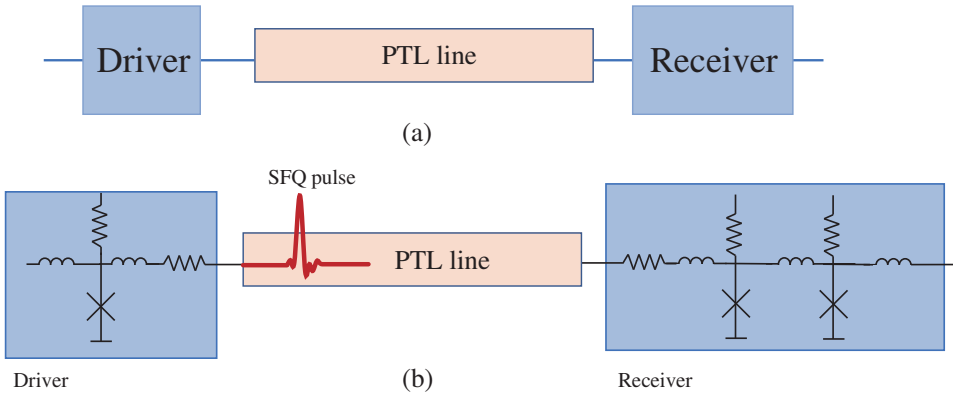


Figure 2. PTL interconnect topology, (a) PTL line between driver and receiver, and (b) PTL line with two JJs in the receiver and one JJ in the driver.

speed, ultra-low power digital applications. Utilizing PTLs rather than JTLs for long lines in SFQ circuits lowers the area, delay, and power dissipation. A primary concern of automated routing methodologies in integrated SFQ circuits is pulse reflections in long transmission lines due to an imperfect impedance match between the SFQ load and the PTL line. A typical PTL topology with an input SFQ pulse is shown in Figure 2. Due to the coincidence of the input SFQ pulse with the reflection of the previous pulse, resonant effects can occur in long passive transmission lines [5]. The resonance in PTLs is dependent on the length of the PTL segment and the frequency of the SFQ signal. Specialized algorithms and guidelines for SFQ-based automated routing tools are needed to assign the interconnect length for each line and driver/receiver configuration when propagating a signal along a long passive interconnect [3, 7–11].

Another primary requirement for SFQ-based automated routing is an accurate impedance model of the striplines. Electromagnetic simulators such as Sonnet provide an accurate estimate of the impedance which depends upon certain material parameters such as the surface inductance $L_s$ of the superconductive material [12]. The surface inductance plays a significant role in characterizing the impedance of a stripline within large scale integrated SFQ systems. The surface inductance is dependent upon the structure of the striplines, distance to the ground layers, thickness of the stripline, magnetic field around the lines, and current distribution inside the line. Specialized guidelines and expressions are needed to provide an accurate estimate of the surface inductance, inductive characteristics along the surface of a stripline, and inductive and capacitive coupling noise.

Another significant issue in large scale superconductive integrated circuits is the sensitivity of SFQ interconnects to magnetic fields [12–16]. Residual magnetic fields in VLSI complexity SFQ circuits increase the probability of trapped fluxons within the superconductive loops and striplines. The fluxons trapped within the wide striplines near the logic cells degrade circuit operation while lowering the critical current and decreasing the bias margins of the Josephson junctions. The trapped magnetic field also couples trapped fluxons into nearby inductances, interconnects, and

bias lines. Flux mitigation is therefore necessary within large scale SFQ circuits and, in particular, the striplines, to support the development of advanced superconductive systems.

In this paper, the principles of SFQ interconnects are briefly reviewed in Section 2. The properties of JTL interconnect are discussed in Section 3. The properties of PTL interconnect are discussed in Section 4. The characteristics of a PTL interconnect when inserting a repeater (driver/receiver pair) are reviewed in Section 5. Avoiding resonance effects in long lines driven by these repeaters is also described in Section 5. Inductive and capacitive coupling noise between lines are summarized in Section 6. Topologies for wide superconductive striplines to eliminate flux trapping are presented in Section 7. Clock routing for SFQ systems is discussed in Section 8. The paper is concluded in Section 9.

## 2. PRINCIPLES OF SFQ INTERCONNECT NETWORKS

An SFQ routing system is typically composed of splitters and interconnects. In this section, the components to enable SFQ routing, splitters and interconnect, are described, respectively, in Subsections 2.1 and 2.2.

### 2.1. Splitters

The distribution of data and clock pulses to multiple fanout is a primary concern in VLSI complexity SFQ systems. Most SFQ gates and flip flops exhibit a fanout of one. A splitter gate is required to convert a quantum pulse into multiple quanta without a significant decrease in amplitude. A splitter is typically placed at the output of an SFQ gate when driving multiple fanout. A standard active splitter is shown in Figures 3(a) and 3(b) [17]. This active splitter can produce two SFQ pulses. A splitter tree with a fanout of four is depicted in Figure 3(c). An important issue in this active splitter is the limited fanout while requiring a large bias current. To support multiple fanout, additional splitters are included within a binary tree structure, significantly increasing the total bias current, physical area, and dissipated power.

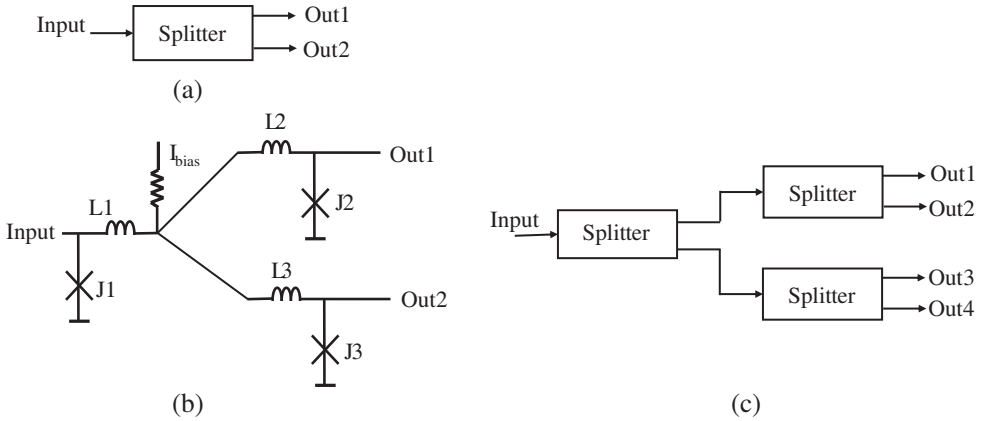


Figure 3. Standard SFQ splitters, (a) block diagram with fanout of two, (b) circuit with fanout of two, and c) block diagram of splitter tree with fanout of four.

Novel splitter topologies have been developed to support multiple outputs while requiring less area and power and exhibiting lower delay. These area and power efficient splitters are 1) active splitter trees requiring fewer JJs, 2) passive splitters, and 3) multi-output active splitters [17]. The multi-output splitters dissipate less power and require smaller area than the active splitter trees since fewer JJs and lower bias currents are required.

### 2.2. Interconnects

In SFQ circuits, two types of interconnects can transmit an SFQ pulse between gates, Josephson transmission lines and passive transmission lines. In SFQ circuits, a JTL interconnect transmits pulses without reflections. PTL lines transfer pulses with extremely low loss at approximately one-third the speed of light in a vacuum. Generally, for short interconnects, JTLs are preferable; for long interconnects, PTLs are preferable.

## 3. JOSEPHSON TRANSMISSION LINES

The propagation of SFQ pulses plays an important role in the efficiency of complex SFQ circuits. Josephson transmission lines are typically composed of basic cells to locally transfer an SFQ pulse between gates. JTLs also amplify an SFQ pulse between gates. A Josephson transmission line can therefore be used as an interface between these gates. JTLs, however, have certain disadvantages and restrictions.

A JTL is typically composed of uniformly sized Josephson junctions with a uniform inductance $L$ between junctions. A chain of JTLs behaves as an SFQ interconnect, as shown in Figure 4. The number of JTLs depends upon the distance between the SFQ cells. The length of one JTL stage is approximately 20 µm [3] (in a 10 kA/cm$^2$ technology). For example, for a distance of 200 µm between SFQ cells, ten JTLs are required.

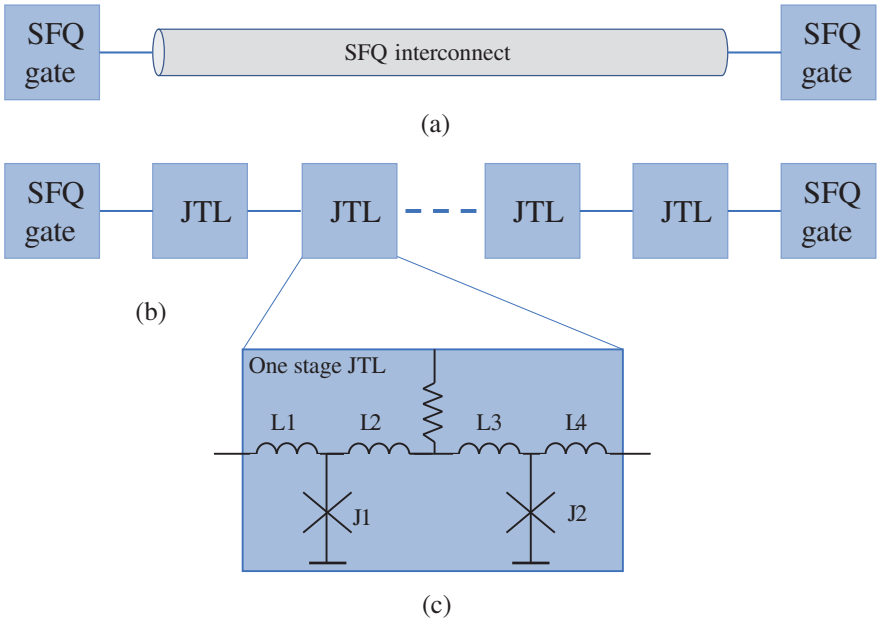


Figure 4. JTL interconnect topology, (a) interconnect between two SFQ gates, (b) chain of JTLs as interconnect between gates, and (c) single stage JTL.

The number and size of the JJs in the interconnect topologies affect the delay and physical characteristics. The delay of one JTL stage is about 5 ps. The delay of a chain of JTLs increases linearly with the number of JTLs. For a short line, a JTL requires less area with comparable delay as compared to a PTL. The JTL interconnect is located within the active gate layers. JTL-based SFQ interconnect consumes significant area, power, and delay when connecting distant SFQ circuits. Although not a significant issue in current MSI SFQ circuits, the greater area, power, and delay of a JTL are a significant challenge for prospective VLSI complexity SFQ circuits. Furthermore, certain constraints on the inductance within a JTL cell exist, which reduces the design flexibility of the physical layout [3, 4].

## 4. PASSIVE TRANSMISSION LINES

In large scale SFQ circuits, PTLs are used to connect distant SFQ gates. The PTL interconnects lower the propagation delay in long interconnections while providing compatibility with automated routing and clock tree synthesis (CTS) layout algorithms. PTL interconnect use fewer JJs and dissipate less power than JTLs in long interconnects.

The length and area of a PTL interconnect affect both the JJ layers and the routing layers. A typical PTL consists of a superconductive microstrip or stripline in the routing layers, one JJ, a small inductance in the driver circuit, and two JJs with an inductance in the receiver within the active gate layers (see Figure 2(b)) [18]. With three bias currents and JJs in a typical PTL topology, significant area and energy requirements are introduced into the bias network.

Fewer JJs within a PTL reduce the area, delay, and bias current of a PTL interconnect. A reliable topology for a PTL in a 10 kA/cm$^2$ technology is introduced in [3] to lower the overhead.

A PTL topology with one JJ in the receiver is shown in Figure 5. The PTL driver includes the last JJ within the previous SFQ gate which produces the flux quantum pulse. The PTL receiver is composed of one JJ and a large inductance. The length of the line within the routing layer is dependent upon the distance between the two gates. For long interconnect, the delay and area of a PTL are significantly lower than the delay of a chain of JTLs. However, congestion in the routing layers, assuming space within the cell layers is available, can make a JTL the preferable choice for interconnect despite the greater area, power, and bias requirements.

A primary issue in superconductive PTLs is the impedance match between the PTL and the Josephson junctions. Due to the partial reflection and imperfect match between the PTL and the driver and receiver, resonant effects can occur in long PTL lines [5, 19, 20, 21]. This resonant effect depends upon the length of the PTL and the frequency of the SFQ signal. A methodology to manage and mitigate these effects is discussed in Section 5.

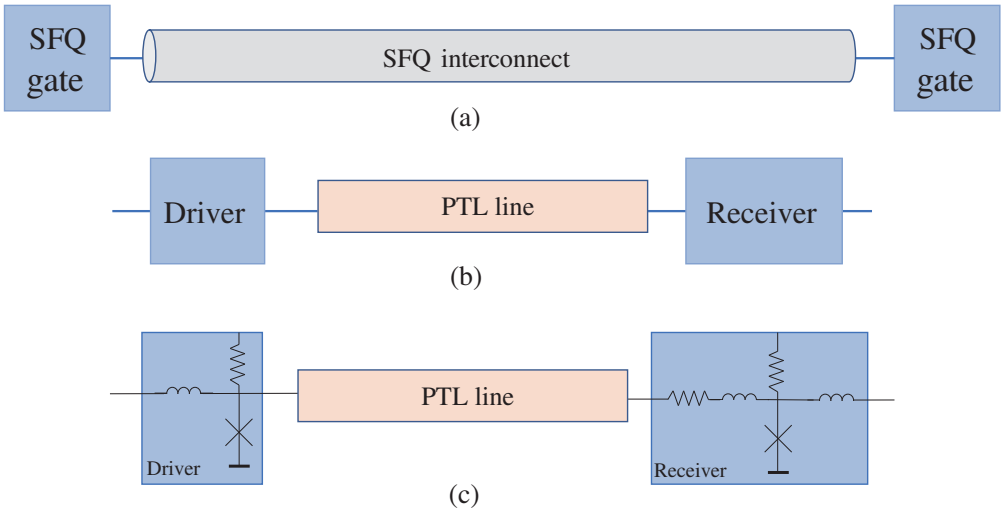


Figure 5. PTL interconnect topology, (a) interconnect between two SFQ gates, (b) PTL configuration as interconnect between gates, and (c) PTL interconnect with the last JJ of the previous SFQ gate as the driver and one JJ in the receiver.

## 5. REPEATER INSERTION IN SFQ INTERCONNECTS

One of the primary concerns of automated routing methodologies in integrated SFQ circuits is resonance effects within passive superconductive transmission lines. This effect occurs in a PTL line when the reflections of the SFQ signal from the receiver or driver coincide with the pulse within a line. These resonance effects decrease the bias margins or can produce incorrect circuit behavior.

An analysis of the bias margins of a receiver within a PTL is depicted in Figure 6 for different interconnect lengths at 20 GHz and 40 GHz. The dependence of the bias margins on the PTL segment length is also depicted in this figure. The set of resonance lengths of a PTL segment depends upon the frequency of the applied SFQ signal which peaks at the lowest margin (see Figure 6). The relationship between the resonant length of an interconnect segment and the frequency of an SFQ pulse is

$$f_{resonance} = \frac{nv_{phase}}{2L_l}, \tag{1}$$

where $v_{phase}$ is the phase velocity [5] of the superconductive passive interconnect, $L_l$ is the physical length of the PTL interconnect, and $n$ is an integer multiplier that describes the harmonics of the resonance frequency.

In Figure 6, a sharp peak in the bias margin at 40 GHz (the dashed line) occurs at 1.35 mm and a second peak occurs at 2.9 mm. At lower frequencies, the resonance lengths occur in longer lines. The second resonance length at 40 GHz occurs at the same length as the first resonance effect at 20 GHz, consistent with (1). This resonance behavior affects the bias margins and can cause a circuit to not function properly.

For any frequency SFQ pulse, a set of forbidden PTL lengths is produced, which corresponds to the main resonant length, consistent with (1). To prevent this resonance effect from degrading

circuit operation, this set of forbidden lengths should be avoided. The length of a PTL segment is typically limited to less than the shortest resonant length.

Similar to conventional CMOS circuits, repeaters are inserted into long passive transmission lines to partition a line into shorter segments [22]. An SFQ PTL line with and without repeaters is shown in Figure 7. The repeaters are located to ensure that the length of each interconnect segment is outside the set of forbidden lengths [5].

The objective of the repeater insertion process in SFQ interconnect is to determine the number of repeaters and the length of each segment within a long PTL. Assuming a bias margin for the receiver at 40 GHz, repeaters are inserted into a long PTL line, determining the number of repeaters and the length of each segment. A bias margin analysis of the PTL interconnect at 40 GHz (for a 10 kA/cm$^2$ technology) is depicted in Figure 8 without repeaters (dashed line) and with repeaters (solid line). These results illustrate the improvement in the bias margins of an interconnect with repeaters. The repeater insertion process in SFQ interconnect also improves the robustness of the receiver due to the wider margins.

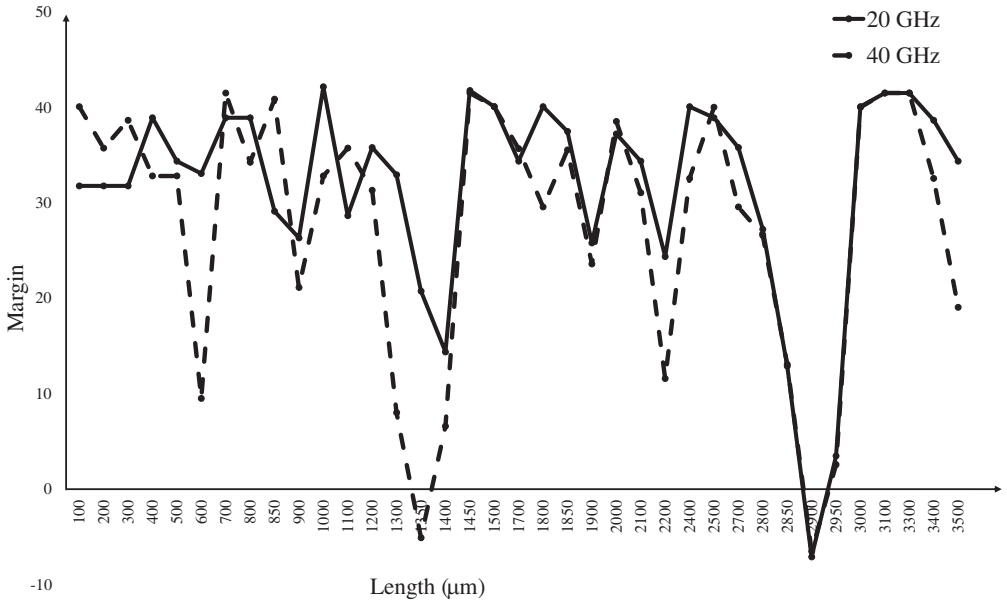


Figure 6. Resonance effects in a lossless superconductive transmission line at 20 and 40 GHz.

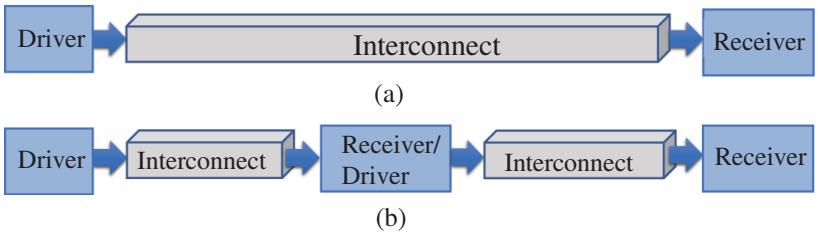


Figure 7. SFQ interconnect, (a) no repeater, and (b) with repeaters.

## 6. COUPLING NOISE

One of the primary issues in SFQ-based automated routing algorithms is the magnitude of the inductive and capacitive coupling noise between lines. Electromagnetic simulators such as Sonnet can be used to provide an accurate estimate of the impedance and noise characteristics. These characteristics depend upon certain material parameters such as the surface inductance $L_s$ of the superconductive material. The surface inductance of a stripline is analytically described in [12]. These expressions for the surface inductance of a stripline provide an accurate estimate of the self- and mutual inductance and capacitance between superconductive lines [12].

Many issues exist in routing SFQ systems to ensure effective manufacturability. At present, routing guidelines are limited to coupling between interconnect lines. The SFQ signals propagating

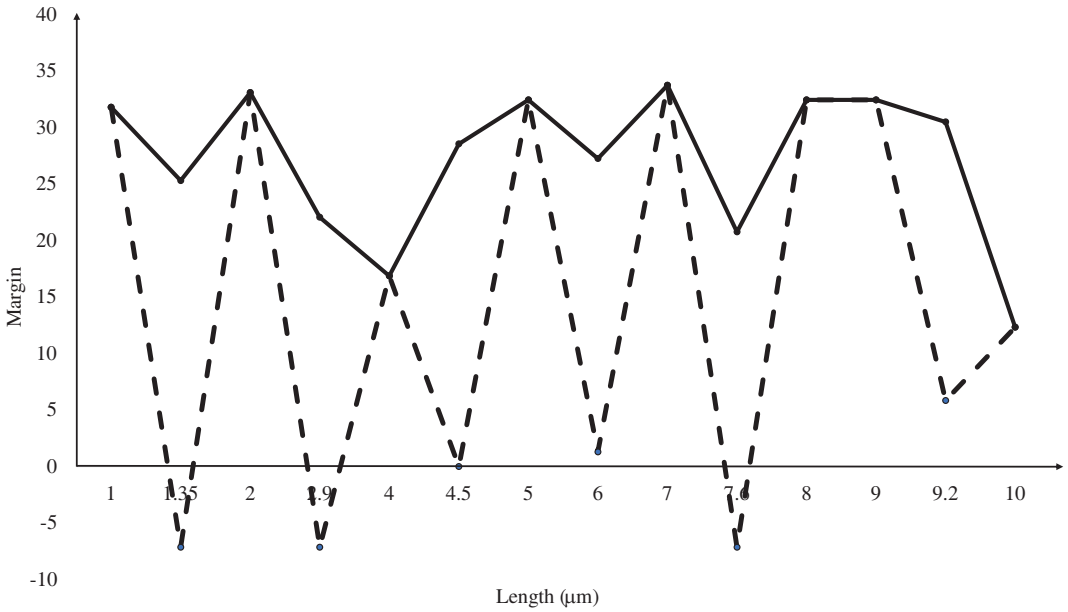


Figure 8. The effects of resonance on the bias margins of a receiver in a lossless PTL at 40 GHz with repeaters (solid line) and without repeaters (dashed line).

along the PTL lines can magnetically couple to other lines, producing significant noise. In the physical layout of SFQ circuits [23, 24], the PTL lines are placed between two ground planes. This feature increases the coupling between PTL lines. Bias lines carrying high current also affect the operation of the PTLs. The mutual inductance of several structures at different distances from the stripline to the ground layers, evaluated in Sonnet, is listed in Table 1. These results match experimental data within 3%, less than the standard deviation of the experimental data [25]. The mutual inductance of these striplines, evaluated by a commercial 3-D inductance extractor (FastHenry) [26], is also listed in Table I. These results match experimental data within 7% [26]. The noise characteristics of striplines based on expressions for the surface inductance therefore provide an accurate estimate of the mutual inductance between striplines [12]. Estimates of the self- and mutual inductance can be used as guidelines for automated routing tools and for the placement of standard cells within VLSI complexity SFQ circuits.

Table 1. Mutual inductance of different stripline structures.

| **Coupled striplines** | **Mutual inductance, pH, experimental [25]** | **% Experimental standard deviation** | **Mutual inductance, pH, Sonnet** | **% Error** | **Mutual inductance, pH, FastHenry [26]** | **% Error** |
|---|---|---|---|---|---|---|
| *M4-M5-M7, M4-M6-M7* | 1.95 | 1.43 | 1.97 | +1.09 | 1.89 | −3.2 |
| *M3-M4-M7, M3-M5-M7* | 2.75 | 2.89 | 2.82 | +2.67 | 2.94 | +6.9 |
| *M2-M3-M7, M2-M4-M7* | 3.04 | 2.04 | 3.09 | +1.60 | 3.13 | +3.0 |
| *M1-M2-M7, M1-M3-M7* | 3.27 | 0.90 | 3.256 | +0.42 | 3.30 | +0.9 |
| *M0-M1-M7, M0-M2-M7* | 3.37 | 1.12 | 3.354 | +0.47 | 3.58 | +6.2 |

## 7. FLUX TRAPPING

Flux trapping within superconductive thin films was discovered in 1982 [13]. A primary type of flux trapping in SFQ systems is trapped fluxons within wide striplines. These fluxons near the

logic cells degrade circuit operation while lowering the critical current and decreasing the bias margins of the Josephson junctions. The trapped fluxons can also couple into nearby inductances, interconnects, and bias lines. Novel stripline topologies are proposed here to mitigate flux trapping in these structures. The topology of the proposed striplines is shown in Figure 9, the narrow parallel line topology and fingered narrow line topology. The narrow parallel line topology is composed of narrow lines and small resistors/vias, where each narrow line is connected to a single resistive layer (see Figure 9(a)). The multiple narrow parallel lines are connected with perpendicular lines at the ends of the narrow lines. Due to the number of vias, a tradeoff exists between the scalability of SFQ circuits and the effectiveness of the parallel line topology. Decreasing the number of vias and resistors will reduce the probability of trapped flux within the narrow parallel lines; however, flux trapping can still occur between parallel lines. To enhance the scalability of SFQ systems, an approach is proposed to eliminate flux trapping within striplines while not increasing the number of vias. The proposed stripline topology is shown in Figure 9(b). Capacitive coupling between lines passes SFQ pulses along the striplines. The preferable width of the narrow lines and the spacing between these lines are technology dependent. A thinner stripline width lowers the likelihood of flux being trapped within the stripline. The proposed topologies break the superconductive loops within the striplines and reduce flux trapping within the striplines and routing layers. The narrow fingered line topology requires less area than the narrow parallel line topology.

The narrow parallel line topology exhibits the same output impedance characteristics as a wide line [14]; no changes are therefore required for the driver and receiver within a passive transmission line segment. In addition, the narrow parallel line topology exhibits the same resonance characteristics as a single wide stripline. Design guidelines for wide striplines are also applicable to the narrow parallel line topology [5].

The coupling capacitance of the fingered line topology is two to three times less than the coupling capacitance of a wide stripline. The inductive coupling coefficient of the fingered line topology is approximately half of the inductive coupling coefficient of the wide stripline [16]. The fingered topology therefore prevents flux from being trapped within striplines, supporting robust routing of superconductive striplines while requiring less area and producing less coupling noise.

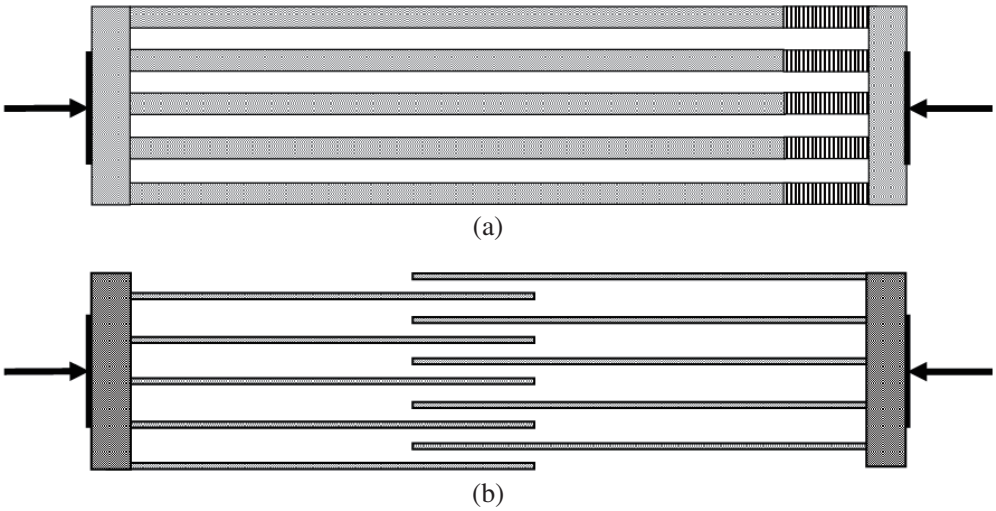


Figure 9. Configuration of stripline, (a) multiple narrow parallel lines, and (b) fingered narrow lines.

## 8. CLOCK TREE SYNTHESIS IN SFQ SYSTEMS

Clock tree synthesis is a process to distribute a clock signal to the many individual clocked SFQ elements. In SFQ circuits, a clock signal is required for most logic gates (except for splitters, JTLs, buffers, and mergers). The clock network typically has the highest priority to avoid competition with the data signals for resources. Clock routing in SFQ systems is often achieved with two sequentially combined methods, global symmetric clock networks [27] followed by local asymmetric clock networks [6].

Global clock synthesis of SFQ circuits is often designed to produce a near zero skew clock network. A commonly used global clock network topology is a symmetric H-tree network with

asymmetric leaves to propagate the clock signal to the individual SFQ gates. A symmetric H-tree network is often used to distribute the high speed clock signals in VLSI complexity SFQ circuits [27, 28]. The structure of an SFQ H-tree clock network is shown in Figure 10. The tree is composed of interconnects, splitters, and leaves. The symmetric structure ensures near zero clock skew between the leaves of the clock tree. Each leaf represents a functional block composed of a large number of SFQ gates. An SFQ H-tree clock network with $N$ leaves requires $N-1$ splitters, consuming significant area and increasing the clock path delay. PTL interconnects are typically used in these long lines in symmetric H-tree clock networks.

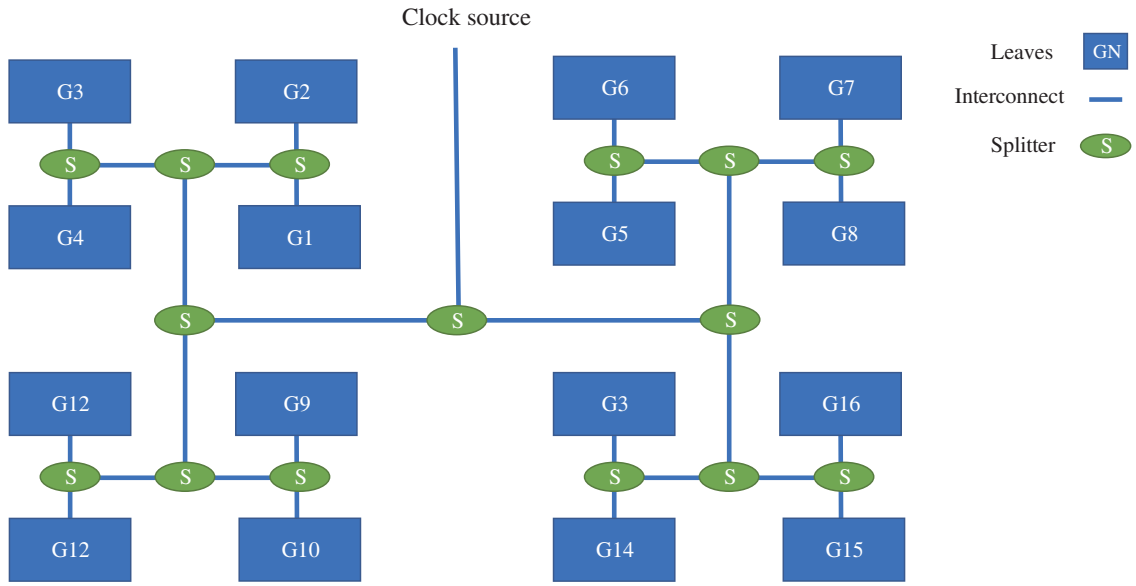


Figure 10. 16 leaf SFQ H-tree topology with splitters, interconnects, and leaves.

Local clock synthesis of SFQ circuits is used to produce a useful skew clock tree network within each block of the H-tree [29]. Different approaches to clocking SFQ circuits have been reported in the literature such as clockless self-timed systems [30], hierarchical chains of homogeneous clover-leaves clocking [31], and QuCTS – single-flux Quantum (SFQ) Clock Tree Synthesis [32]. A routing technique for asymmetric clock networks, based on QuCTS, is proposed in [32] to minimize the interconnect length and the number of delay elements to produce local clock skew within an SFQ clock tree [29]. QuCTS utilizes a two stage framework for synthesizing clock networks. During the first stage of the clock skew scheduling process, the arrival time of the clock signal for each gate is determined to increase the robustness of the circuit to timing variations. The second stage of the clock tree synthesis process generates the layout of the clock distribution network using a novel delay equilibration technique [32]. This approach makes QuCTS the first clock tree synthesis tool for SFQ circuits that utilizes useful clock skew. The synthesized network satisfies the clock arrival time requirements while minimizing associated overheads such as the interconnect length and the number of delay elements. The algorithm has been validated using a set of benchmark circuits [32].

## 9. CONCLUSIONS

The automated routing process determines the topology and methodology that connects the logic cells while satisfying design constraints. Routing in SFQ systems is preferably performed with one of two approaches, based on whether the path is local or global. Longer interconnects typically require higher routing priority. Design guidelines are provided to determine when to treat a line as either a global or local interconnect. Novel algorithms and topologies are presented to manage resonance, flux trapping, and coupling noise in VLSI complexity SFQ circuits. These specialized guidelines and algorithms enhance the automated layout and routing mothodologies used to synthesize VLSI complexity SFQ systems.

## ACKNOWLEDGMENT

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