Methodology for Placing Localized Guard Rings to Reduce Substrate Noise in Mixed-Signal Circuits

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***Abstract*— A methodology is proposed to improve the efficacy of placing guard rings to reduce substrate coupling noise in mixed-signal circuits. The methodology is based on a *localized* guard ring structure within an aggressor circuit by redesigning the standard cells in a library. Specifically, a noise aware library is generated where each standard cell contains a dedicated substrate contact. This library is used within the aggressor block. Dedicated contacts within the cells generate a *localized guard ring* structure within each aggressor block. The proposed methodology achieves enhanced isolation as compared to conventional guard rings by minimizing the number of vertical current paths within the substrate.**

I. INTRODUCTION

The ever increasing demand to integrate a variety of functions on the same monolithic substrate, commonly referred to as a system-on-chip (SoC), places stringent signal integrity constraints. The decreasing physical distance between the noisy digital circuits and the sensitive analog/RF circuits exacerbates this issue. A common coupling medium is the monolithic substrate, forming a conductive path between the switching digital circuits and the sensitive analog/RF circuits [1].

Three primary mechanisms exist for injecting noise into the substrate: coupling from the noisy digital ground and power rails, coupling from the junction capacitance of the devices during switching, and impact ionization [2]. The injected noise propagates through the substrate, reaching the boundary of the sensitive circuit. The substrate noise can affect the sensitive circuit by modifying the threshold voltage of the devices through the body effect or capacitively coupling into the power/ground and signal lines. Significant performance degradation and functional failure due to substrate noise have been demonstrated [3], [4], [5].

A common technique to reduce substrate coupling noise is to modify the transfer function of the substrate medium by placing guard rings around the sensitive or aggressor blocks [4]. These guard rings consist of substrate contacts (p+ diffusion areas for p- substrates) connected to a dedicated ground pad. The guard ring acts as a low impedance path, filtering the current noise within the substrate. The efficacy of conventional guard rings, however, is limited due to the vertical current propagation paths throughout the substrate. A portion of the noise current can flow deeper into the substrate, thereby bypassing the guard ring, making the isolation less effective. This inefficiency is significant, particularly in large aggressor blocks, since the noise current is more likely to spread throughout the substrate until the current reaches the guard ring surrounding the block.

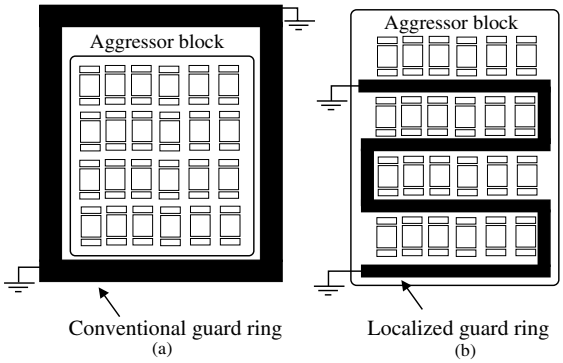

Fig. 1. Simplified representations of a (a) conventional guard ring around an aggressor block, (b) proposed localized guard ring within an aggressor block.

A methodology is proposed in this paper to improve the efficiency of guard ring structures by generating a localized ring within the aggressor block rather than placing the ring around the block, as illustrated in Fig. 1. This localized structure is achieved by designing a noise aware cell library where each cell contains a dedicated substrate contact that adds to the local guard ring. The proposed methodology reduces the substrate noise by 72%, on average, as compared to a conventional guard ring. Furthermore, the methodology can be automated within existing digital standard cell design flows.

The rest of the paper is organized as follows. Conventional guard ring placement and associated limitations are reviewed in Section II. The proposed methodology is described in Section III. Simulation results are presented in Section IV. Finally, some conclusions are drawn in Section V.

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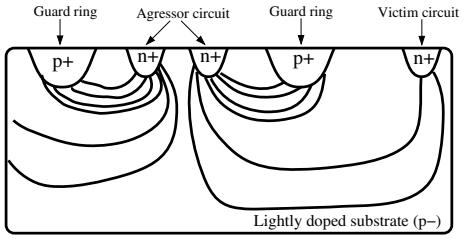
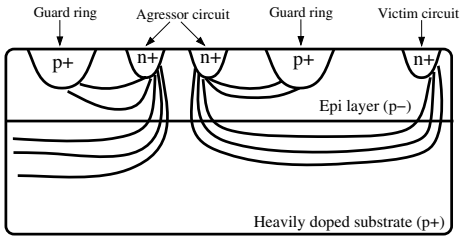


(a)



(b)

Fig. 2. Representative current flow within the substrate among a guard ring, aggressor, and victim circuit: (a) Lightly doped (bulk type) substrate, (b) Heavily doped (epi type) substrate.

II. CONVENTIONAL GUARD RING PLACEMENT

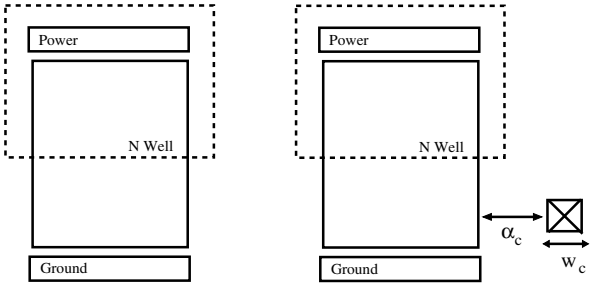
A guard ring is traditionally placed around a victim or an aggressor block to filter the noise current within the substrate. An order of magnitude and nine decibel reduction in the substrate noise has been shown, respectively, in [4] and [6]. The existing vertical current paths, however, limit the efficiency of conventional guard rings [4], [7], as illustrated in Fig. 2.

The flow of the current within a lightly doped substrate is illustrated in Fig. 2(a). The p+ contacts of the guard ring filter a significant portion of the substrate current generated by the aggressor circuit. The vertical current paths, however, bypass the guard rings, reaching the victim circuit. This limitation of conventional guard rings is more significant in heavily doped or epi type substrates since the bulk can be modeled as a single equipotential node, as illustrated in Fig. 2(b). The guard rings should therefore be placed as close as possible to an aggressor or victim block to enhance the isolation. A brief guideline is provided in [8] for placing and biasing guard rings.

The dependence of noise isolation on the width of the guard ring is investigated in [7]. The isolation is shown to be a weak function of the guard ring width. Increasing the width is therefore an ineffective technique for enhancing isolation. An alternative methodology is proposed in this paper to improve the isolation based on a localized guard ring rather than increasing the width, as described in the following section.

III. PROPOSED LOCALIZED GUARD RING METHODOLOGY

The design of a standard cell library with dedicated substrate contacts is explained in Section III-A. An analysis of the substrate noise reduction mechanism by generating a localized guard ring using these standard cells is described in Section III-B.



(a) (b)

Fig. 3. Standard cell: (a) Conventional cell, (b) Noise aware cell with a dedicated substrate contact for the local guard ring. α_c is the minimum distance between the contact and the diffusion, and w_c is the width of the contact.

A. Standard Cell with a Dedicated Substrate Contact

In the design of a digital integrated circuit, placing the substrate contacts is usually accomplished after the place-and-route phase of the design flow is completed. The latch-up design rules determine the minimum distance among the contacts.

A standard cell design approach is proposed in this paper where each cell in the library has a dedicated substrate contact used to generate a localized guard ring. This dedicated substrate contact is placed in close proximity to the cell, specified by technology based design rules. Conventional and *noise aware* standard cells are illustrated in Fig. 3. Note that these noise aware cells are in addition to existing conventional cells in the library. The choice between a conventional and noise aware cell depends upon several factors such as the switching activity of the digital blocks and the physical distance between the digital and sensitive analog blocks.

The physical representation of an aggressor device with a dedicated substrate contact is shown in Fig. 4. C_1 represents an existing substrate contact placed according to latch-up design rules and C_2 represents the dedicated substrate contact of the cell within the local guard ring. Note that C_1 is connected to the ground network of the digital circuit; a separate ground network, however, is necessary for the dedicated contacts to isolate these contacts from the noisy ground network. This isolation is required for the local guard ring to filter noise from the substrate rather than inject additional noise into the substrate. Noise reduction is achieved through the low impedance path between C_1 and C_2, and between the bulk of the aggressor device and C_2. The injected noise from the noisy contact C_1 and the bulk is filtered through C_2 rather than propagated into the substrate.

B. Analysis of Noise Reduction Mechanism

A localized guard ring significantly reduces the noise current propagating through the substrate. The current injected into the substrate is more effectively filtered by the local ring as compared to a conventional ring due to the decreased

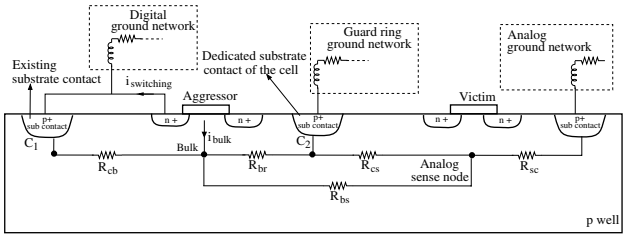


Fig. 4. The effect of the local guard ring on reducing substrate noise. The noise injected from the noisy contact C_1 and bulk of the aggressor device is filtered through the dedicated contact C_2 of the guard ring rather than propagated into the substrate.

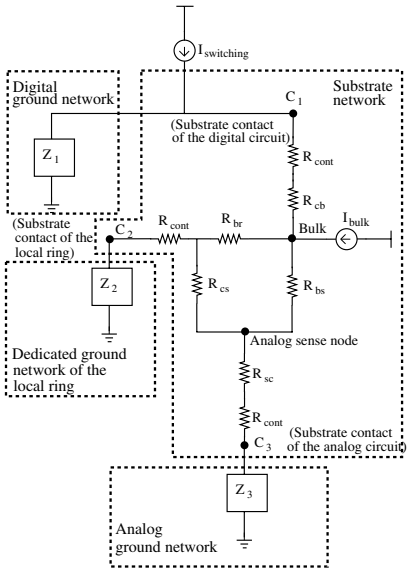


Fig. 5. Equivalent circuit model to analyze the effect of the localized guard ring consisting of the ground network of the digital circuit (Z_1), ground network of the local guard ring (Z_2), and ground network of the analog circuit (Z_3). The substrate network is represented by the equivalent resistance among the substrate contacts and the analog sense node.

substrate resistance between the noise source (the substrate contact and bulk of the aggressor circuit) and the noise filter (the substrate contact of the ring). The number of vertical current paths that bypass the ring are therefore decreased.

An equivalent circuit model to analyze the significance of a localized guard ring is shown in Fig. 5. Z_1, Z_2, and Z_3 represent, respectively, the parasitic impedance of the ground network of the digital (aggressor) circuit, dedicated ground network of the local guard ring, and ground network of the analog (victim) circuit. $I_{switching}$ and I_{bulk} represent, respectively, the switching current of the aggressor circuit and the bulk current injected into the substrate through the source/drain junctions. R_{cont} is the resistance of the substrate contact. A physical perspective of the substrate resistances is provided in Fig. 4.

The noise voltage at the analog sense node is determined from the superposition of the noise due to I_{swi} and I_{bulk}. Assuming the sense node is sufficiently far from the aggressor circuit to ensure that $R_{br} \ll R_{bs} \approx R_{cs}$, and the contact resistance and ground network impedance are much smaller

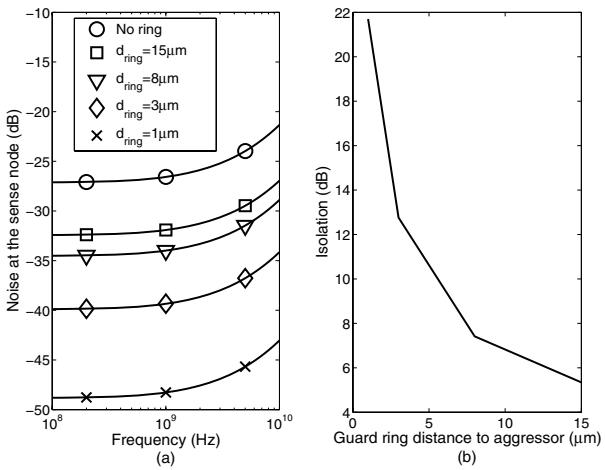


Fig. 6. Analytic model illustrating the significance of the distance of the guard ring from the aggressor: (a) Noise voltage at the sense node with respect to frequency, (b) Isolation as a function of distance of the guard ring from the aggressor.

than the substrate impedance, the noise current caused by the switching current I_{sense}^{swi}, bulk current I_{sense}^{bulk}, and noise voltage at the sense node V_{sense} can be approximated, respectively, as

$$I_{sense}^{swi}(\omega) \approx \frac{I_{swi}(\omega)Z_1(\omega)R_{br}}{(R_{cb}+R_{br})(R_{br}+R_{bs}+R_{sc})}, \quad (1)$$

$$I_{sense}^{bulk}(\omega) \approx \frac{I_{bulk}(\omega)(R_{br}\backslash\backslash R_{cb})}{(R_{br}\backslash\backslash R_{cb})+R_{bs}+R_{sc}}, \quad (2)$$

$$V_{sense}(\omega) \approx [I_{sense}^{swi}(\omega)+I_{sense}^{bulk}(\omega)](R_{sc}+R_{cont}+Z_3). \quad (3)$$

Assuming $Z_1 = Z_2 = Z_3$, the noise voltage predicted by (3) is illustrated as a function of frequency in Fig. 6(a) at different locations of the guard ring, *i.e.*, the distance d between the ring and aggressor circuit is varied. The isolation as a function of distance at 1 GHz is shown in Fig. 6(b), where the isolation is

$$\Delta V_{noise}(dB) = V_{sense}^{without\ ring}(dB) - V_{sense}^{with\ local\ ring}(dB). \quad (4)$$

Note that the substrate resistances have been extracted using SubstrateStorm [9] for a 90 nm CMOS technology with a bulk type substrate. As shown in Fig. 6, a localized guard ring ($d = 1\ \mu$m) achieves an additional isolation of 17 dB as compared to a conventional guard ring ($d = 15\ \mu$m), demonstrating the importance of the location of the guard ring. These results have been validated by an industrial circuit, as described in the next section.

IV. SIMULATION RESULTS

The proposed guard ring placement methodology has been evaluated on an aggressor digital core located close to a sensitive block in an industrial transceiver circuit designed in a 90 nm CMOS technology with a bulk type substrate. The layout of the aggressor circuit and the sense nodes where the substrate noise is observed are shown in Fig. 7. Three different versions of the circuit have been investigated. The

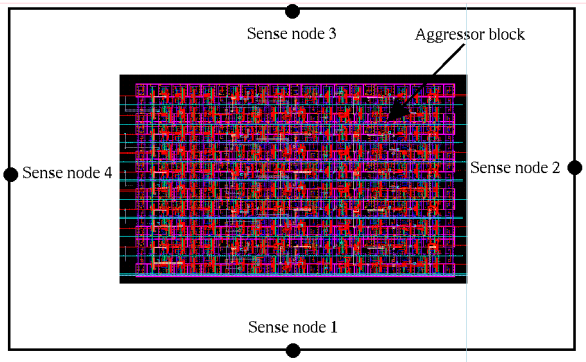


Fig. 7. Layout of the aggressor digital core located close to a sensitive block in an industrial transceiver circuit. The substrate noise is observed at the four sense nodes located on each side of the block.

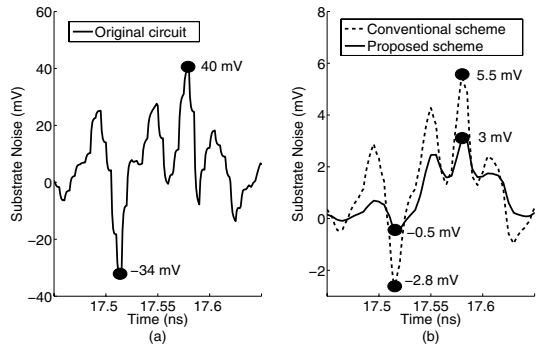


Fig. 8. Substrate noise voltages observed at sense node 2: (a) The original circuit, (b) Conventional and proposed guard ring schemes.

first circuit does not have a guard ring structure. The second circuit utilizes a conventional scheme where the guard ring is placed around the aggressor core. The third circuit utilizes the proposed methodology where the standard cells are replaced with noise aware cells and dedicated contacts are used to generate the localized guard ring scheme.

The layout and substrate impedances of the three circuits have been extracted using Assura and SubstrateStorm [9]. The substrate noise voltage is examined at the sense nodes, using Spectre. In addition to the extracted parasitic impedances of the on-chip ground distribution network, the bond wire package exhibits a parasitic impedance of 1 nH and 0.2 Ω.

The substrate noise voltage waveforms observed at sense node 2 are shown in Fig 8. The peak-to-peak substrate noise voltage for the original circuit is 74 mV, as illustrated in Fig. 8(a). The conventional guard ring scheme achieves an 89% improvement, reducing the peak-to-peak substrate noise to 8.3 mV. The proposed guard ring placement methodology achieves an additional 58% reduction with a peak-to-peak noise of 3.5 mV. The peak-to-peak noise voltage for conventional and proposed guard ring placement schemes are listed in Table I for the four sense nodes. On average, the proposed methodology reduces the peak-to-peak substrate noise voltage by 72% as compared to a conventional scheme. Note that the improvement obtained by the localized guard ring placement methodology will be greater in larger aggressor blocks and

TABLE I

COMPARISON OF PEAK-TO-PEAK SUBSTRATE NOISE VOLTAGE FOR CONVENTIONAL AND PROPOSED GUARD RING SCHEMES.

Sense location	Peak-to-peak substrate noise (mV)		Reduction in substrate noise
	Conventional	Proposed	
Sense node 1	15.1	1.5	90%
Sense node 2	8.3	3.5	58%
Sense node 3	21.5	6.5	70%
Sense node 4	5.7	1.7	70%

epi type substrates due to the additional vertical current paths within the substrate.

Two primary drawbacks exist for the proposed technique. One drawback is the increased area due to the additional substrate contacts since a contact is required for each cell in the aggressor block to generate the local ring. This increased area, however, is not significant since these modified cells are only used in the primary noise generating blocks within a circuit. The second drawback is the use of a metal layer to route the ring within the aggressor block. This metal layer separates the ground network of the ring from the ground network of the aggressor circuit.

V. CONCLUSIONS

A methodology is proposed for improving the efficiency of guard ring structures around an aggressor circuit at the expense of area and a metal layer. The guard ring is localized by redesigning each cell within a standard cell library with a dedicated substrate contact. These dedicated contacts generate a localized guard ring. The proposed methodology achieves enhanced isolation as compared to a conventional guard ring by decreasing the number of vertical current paths within the substrate. Furthermore, this methodology is amenable to automation since it is standard cell based.

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