INFORMATION TO USERS

This manuscript has been reproduced from the microfilm master. UMI films the text directly from the original or copy submitted. Thus, some thesis and dissertation copies are in typewriter face, while others may be from any type of computer printer.

The quality of this reproduction is dependent upon the quality of the copy submitted. Broken or indistinct print, colored or poor quality illustrations and photographs, print bleedthrough, substandard margins, and improper alignment can adversely affect reproduction.

In the unlikely event that the author did not send UMI a complete manuscript and there are missing pages, these will be noted. Also, if unauthorized copyright material had to be removed, a note will indicate the deletion.

Oversize materials (e.g., maps, drawings, charts) are reproduced by sectioning the original, beginning at the upper left-hand corner and continuing from left to right in equal sections with small overlaps.

Photographs included in the original manuscript have been reproduced xerographically in this copy. Higher quality 6" x 9" black and white photographic prints are available for any photographs or illustrations appearing in this copy for an additional charge. Contact UMI directly to order.

Bell & Howell Information and Learning
300 North Zeeb Road, Ann Arbor, MI 48106-1346 USA
800-521-0600

On the Interdependence of Substrate Coupling on Technology, Circuit, and Physical Design in Mixed-Signal Smart-Power Circuits

by

Radu M. Secareanu

Submitted in Partial Fulfillment

of the
Requirements for the Degree
Doctor of Philosophy

Supervised by

Professor Eby G. Friedman

Department of Electrical and Computer Engineering
The College
School of Engineering and Applied Sciences

University of Rochester
Rochester, New York

2000

UMI Number: 9972235

Bell & Howell Information and Learning Company
300 North Zeeb Road
P.O. Box 1346
Ann Arbor, MI 48106-1346

Dedication

To my parents, Ion and Georgeta, and to the many people that shaped my life.

Curriculum Vitae

The author was born in Campina, Prahova County, Romania, on September 18, 1965. He attended "Politehnica" University of Bucharest from 1985 to 1990 and graduated with a Master of Science degree in Electrical Engineering. His graduation thesis was *High Resolution Digital to Analog Converters*. From 1990 to 1995 he was with IPRS Semiconductor, Bucharest, Romania, working as a process, design, and R&D engineer on a variety of issues related to circuit design. He joined the University of Rochester in 1996 after completing one term at the University of Victoria in Canada. From 1996 to 2000 he was also a research assistant with Xerox Corporation, Webster, New York. In 1998, he received his Master of Science degree in Electrical Engineering from the University of Rochester. He pursued research in VLSI circuit design under the direction of Professor Eby G. Friedman from 1996 to 2000 in the areas of substrate noise in mixed-signal circuits and high performance analog and digital circuit design.

Acknowledgments

Life is a series of decisions we make. We all want the decisions to be successful; we can estimate the degree of success for a particular decision, but we only find out for sure after we make them. I consider that coming to the University of Rochester for my graduate studies was one of the best decisions I made in my life. The principal reason is because Professor Eby G. Friedman led my steps throughout my graduate studies with unmatched dedication and commitment to excellence as my advisor. During these years, I learned from Prof. Friedman not only highly valuable knowledge in integrated circuit design from his vast knowledge and experience, but I also learned very important lessons and experience for my career, either academic or industrial, and for life. Prof. Friedman made the time I spent at University of Rochester highly enjoyable and rich in research and academic achievements; he made all of the hard work seem effortless. I consider Prof. Friedman the ideal mentor for any student; for me he is an ideal mentor and example in my research, academic, and personal growth, and a mentor for my life.

I would like to give special thanks to Prof. Michael Kriss, Prof. Mark Bocko, and Prof. William Forrest for their valuable suggestions and for serving on my committee. I would also like to thank Prof. David Albonesi for his suggestions and ideas for my research. Special thanks to RuthAnn Williams for coordinating all the paperwork over the years.

I would like to express my appreciation to Xerox Corporation, Webster, New York, which, besides paying the bills, provided a large part of the support for my research; chip fabrication, test equipment, lab space, and valuable suggestions and support by the following specialists: Juan Becerra, Cathie Burke, Tom Watrobski, Tom Tellier, Christopher Morton, Scott Warner, Scott Seabridge, and William Staub.

If my special acknowledgments would measure the time and memories, then my fellow graduate students in the VLSI Design and Analysis Laboratory at University of Rochester (my office and lab) deserve the most: Victor Adler, Ivan Kourtev, Kevin Tang, Andrey Mezhiba, Dimitris Velenis, Jose Neves, Tolga Soyata, and Yehea Ismail.

At the University of Rochester, I met high quality people; faculty, staff, students. I would like to acknowledge Prof. Marc Feldman, Prof. Alexander Albicki, Prof. Philippe Fauchet, Prof. Vasillious Tourassis, Prof. Murat Tekalp, as well as Jim Prescott, John Simonson, John Strong, Maureen Muar, Debra Neiner, Dorothy Welch, Sandra Garcia, Mary Beth Vogel, Amy Freitas, and Melissa Singkhamsak. I would also like to acknowledge fellow students; Selena Chan, Shiloh Dockstader, Cesar Mancini, Laura Burattini, Stephen McAleavey, Nenad Nenadic, Christopher Streimer, Carlo Williams, Michal Volkin, Herman Lopez, Julie Heinrich, Christen Roberts, Lynn Czerwonka, and many, many others.

Many people, across my life, besides the above, significantly influenced my path in life and contributed to this important professional step of mine, and I would like to acknowledge them: Elisabeta, Ion, Maria, Gheorghe, Constantin, Eliade, Veronica, Ion, Dana, Iorgandopol, Elena, George, "Terra", Nelu, Neli, Silu, Mircea, Anca, Anton, Adrian, Gabriel, Marieta, Mihai, Tina, Russ, Harry, and many, many others.

Finally, I would like to thank God for giving me this path in life.

Abstract

Multi-million transistor digital systems have become commonplace, and the number of transistors is expected to increase further as described by Moore's law. Systems-on-a-chip (SOC) is a new trend intended to exploit the advantages offered by deep submicrometer (DSM) CMOS technologies. An SOC is a complex mixed-signal circuit composed of analog, digital, high power, low voltage, and/or high voltage circuit blocks, all of which must coexist with minimal interaction.

An important parasitic interaction among circuits sharing a common substrate is substrate coupling noise (SCN). SCN may affect the signal integrity of both the digital and analog portions of a circuit. During the past decade, the tolerance of analog circuits to substrate coupling noise has been investigated. The effect of substrate coupling noise on digital circuits is the focus of this dissertation, particularly targeting mixed-signal applications. The research described in this dissertation can also be seen as a starting point for a research problem that will become significant in the near future: substrate coupling noise in multi-million transistor DSM digital applications.

The experimental results derived from test circuits and described in this dissertation address the most common, lowest cost semiconductor technologies: NMOS and N-well CMOS. The primary focus is on developing circuit and physical design solutions to improve the tolerance of digital circuits to substrate noise, targeting low cost SOCs and multi-million transistor DSM digital applications.

Design solutions for reducing the substrate noise interacting with the circuit are presented. Circuit and physical design techniques are provided to decrease the noise that is generated, transmitted throughout the substrate, and received by the digital circuits. Solutions to improve the noise behavior of digital circuits by tolerating larger amounts of noise are demonstrated. Theoretical expectations are compared with simulation and experimental data for both NMOS and CMOS circuits. While the research presented in this dissertation primarily addresses digital circuits, these results can also be used to enhance the immunity of analog circuits to substrate coupling noise.

Contents

List of Tables

List of Figures

Chapter 1

Introduction

The dramatic technological revolution that occurred in electronics between 1948 and 1958 created practically a new world. John Bardeen, Walter Brattain, and William Schokley discovered the point-contact transistor at Bell Laboratories on December 23, 1947 [1, 2]. The first public announcement of the invention was made on June 30, 1948 [3, 4]. Shortly after this event, Shockley invented the junction bipolar transistor [5]. Towards the end of the 1950's, technological attention turned to silicon due to major technological advantages such as the existence of a native oxide (SiO_2) [6, 7]. In 1958, Jack Kilby of Texas Instruments and almost simultaneously Robert Noyce of Intel demonstrated the first working bipolar integrated circuit (IC) where multiple transistors coexisted on the same physical substrate. In 1960, J. Hoerni described the planar process [8]. Also in 1960, D. Khang and M. Atalla demonstrated the first Si based MOSFET [9], followed in 1967 by the first Si-gate MOSFET [10]. These inventions formed the basis for today's multi-billion dollar microelectronics industry.

While the first microelectronic circuits were primarily analog bipolar, digital applications, typically in MOS technologies, also developed rapidly. In November 1971, Intel developed the first fully integrated microprocessor (4004) and memory

circuits (1103) [11], both based in PMOS technology. These products represent the beginning of today's digital era. More sophisticated functions were included on the same monolithic substrate, such as systems containing both high precision and high power analog circuitry. The concept of a *mixed-signal* system, where digital circuits and analog circuits are both physically on the same monolithic substrate, was introduced [12]. *Digital-to-Analog Converters (DAC)* and *Analog-to-Digital Converters* (ADC) were among the first mixed-signal applications to be implemented monolithically. The first monolithic implementations of a DAC used bipolar transistors with a passive resistor network, such as Pastoriza's four bit implementation [13]. For technological and precision reasons, the resistor network was fabricated in thin film technology on a ceramic substrate. One of the first significant fully monolithic implementations of a DAC was a six bit implementation realized by D. J. Dooley in 1971 [14]. A five bit parallel ADC was proposed by D. R. Breuer in 1972 [15], the work being performed under an Air Force contract. The final converter was, however, a multi-chip implementation.

The first power integrated circuits evolved from bipolar devices, targeting analog applications such as voltage regulators, motor drivers, and audio power amplifiers. Up to the early '80's, the primary way to combine analog power circuitry and digital control blocks into one application at a competitive price was by employing a multiple die (hybrid) solution [16]. The hybrid solid-state relays were an important step in the realization of mixed-signal high-power systems. In the early '80's [16, 17], however, many companies developed price competitive processes that integrated on the same IC both analog power circuits and digital control circuits, creating the so-called *smart-power* class of circuits. In particular, the automotive industry was a primary contributor to the development of these type

of circuits [18–20]. Among the many companies developing smart-power process technologies during this period were Texas Instruments, Sprague, SGS Semiconductor, General Electric, Motorola, Siemens, and Unitrode [16, 17, 21]. The first smart-power processes were purely bipolar, based on an IIL[1] (or I^2L) [22] technology. More sophisticated and higher cost smart-power technologies were later developed [16, 17, 21]. An example of a typical high performance smart-power process, based on a very complex technology, is BCD[2] [23] (see Section 2.3 for more details on BCD technology).

Currently, there are a large variety of processes, such as deep submicrometer (DSM) digital only CMOS processes, DRAM[3] specific processes, processes that integrate on the same IC high-power analog circuitry with highly sensitive analog circuitry, or digital circuitry with highly sensitive analog circuitry (such as DACs and ADCs converters), or high-power analog circuitry with digital circuitry (such as smart-power circuits). Each of these processes are faced with the fundamental problem of noise, and in particular, *substrate coupling noise* (SCN). For example, in DSM digital processes, due to the inherently low supply voltages, low transistor threshold voltages, as well as short channel and short width phenomena [24], SCN can create parasitic signal glitches, destroying logic states or even inducing latch-up [25–29] (due to the parasitic bipolar transistors present in short-channel devices). In DRAM processes, SCN can parasitically charge or discharge the DRAM capacitors and degrade the operation of the sensitive sense amplifiers. A small signal, high precision analog amplifier can be influenced by the high power analog circuitry present on the same monolithic substrate. Today, SCN in digital DSM CMOS has not, as yet, become a fundamental issue, but as technologies

[1]Injection Injection Logic
[2]Bipolar, CMOS, and DMOS
[3]Dynamic Random Access Memory

continue to scale, decreasing the magnitude of the power supply and threshold voltages, SCN in DSM circuits will also become of increasing importance.

A classic problem in mixed-signal systems is the high speed digital circuitry influencing the highly sensitive analog circuitry due to the noise generated by the high frequency switching within the digital circuit. The noise is transmitted through the common substrate, and received by the sensitive analog portion of the circuit. This circuit configuration is schematically depicted in Fig. 1.1. Due to the important market that analog (and mixed-signal) circuits represent (such as A/D and D/A converters), and due to the high level of precision required by these analog signal processing circuits, SCN in these mixed-signal circuits is an important problem which is currently under significant investigation.

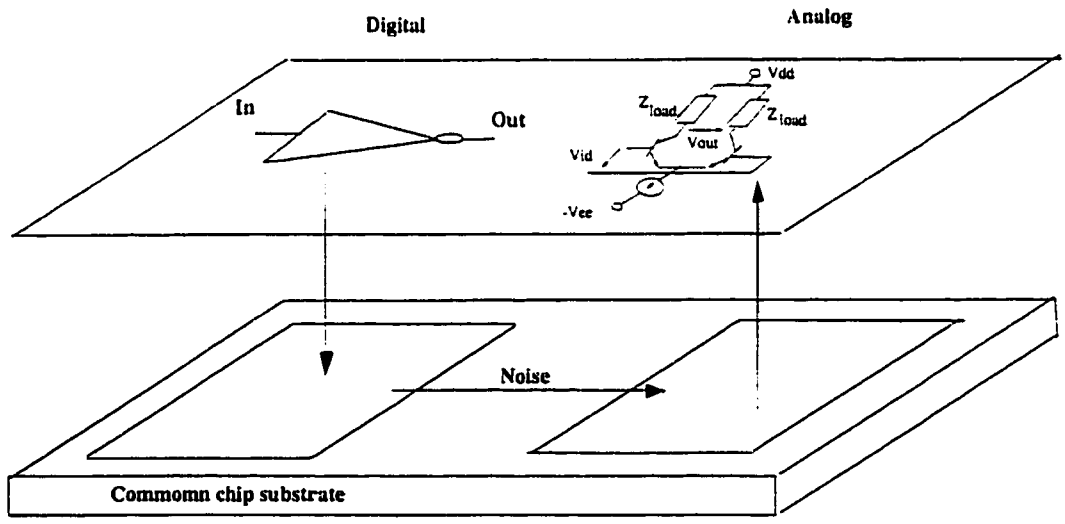


Figure 1.1: Digital circuitry influencing the highly sensitive analog circuitry in mixed-signal circuits.

The precision required by the analog processing in a DAC depends upon the bit resolution of the converter. Currently, there are high precision monolithic DAC implementations with precisions of 16 to 24 bit resolution (*e.g.*, DAC56, DAC 729,

PCM1702P, PCM1702U, PCM1728) [30]. Consider a 16 bit implementation (*e.g.*, the DAC56), with a full range voltage output of 6.5536 V. This voltage range is equivalent to an LSB[4] voltage level of $6.5536/65536 = 100\,\mu$V. Typically, the specified precision level for a DAC is 1/2 LSB. For this converter, the required precision is therefore $50\,\mu$V. If more bits of resolution are necessary, the required precision level is even greater. This precision level must include the effects of all types of nonlinearities, errors, and noise. SCN for these types of high precision circuits has therefore received a great deal of attention.

To attain the high level of accuracy required for 16 to 24 bit converters, Burr-Brown, for example, uses a thin film monolithic DAC process, a dielectric op-amp process, a hybrid technology, advanced laser-trim techniques, bipolar and BiCMOS processes, and specialized circuit and architectural techniques-[30]. Recent techniques to achieve these high accuracies and to eliminate noise use specialized *noise shaping techniques*, such as Bitstream and MASH [30], which obtain higher accuracies at the expense of decreased signal-to-noise ratio (SNR). A recent high performance circuit approach to obtain high accuracies and high SNR that eliminates glitches (that could be induced by substrate coupling noise) and large linearity errors is a complementary linear or advanced sign magnitude technique [30]. This technique consists of two similar DACs placed on the same monolithic substrate which share a common reference and a common R-2R ladder to provide the bit current sources. The two DACs are combined in a complementary arrangement to produce a highly linear output.

The primary effect of SCN in a DAC is degradation of the precision of the analog signal processing circuits. In smart-power circuits, the problems of SCN are quite different due to the following reasons:

[4]Least Significant Bit

- In smart-power circuits, the noise is generated by the high voltage, high current analog circuits.
- The smart-power technologies significantly reduce the amount of transmitted noise through the substrate as compared to a standard digital technology (see Section 2.3).
- The noise is received by the sensitive circuitry which, in a mixed-signal smart-power system, processes the digital signals (as compared to the analog signals in a DAC).

This research focuses on studying the technology, circuit, and physical design issues that influence the interaction between the high-power analog circuitry and the digital circuitry sharing the same monolithic substrate, as shown in Fig. 1.2.

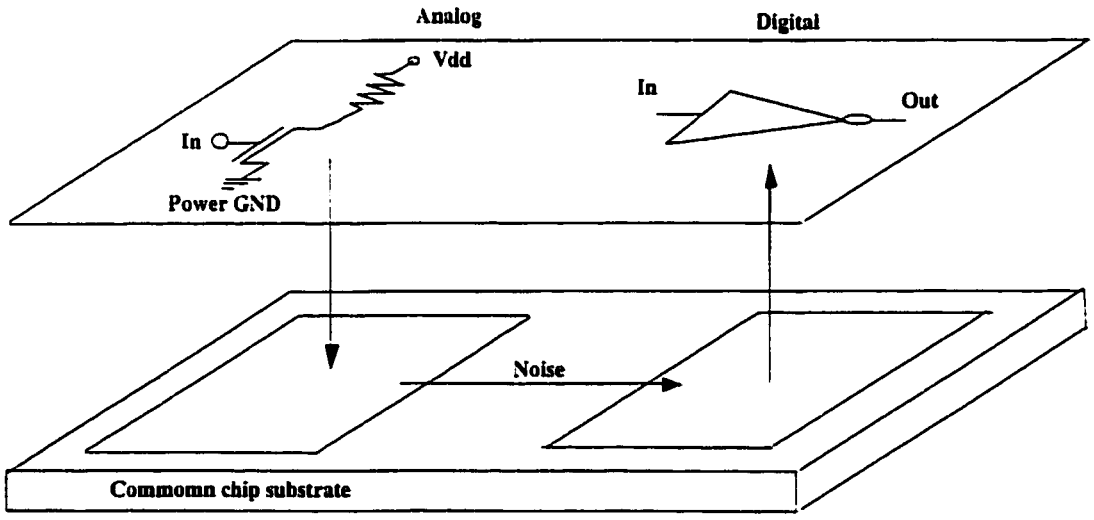


Figure 1.2: Noise coupling in smart-power circuits.

Note in Fig. 1.2 that the analog circuitry influences the digital circuitry through the common substrate. The primary objective of this research is to determine

the principal issues that generate, transmit, and receive noise in mixed-signal smart-power circuits in high voltage, low cost MOS processes. A second research objective is to determine the effect of the received noise on different families of digital circuits as well as to investigate the principal mechanisms by which the substrate noise affects a logic family. Finally, an important research objective is to develop techniques to minimize the deleterious effects of substrate coupling noise in these mixed-signal smart-power circuits. To achieve these research objectives, the experimental work in this research effort focuses on mixed-signal smart-power integrated circuits used in the Thermal Ink Jet (TIJ) printers designed and manufactured at Xerox Corporation.

In Chapter 2 of this research proposal, SCN is defined and the primary research issues related to SCN that have been reported in the literature are described. The importance of choosing the appropriate technology for a given application, as well as the process cost, maturity, availability, and the trade-offs among these criteria with respect to SCN are outlined. The principal research results describing how digital circuits influence analog circuits, specifically the generation, transmission, and reception of substrate noise, are reviewed in detail in this chapter.

The focus of Chapter 3 is to describe the development of a strategy for the practical analysis of the noise behavior of NMOS digital circuits. To accomplish this, the high-voltage NMOS process is characterized from a noise point of view, and a number of general and smart-power specific issues that influence the generation, transmission, and reception of noise are investigated.

The objective of Chapter 4 is on defining and describing several models, mechanisms, and effects that describe the process in which digital circuits are affected by substrate noise. A thorough characterization of both an NMOS inverter and an NMOS latch under the influence of substrate noise based on the previously described models, mechanisms, and effects, is provided in Chapter 5.

The experimental data gathered from the analysis of a large number of fabricated NMOS test circuits is presented and discussed in terms of the theoretical expectations, proposed models, and simulation results. This topic is reviewed in Chapter 6. Several noise mitigation techniques are also developed.

The theoretical analysis described in Chapters 4 and 5 and the experimental results from Chapter 6 suggest that the placement of substrate contacts represents a powerful physical design technique to reduce the amplitude and spreading of substrate noise and therefore improve the noise behavior of these circuits. A methodology for efficiently placing substrate contacts to reduce the influence of substrate noise, addressing both NMOS and CMOS technologies, is described in Chapter 7.

Similar to Chapter 4 for NMOS circuits, a theoretical analysis of the noise behavior of CMOS digital circuits is performed in Chapter 8. The latch-up phenomenon is discussed in detail. The sensitivity of latch-up to technology scaling is estimated. The behavior of both a CMOS inverter and a CMOS latch under the influence of substrate noise is analyzed and characterized.

The experimental data gathered from the analysis of a large number of fabricated CMOS test circuits are presented and discussed in detail according to theoretical expectations, the proposed models, and the simulation results. This topic is reviewed in Chapter 9. The importance of substrate noise in multi-million

transistor digital applications implemented in DSM CMOS technologies is also discussed in Chapter 9.

A summary with some conclusions are offered in Chapter 10. Possible future work in the area of substrate coupling in mixed-signal systems is outlined in Chapter 11.

Chapter 2

Overview of Substrate Coupling Noise

According to Webster's Dictionary [31], *noise* is defined as "an undesired, or unwanted, or irrelevant, or meaningless signal, or data, or disturbance, or output interfering with the desired information, or with the operation of a device or system." In any system, either electrical, mechanical, or of any other nature, a constant focus consists in finding ways to eliminate any present noise, since by its nature, the noise is *"unwanted."* There are fundamental types of noise that cannot be eliminated. Fortunately however, techniques, technologies, and methodologies to reduce or eliminate a large number of types of noise and the associated problems have been developed.

2.1 Electrical Engineering and Noise

In electrical engineering, noise can be found at all levels, starting with materials and ending with complex systems and equipment. At the material and device levels [32], thermal noise (caused by the random motion of current carriers), flicker noise (or 1/f noise, due to the semiconductor surface effect), and shot noise (which

constitutes the major source of noise in most semiconductor devices), are the fundamental types of noise [32]. A different terminology classifies the noise according to the physical processes: generation-recombination noise, diffusion noise, and modulation noise [32]. The generation-recombination noise is caused by spontaneous fluctuations in the generation, recombination, and trapping rates of the carriers. For junction devices this source of noise exhibits a close resemblance to shot noise. The diffusion noise is caused by the fact that diffusion is a random process. In bulk material it is the cause of thermal noise. In junction devices, it is a major contributor to shot noise. The modulation noise refers to carrier density fluctuations caused by modulation mechanisms such as surface field effects.

At the circuit level, application and technology dependent noise exists. Noise is present in digital applications, in analog applications, as well as in mixed-signal applications such as *analog influencing digital* or *digital influencing analog* applications.

The main result of the presence of noise is signal degradation, either digital signals or analog signals. Digital signal degradation implies parasitic transitions of the data path, while analog signal degradation is manifested by parasitic harmonics [33]. In a mixed-signal system, the noise influence affects the ability to correctly recover a signal either from analog to digital or from digital to analog domains. In all cases, the final result of the analog, mixed-signal, or digital signal processing is affected, which is reflected at the system level in the final application or equipment.

2.2 Noise in Mixed-Signal Circuits

A mixed-signal circuit, where both analog and digital circuits coexist and share a monolithic substrate, is a more complex case from the noise point of view as compared to a pure analog or a pure digital circuit. That is, in a mixed-signal circuit, besides the existence of the specific analog and digital noise problems, the interactions between the analog and digital portions create significant additional problems.

The interaction between the analog and digital portions of the circuit creates two major noise problems in a mixed-signal system: noise induced by capacitive coupling and by substrate coupling (SCN). Both problems exist in a pure digital or a pure analog system, however, their importance increases in a mixed-signal system. The effects of capacitive coupling and substrate coupling noise in a mixed-signal system depend on a multitude of factors, and are different for a *digital influencing analog* as compared to an *analog influencing digital* type of application. Inductive coupling effects are present in a smaller range of applications, such as RF applications and have just begun to become important in very high speed digital applications [34–37].

2.2.1 Capacitive Coupling Noise

Capacitive coupling is an important problem in any type of application, analog, digital, or mixed-signal. It has been extensively studied for digital applications [38–41], since the signal integrity of the on-chip signals has become an important issue as the speed of digital applications continues to increase and the digital technologies continue to be scaled.

In analog and mixed-signal design [42, 43], the problem of capacitive and crosstalk noise have different aspects as compared to a digital circuit, even if the basic mechanism remains the same. The difference is due to the fact that, as shown in Chapter 1, for an analog/mixed-signal application almost any amount of noise is important, *i.e.*, any amount of noise induced by a switching digital signal into a neighboring analog signal line can degrade signal quality in the analog portion of the system.

2.2.2 Substrate Coupling Noise

For both *digital influencing analog* and *analog influencing digital* types of applications, as shown in Fig. 1.1 and 1.2, a noise source, a transmission medium (the substrate), and a noise receptor exists as shown in Fig. 2.1. The source-transmission medium-receptor triad is valid for any type of noise.

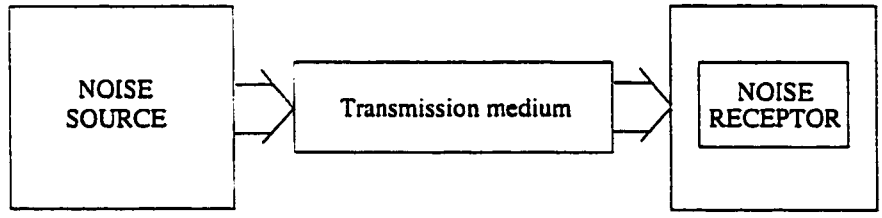


Figure 2.1: Noise coupling – the general case.

However, as mentioned in Chapter 1, major fundamental differences exist between the *digital influencing analog* and *analog influencing digital* type of applications regarding the process of noise generation, transmission, and reception. Substrate coupling noise received attention primarily in mixed-signal circuits, specifically, where the high speed switching digital circuitry influences the high precision analog circuitry (see Fig. 1.1). Typical applications of this category of circuits are

A/D and D/A converters. In this chapter, the primary research issues related to SCN which have been reported in the literature are summarized.

In Section 2.3, the importance of choosing the appropriate technology for a given application, as well as the process cost, maturity, availability, and the trade-offs among these criteria with respect to SCN are outlined. Typical noise waveforms and noise flow through the substrate are described in Section 2.4 and Section 2.5, respectively. Substrate modeling is reviewed in Section 2.6. The principal research results describing how digital circuits influence analog circuits, specifically the generation, transmission, and reception of substrate noise, are reviewed in Section 2.7.

2.3 Technologies and Noise Coupling

The generation, transmission, and reception of substrate noise is significantly influenced by the technology chosen to implement an application. The most important technologies are reviewed in this section. The sensitivities of these technologies to SCN are discussed qualitatively. Quantitative aspects, described in the literature, are reviewed in Section 2.7. As previously discussed in Chapter 1 and Section 2.2.2, SCN has been extensively studied for *digital influencing analog* applications, such as DACs. In Section 2.7, these SCN studies are presented. Two major categories of technologies are used to present the results shown in Section 2.7. These are technologies using substrates consisting of a lightly doped epitaxial layer grown on a heavily doped bulk, referred to here as *heavily doped substrates*, and technologies using lightly doped bulk substrates, referred to here as *lightly doped substrates*. In this section, reference to Section 2.7 is suggested for additional, more detailed information.

2.3.1 NMOS (PMOS) Technology

From an SCN sensitivity point of view, NMOS and PMOS technologies, exemplified in Fig. 2.2a, are similar to the *lightly doped substrate* case. Additional quantitative information describing SCN in these technologies is described in Sections 2.5 and 2.7.

2.3.2 DRAM Technologies

A high density DRAM process is exemplified in Fig. 2.2b (Epitaxy Over Trench process [44]). The use of three-dimensional integration is necessary due to the need for both high capacitance and small cell size. The planar (two-dimensional) capacitor requires a large cell to provide the necessary capacitance. The DRAM capacitor is highly susceptible to noise due to the parasitic charge/discharge process of the DRAM capacitor. Another reason is the sensitivity of the DRAM capacitor to noise, due to its exposure to noise as shown in Figs. 2.2b and 2.7a. This exposure to noise is generated due to the depth of the capacitor into the substrate. Note from the two figures that, since the noise path is predominantly at the interface between the epitaxial layer and the bulk (Section 2.5), the noise path passes through the body of the DRAM capacitor. Also, the sensitive analog sense amplifiers are affected by noise in a similar way as the sensitive analog circuitry is affected by noise in a DAC.

2.3.3 CMOS Technologies

- **CMOS Technologies Without Epitaxial Layer** (Fig. 2.2c) From an SCN sensitivity point of view, this technology is similar to the *lightly doped*

substrate case. Additional quantitative information describing SCN in these technologies is described in Sections 2.5 and 2.7.

- **CMOS Technologies with epitaxial layer** (Fig. 2.2d)

  From an SCN sensitivity point of view, this technology is similar to the *highly doped substrate* case. Additional quantitative information describing SCN in these technologies is described in Sections 2.5 and 2.7.

- **Double Well CMOS Technologies** (Fig. 2.2e) Each device is isolated in a N-type or P-type well using a *junction isolation* technique (see Section 2.3.7). The noise path between any two transistors must cross through two reverse biased well–epitaxial layer junctions, twice through the epitaxial layer, and through the bulk (see Fig. 2.2e). The improved isolation between any two devices significantly reduces the noise interaction, for example the carriers will recombine.

- **High Voltage CMOS (NMOS), Special CMOS Technologies** (see Fig. 2.2f). High voltage technologies are similar to those illustrated in Figs. 2.2a, 2.2c, and 2.2d. Additional process steps are added to produce the high voltage devices. For example, if the NMOS transistors are power transistors, a drift N- region is added (see Fig. 2.2f). Also, the special CMOS process shown in Fig. 2.2f consists of isolating each device with deep wells which could be either deep isolation diffusions as in bipolar processes or wells obtained through anisotropic etching (Section 2.3.7). Device isolation is an important issue in high voltage technologies and is discussed more extensively in Section 2.3.7. Substrate coupling noise increases for high voltage processes, due to the high voltages and high currents that are switched, and

is directly dependent on the techniques used to isolate the devices. The special CMOS process with improved isolation enhances the noise behavior, decreasing the transmitted noise.

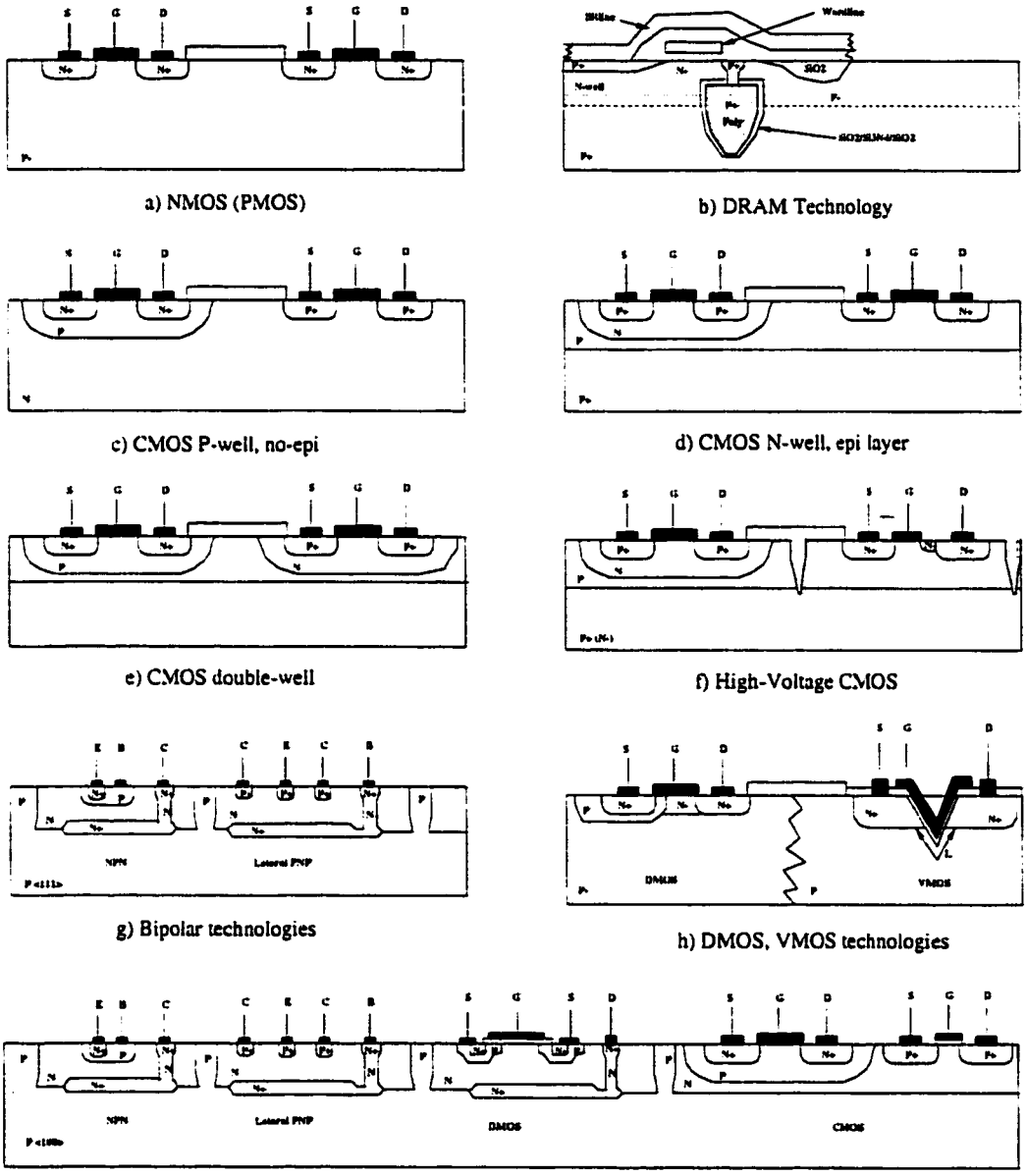


Figure 2.2: Overview of different semiconductor technologies

- **DSM CMOS Technologies** The noise behavior of DSM CMOS technologies deteriorates due to short channel and short width device sizes [24]. The gain of the parasitic bipolar transistors is increased due to the decreased base thickness (increased β). Under substrate noise influence, the sensitivity to latch-up increases [25, 26, 28]. The increase in latch-up sensitivity is significant if high voltage circuitry is present on the same substrate with DSM low voltage circuitry. Increasing device separation or increasing the device size in the potentially sensitive low voltage circuit, reduces noise sensitivity. SCN is expected to become significant in DSM CMOS even for those applications that employ only low voltage DSM circuits as the device and interconnect dimensions continue to shrink, since the parasitic bipolar effects will increase in importance, the power supplies and threshold voltages will decrease, decreasing the effective noise margin.

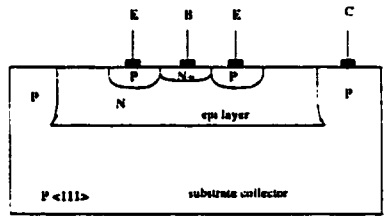


Figure 2.3: A vertical (substrate) PNP transistor

2.3.4 Bipolar Technologies

The noise behavior of bipolar technologies, exemplified in Fig. 2.2g is typically better than CMOS technologies due to the device isolation (see Section 2.3.7 for additional information). The devices are naturally isolated using *junction isolation* techniques. However, since the vertical PNP transistors use the substrate as

an active layer, these transistors collect the substrate current flow (see Figs. 2.3 and 2.7) and become affected by substrate noise. Therefore, vertical PNP transistors should not be used in noise sensitive circuitry.

2.3.5 DMOS (VMOS) Technologies

Typically, DMOS and VMOS structures, exemplified in Fig. 2.2h, are high voltage devices. The generated noise is expected to be large due to the high voltages and currents that are switched. However, due to the unusual design of these devices, the electric fields are smaller and/or the switching speeds are greater than in typical CMOS devices. Therefore, DMOS (VMOS) devices benefit from the noise point of view as compared, for example, to high voltage NMOS devices.

2.3.6 BiCMOS Technology

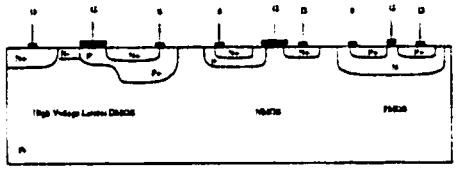
This technology, exemplified in Fig. 2.2i, combines the advantages and noise properties of CMOS and bipolar technologies (see Sections 2.3.3 and 2.3.4). In addition, the CMOS and bipolar portions interact through a common substrate. This interaction can be important depending on the application, device sizes, transistor biasing, and other related aspects [45].

2.3.7 Smart-Power Technologies

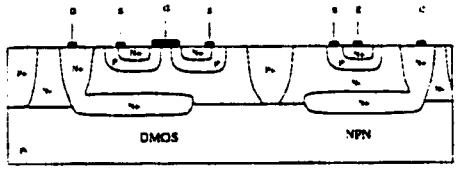
Smart-power technologies are typically highly sophisticated and costly. The sophistication comes from the necessity to obtain high performance power devices (both high voltages and high currents), and to isolate the high voltage transistors from the sensitive circuitry to maintain minimum device interaction through media such as the common substrate. Typically, three types of isolation techniques are

employed: *self-isolation*, *junction isolation*, and *dielectric isolation* [17, 18, 46–49] (see Fig. 2.4). These isolation techniques consist of:

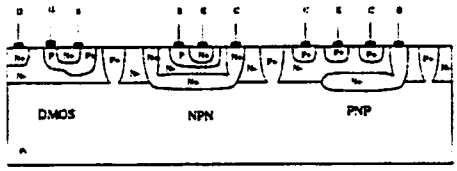
- The *self-isolation technique* (see Fig. 2.4a) consists of isolation through the reverse-biased junction between the source-drain region and the body region. This isolation technique occurs naturally. However, supplemental process steps are required for the high voltage transistors. The drain must be completely surrounded by the gate and source regions.



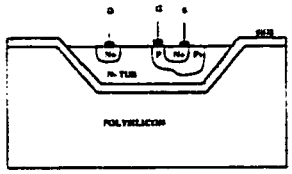
a) The self-isolation technique



b) The thick-epitaxial layer junction isolation technique



c) RESURF junction isolation technique



d) Dielectric isolation technique

Figure 2.4: Examples of common isolation techniques used in high voltage and/or smart-power IC technologies

- The *junction isolation technique* (see Fig. 2.4b and Fig. 2.4c) utilizes the ability of a reverse biased epitaxial-substrate junction to provide isolation. In Fig. 2.4b, a thick epitaxial layer is used to isolate the high voltage devices. This technique offers the advantage of high performance for the high voltage transistors, but low performance for the low voltage devices due to the thick epitaxial layer. The second technique shown in Fig. 2.4c uses a thin (5 to 8 μm) epitaxial layer optimized to obtain high performance, low voltage devices. To obtain the high voltage transistors, the *RESURF* principle [50] is used, which is based upon using a low, optimized charge in the N- epitaxial layer. This limited charge forces a two-dimensional redistribution of the electrical field so that a high voltage can be supported laterally between the source and drain of the DMOS transistor. The breakdown voltage of the high-voltage device is adjusted by varying the distance between the gate-to-drain and source-to-drain regions.

- The *dielectric isolation technique* (see Fig. 2.4d) uses oxide to isolate the devices. An example is the *etch-refill* process [51]. A particular case of this isolation technique is SOI[5] technology [18, 47]. The advantages of this isolation technique are: the ability to integrate a variety of high performance components, excellent immunity to latch-up, operation at high temperatures, and higher packing densities due to the smaller area required by the isolation region.

Note that the better the isolation technique, the more complex and expensive the process.

[5]Silicon-On-Insulator

Many attempts to reduce technology costs without compromising performance have been made. All of these attempts intend to develop low cost techniques to allow a standard process to integrate circuit functions for which the process was not originally designed [52, 53]. Some of these attempts reduce the substrate coupling noise in a standard low-cost process by

- Including circuit sensing functions for overcurrent, short-circuit, and open-loop detection [54] to predict large amounts of noise and to increase reliability.

- Using forward biased N+ guard ring diodes to generate a relatively large on-chip capacitance. This variable capacitance is resonant with the substrate lead inductance to form a low impedance path to ground [55].

- Using a guard ring to detect the magnitude of substrate noise. Based on this detected noise signal, an operational amplifier produces a noise cancellation signal that is the inverse of the substrate noise magnitude. This operational amplifier actively injects this noise cancellation signal into the substrate through another guard ring, suppressing the substrate noise [56].

Less process sophistication implies a lower cost for the technology. However, the interaction between the analog and the digital sections generally increases as the process sophistication decreases, creating more SCN problems.

2.3.8 Other technologies

Improvements and/or combinations of the aforementioned technologies exist. For example, in Fig. 2.2i, a BCD (BiCMOS process that includes DMOS devices)

process is depicted which is particularly appropriate for high performance smart-power applications. The interaction between the different devices for this process is through the common bulk. Combinations of these technologies exist, such as a CMOS double-well with junction isolation between devices and NMOS with epitaxial layer. As shown, a key factor in substrate noise immunity is device isolation.

2.3.9 The relationship between application, technology, and noise

For the same technology, different applications behave differently to SCN. For example, a CMOS technology with an epitaxial layer that includes high sensitivity analog circuitry is more affected by noise than the same technology that implements a digital only application. The difference derives from the inherent sensitivity of the analog signals to noise. Therefore, by knowing the application and the noise behavior of each technology, the appropriate technology for that application can be chosen to minimize the effects of SCN. Practically, the cost of the technology and the availability and maturity of a process also limit the possible options. Thorough analyses are performed to characterize and improve the noise behavior of a specific technology. These solutions encompass technological (process adjustments, such as doping variations, annealing temperatures variations), circuit, physical (layout), operating conditions (such as operating temperature), circuit signal conditioning (such as turning on and off digital blocks during the noise generation), signal and power routing aspects, and block placement.

2.4 Substrate Coupling Noise Waveforms

A number of articles in the literature [69–73] have reported experimentally observed noise waveforms caused by the switching of digital logic blocks. These waveforms have been compared with simulations results using MEDICI [74]. A typical noise waveform, both experimentally observed and simulated, is shown in Fig. 2.5, while the typical device structure including the noise source, the transmission medium, and the noise receptor is shown in Fig. 2.6.

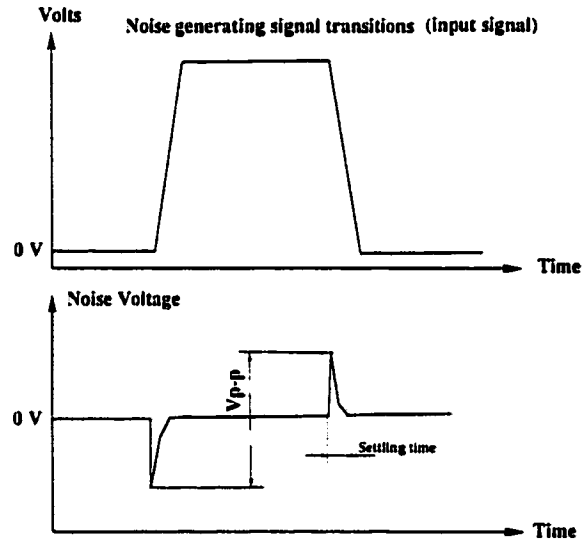


Figure 2.5: A typical noise waveform caused by digital switching: a) the noise generating transitions of the digital signal and b) the output of a current source, affected by substrate noise

Note the analogy between Fig. 2.6 and Fig. 2.1 for substrate noise, where the *noise source* is the *noise generating transistor*, the *transmission medium* is the *common substrate*, and the *noise receptor* is the *sensitive transistor*. Wooley, Rubio, and Masui [69–71] reported a positive and negative transitioning noise spike generated during the signal switching, as shown in Fig. 2.5. In the experiments described in [69–73], the noise source is digital and the noise receptor is analog, consisting of a current source.

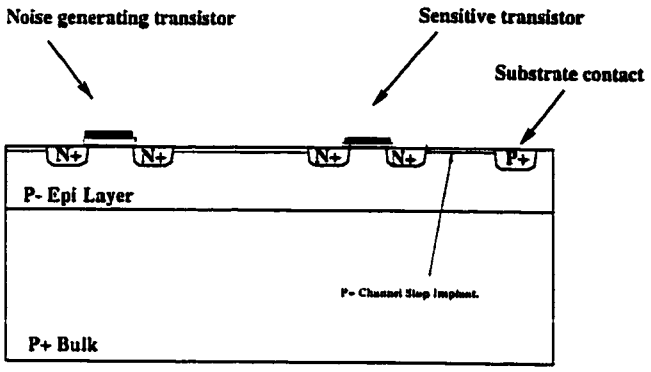


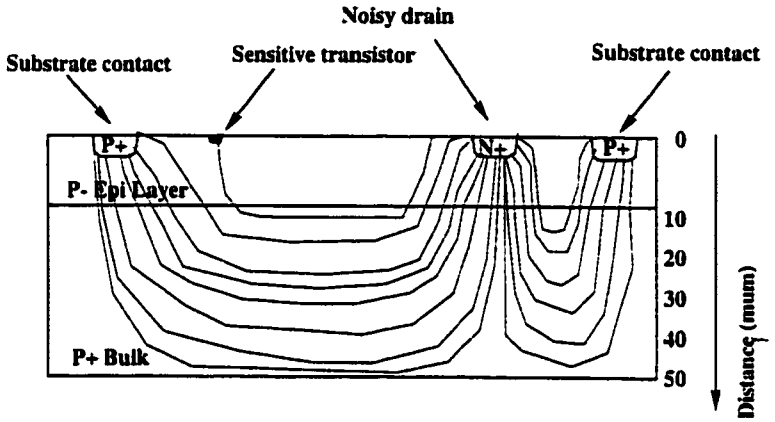
Figure 2.6: The typical device environment for substrate coupling noise interaction.

The observed noise waveform at the output of the current source (see Fig. 2.5) is caused by the negative (positive) voltage transients from the substrate generated by the switching of the digital signals [69, 71, 72]. These transient signals increase (decrease) the threshold voltage V_T of the current source MOS transistor through the body effect, thereby decreasing (increasing) the current flow in the current source and inducing a positive (negative) spike in the output voltage V_{out} of the current source, creating a peak voltage V_{pp} as illustrated in Fig. 2.5. The noise waveform in Fig. 2.5 is observed for both a *highly doped substrate* case and a *lightly doped substrate* case. The peak-to-peak measured noise voltage V_{p-p} depends on a wide range of technological and design aspects, as is discussed in the following sections.

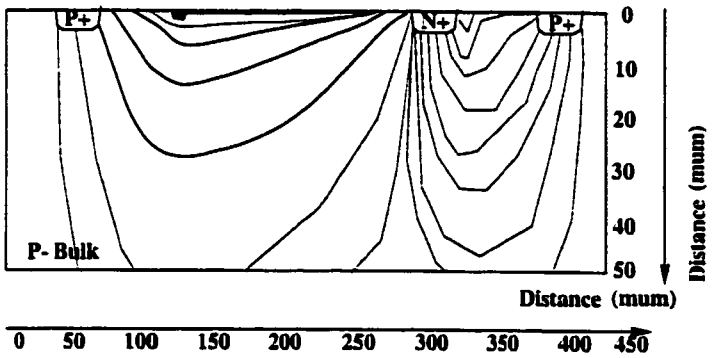
2.5 The trajectory of the noise signal through the substrate

As mentioned in Section 2.3 and Chapter 1, SCN has been seriously investigated for the *highly doped substrate* case and the *lightly doped substrate* case

and for *digital influencing analog* applications. The current flow lines for a *highly doped substrate* and a *lightly doped substrate* [69] are shown in Fig. 2.7. The reported current flow lines are obtained by simulations using PISCES-IIB [69, 75]. Intuitively, the waveforms shown in Fig. 2.7 can be explained by the fact that the substrate current transients propagate towards the path with the lowest substrate resistivity.



a) The substrate current flow for a highly doped substrate



b) The substrate current flow for a lightly doped substrate

Figure 2.7: The current flow lines for a lightly and highly doped substrate. All distances are in micrometers.

For a *highly doped substrate*, the substrate current crowds towards the low resistivity bulk and propagates towards the sensitive transistors and substrate contacts through the low resistivity bulk. The maximum amount of noise is propagated at the interface between the epi layer and the bulk (see Fig. 2.7a) and through the bulk, since that path is the lowest resistivity path. For a *lightly doped substrate*, the lowest resistivity path is at the surface of the substrate. Therefore, as shown in Fig. 2.7b, the substrate current crowds towards the surface, and is less present towards the back of the substrate within the volume of the substrate. This current flow behavior depends upon the substrate type (*i.e.*, the technology) and has important consequences on the nature of the transmitted noise towards the noise sensitive circuitry, as is discussed in the following sections.

2.6 Substrate modeling

In order to simulate the effect of SCN, the common circuit substrate must be properly modeled [76]. Several modeling techniques have been employed, achieving different levels of precision. The substrate has been modeled as a 2-D and 3-D mesh of resistors or *R mesh* [77–79], and as a mesh of parallel resistors and capacitors or *RC mesh* [80–83]. The *RC mesh* model is shown in Fig. 2.8. For each drain, source, or transistor, a node, which represents the location where the noise is generated or received within the substrate, is introduced in the model. Each node interacts with every other global or neighboring node. The computational complexity of the model increases exponentially with circuit size. Different approaches to model the substrate have been developed for large circuits [78] due to this trade-off between computational speed and model accuracy. A modeling methodology that achieves reasonably high accuracy and fast computational

speeds is the *noise signature* method [84]. This method uses accurate local substrate models to obtain high accuracy, while the computational complexity is reduced by dividing the circuit into blocks and determining the *noise signature* for each block. The substrate noise of the entire circuit at a macro level is determined by analyzing the interaction between the *noise signatures* of each of the blocks. The noise for one block is a sum of the *noise signatures* influences coming from all of the other blocks. A similar approach involves partial substrate modeling [85].

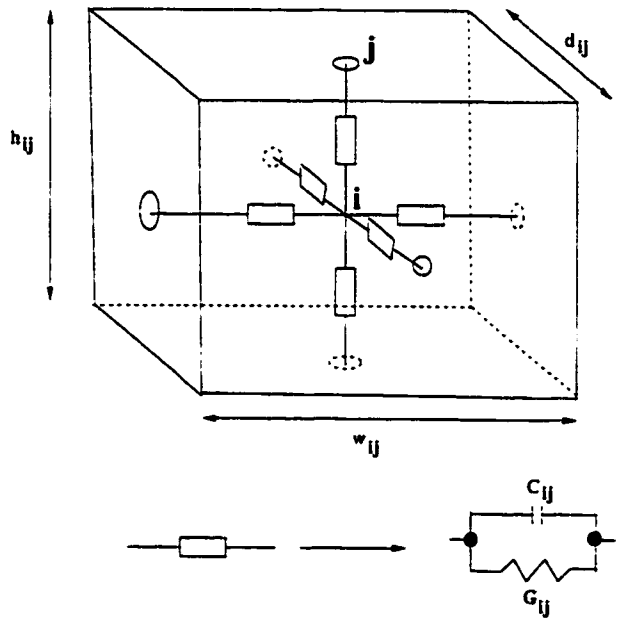


Figure 2.8: Spatial discretization of the substrate using Maxwell's equations.

The basic principles of substrate modeling [81] are based on the notion that outside the diffusion/active areas the substrate can be approximated as layers of uniformly doped semiconductor of varying doping density. In the following analysis, the starting point is Maxwell's equations in differential form [86–88],

$$\vec{\nabla} \cdot \vec{D} = \rho, \tag{2.1}$$

$$\vec{\nabla} \cdot \vec{\mathrm{B}} = 0, \tag{2.2}$$

$$\vec{\nabla} \times \vec{\mathrm{E}} = -\frac{\mathrm{d}\vec{\mathrm{B}}}{\mathrm{d}t}, \tag{2.3}$$

and

$$\vec{\nabla} \times \vec{\mathrm{H}} = \mathrm{J} + \frac{\mathrm{d}\vec{\mathrm{D}}}{\mathrm{d}t}, \tag{2.4}$$

where E is the *electric field*, D is the *electric flux density*, H is the *magnetic field intensity*, B is the *magnetic field density*, J is the *current density*, and ρ is the *charge density*.

Ignoring the magnetic fields and using the identity,

$$\vec{\nabla} \cdot (\vec{\nabla} \times \mathrm{a}) = 0, \tag{2.5}$$

(2.4) can be written as

$$\vec{\nabla} \cdot \vec{J} + \vec{\nabla} \cdot \frac{\mathrm{d}\vec{D}}{\mathrm{d}t} = 0. \tag{2.6}$$

Using the material constants ϵ (permitivity) and σ (conductivity)

$$\vec{D} = \epsilon \vec{E} \tag{2.7}$$

and

$$\vec{J} = \sigma \vec{E}, \tag{2.8}$$

(2.6) becomes

$$\sigma \vec{\nabla} \cdot \vec{E} + \epsilon \frac{\mathrm{d}}{\mathrm{d}t}(\vec{\nabla} \cdot \vec{E}) = 0. \tag{2.9}$$

Modeling the substrate as a three-dimensional *RC mesh* (see Fig. 2.8) with the primitive element box sizes of width w_{ij}, length d_{ij}, and height h_{ij}, and applying a box integration strategy [89], the following expression is obtained,

$$\Sigma[G_{ij}(V_i - V_j) + C_{ij}(\frac{\delta}{\delta t}V_i - \frac{\delta}{\delta t}V_j)] = 0, \tag{2.10}$$

where

$$G_{ij} = \sigma(\frac{w_{ij}d_{ij}}{h_{ij}}), \tag{2.11}$$

and

$$C_{ij} = \epsilon(\frac{w_{ij}d_{ij}}{h_{ij}}). \tag{2.12}$$

The complexity problems in substrate modeling result from the number of boxes that are considered (the number of primitive elements), and from the circuit size, since, as discussed above, for each drain, source, or transistor, a node, which represents a noise generating or receiving point must be introduced in the model.

2.7 Quantitative aspects in substrate coupling noise

SCN is currently being studied for a narrow range of applications, namely for A/D and D/A converters as well as those applications that contain on-chip digital logic blocks and high precision analog signal processing. In these applications, the digital circuitry influences the high precision analog circuitry. The semiconductor technologies employed to implement these applications are referred to as the *lightly doped case* and the *highly doped case*, as mentioned in Sections 2.3, 2.4, and 2.5. The principal results of the experimental work and analysis of SCN that has

previously been reported in the literature, for both the *lightly doped case* and the *highly doped case*, are reviewed in this section. Many of the results reviewed here, even if obtained for a *digital influencing analog* type of application, can be extended, at least in principle, to other types of applications, such as a smart-power application.

The following issues that influences the peak-to-peak measured noise V_{p-p} as depicted in Fig. 2.5 depend on a wide range of technological and design aspects such as the

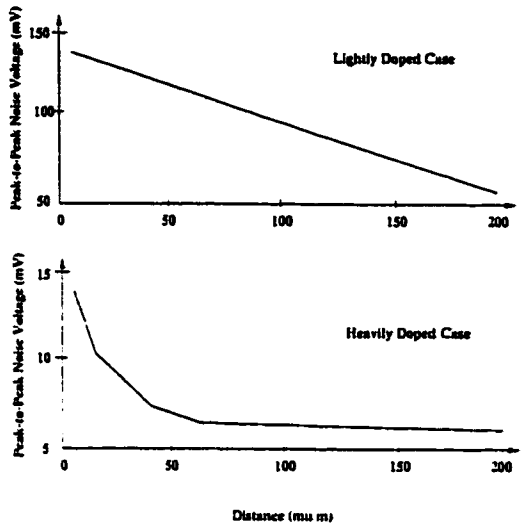
- Substrate doping
- Distance between the noise source and noise receiver
- Noise reduction techniques (rings, substrate contacts, etc.)
- Substrate (epitaxial layer) thickness
- Backplane substrate contact
- Substrate contact placement
- Switching speed and transition times
- Interaction between different types of transistors
- Noise source supply voltage
- Logic circuit size
- Power (high current) line routing
- Other issues

Each of these aspects is briefly reviewed, demonstrating how each of these aspects influence the generation, transmission, and reception of substrate noise.

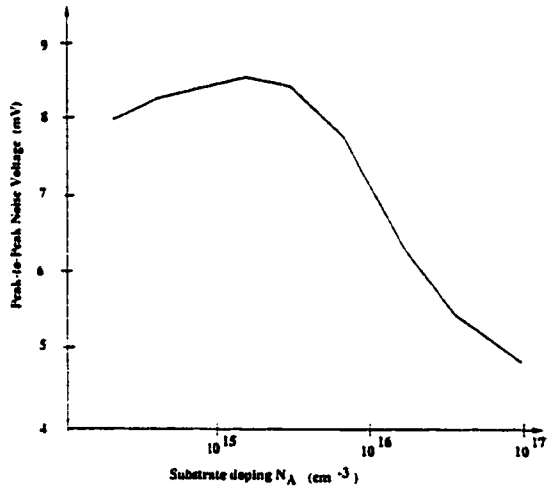
2.7.1 Influence of Substrate Doping and Distance between the Noise Source and the Noise Receptor

It is shown in [69, 70] (see Fig. 2.9a) that for the *heavily doped substrate* case, if two substrate contacts are separated by more than four times the effective thickness of the epitaxial layer, the resistance between the contacts is independent of the separation, and the heavily doped bulk can be regarded as a single node. This characterization implies that any noise injected through the epitaxial layer into the bulk will spread through the entire substrate. Accordingly, the peak-to-peak noise amplitude V_{p-p} is independent of the distance between the noise source and the noise receptor. In the lightly doped case, the peak-to-peak noise voltage decreases almost linearly with the separation distance. However, it has also been seen that lightly doped substrates may produce latch-up [63, 64, 90]. Note that in comparing the lightly doped case to the heavily doped case (see Fig. 2.9a), a 30% reduction in noise is achieved in only a 60 μm spacing for the heavily doped case, as compared to a 200 μm spacing for the lightly doped case. Accordingly, if the sensitive circuitry is less than 200 μm apart from the noise source, a heavily doped case is preferred. A lightly doped case is preferred for large distances between the noise source and the noise receptor.

As also shown in [70] and illustrated in Fig. 2.9b, the peak-to-peak noise voltage strongly decreases with increasing substrate doping level in a non-epitaxial process. The doping levels increase in the new generations of scaled down technologies, a beneficial aspect when minimizing SCN.



a) The peak-to-peak noise as a function of distance between the digital noise source and the current source.



b) The peak-to-peak noise as a function of substrate doping level

Figure 2.9: Noise dependency on distance [69] and substrate doping [70]

2.7.2 Noise Reduction Techniques

Several noise reduction techniques [69–71, 91] have become standard such as

- Substrate contacts
- N+ and P+ rings
- Buried layer
- Wells

The results illustrated in Fig. 2.10 have been reported in [70]. Similar results for some of the issues studied in [70] are described in [69, 71, 91]. The experimentally determined peak-to-peak noise voltage shown in Fig. 2.10 for the different noise reduction techniques depend on the specific technological and design issues, as discussed in this chapter. The noise reduction efficiency of these techniques relative to one another is summarized in Fig. 2.10 and reported in [69–71, 91].

The buried layer is a particular case of a backside substrate contact (see Section 2.7.4). If N+ and P+ rings are used, the wider the rings, the larger the noise reduction [70]. In [69], a 99 μm wide ring is used (however, a proper ring size depends on issues such as substrate doping, technology featured size, etc). It is shown in [69] that the effectiveness of the guard rings increases if the rings are biased through a dedicated pin. If the ring is connected to a large substrate contact, and both the ring and the substrate contact are connected to the same pad, results in an increase in noise. The ring must be placed as close as possible to the sensitive circuitry in order to increase the protection of the sensitive circuitry.

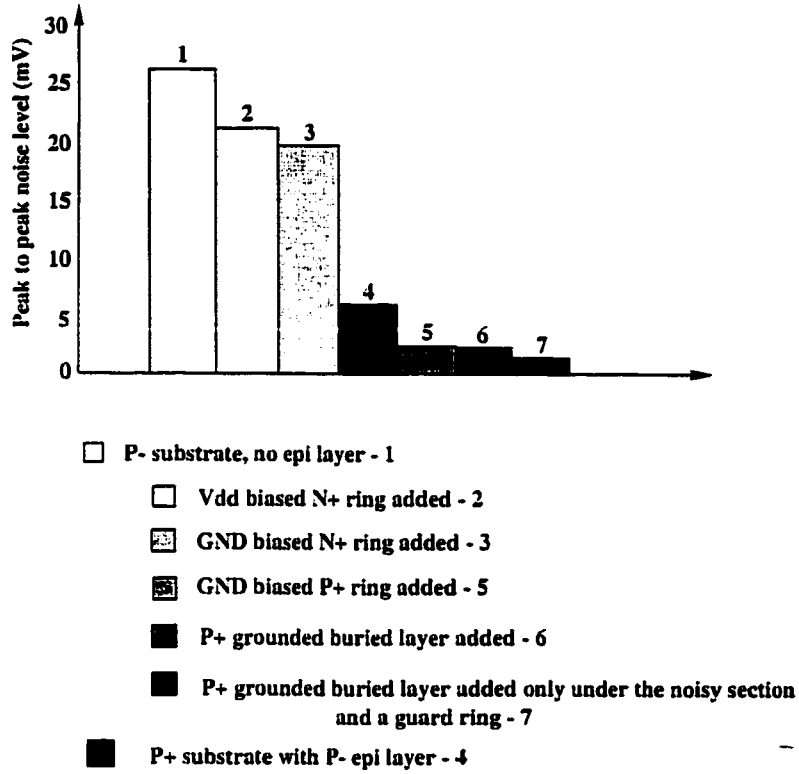


Figure 2.10: Comparison of noise reduction techniques

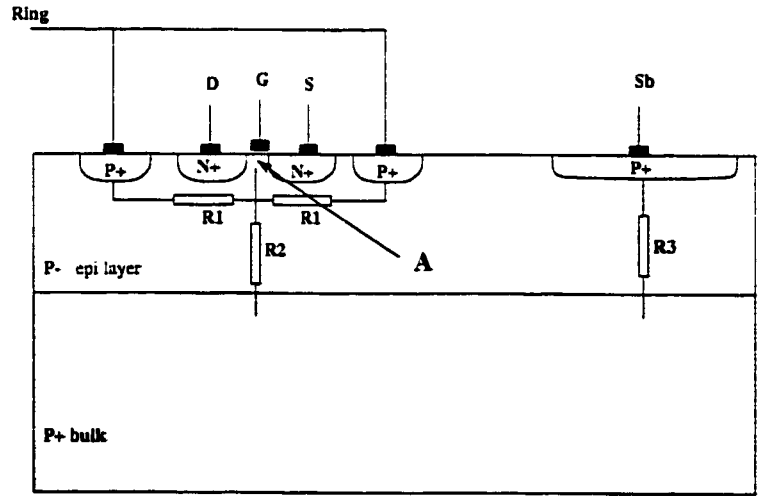


Figure 2.11: The effectiveness of guard rings depends on the resistive paths and connections

These issues can be better explained by referring to Fig. 2.11. To decouple node A, R1 must be smaller than R2 (the guard ring should be as close as possible to the sensitive circuitry). If the ring is connected to the large substrate contact, node A receives the substrate noise through R3 (smaller than R2 due to the substrate contact size) and the metal layer between the guard ring and the substrate contact, increasing the observed noise.

The P+ guard rings are highly efficient for a *lightly doped substrate*, and are far less efficient for a *highly doped substrate* [69, 71]. This behavior is due to the fact that (see Fig. 2.11 and Fig. 2.7) the substrate current lines are attracted towards the ring, propagating along the substrate surface through a small R1, while R2 and R3 are large for a *lightly doped substrate*. For a *highly doped substrate*, R2 and R3 are comparable to R1 and the efficiency of the ring is diminished. As shown in Fig. 2.7, the current lines propagate in all directions. The use of wells to break the channel stop implant has a small effect as shown by the current flow lines depicted in Fig. 2.7. The peak-to-peak noise voltage decreases a great deal [69] if multiple pins are used to bias large substrate contacts due to inductive effects (see Section 2.7.11). As described, a *highly doped substrate* has up to one order of magnitude improved noise behavior than a *lightly doped substrate* for small distances between the noise source and the noise receptor. However, for a *lightly doped substrate*, the noise decreases with distance.

2.7.3 Substrate (Epitaxial Layer) Thickness

The influence of the substrate thickness with respect to the received noise is studied in [70] for the *lightly doped substrate* case. These results can be partially extrapolated to a *highly doped substrate* case by considering the bulk with zero

resistance. It has been reported [70] that the noise increases almost linearly with substrate thickness for thicknesses up to $\approx 80\,\mu$m, after which the magnitude of the noise saturates (see Fig. 2.12).

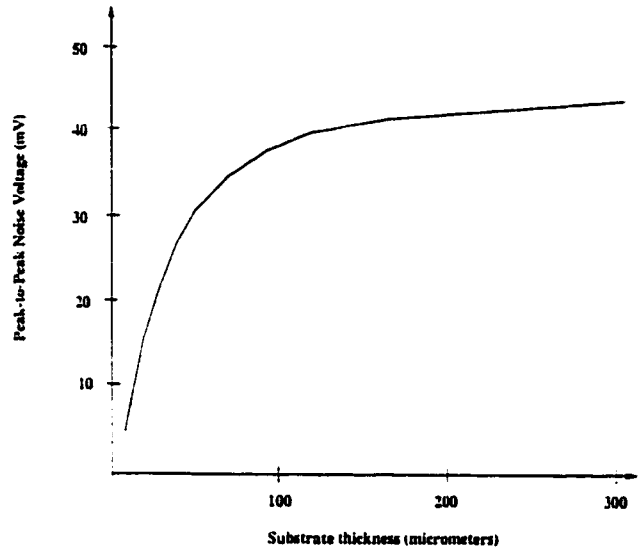


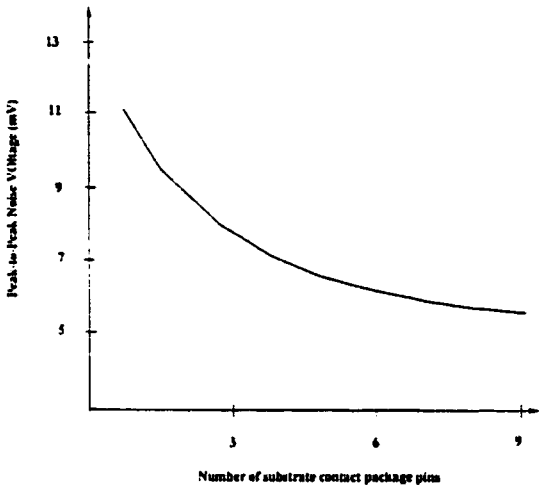
Figure 2.12: Dependency of noise on substrate thickness.

2.7.4 Backplane Substrate Contact

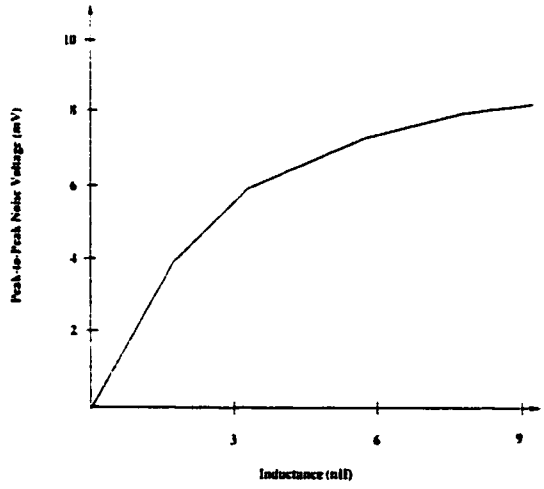
A backplane bias has been shown to reduce SCN in both the *lightly doped substrate* case [70, 72, 91] and the *highly doped substrate* [69, 71, 91] case. The buried layer technique [70] (Section 2.7.2) is a particular case of the backplane substrate contact, and is particularly beneficial for the noise behavior since it reduces the substrate thickness (Section 2.7.3) to epitaxial layer thickness if the buried layer is placed at the interface of the epi layer and the bulk.

For a *lightly doped substrate*, the backplane contact acts as a highly doped substrate bulk (Section 2.7.1), saturating the noise with distance [72]. As shown in Figs. 2.13a and 2.13b, for a *highly doped substrate*, a backside contact effectively

reduces SCN, provided that the package provides a low inductance path between ground and the backside contact, thereby reducing $L\ di/dt$ noise [69, 71]. With an efficient backside contact, the P+ guard rings provide little benefit since the switching-induced current is supplied from the backside contact.



a) Peak-to-peak noise voltage as a function of the number of substrate contact package pins



b) Peak-to-peak noise voltage as a function of the inductance used to bias a backside substrate contact

Figure 2.13: Dependency of noise on the substrate (backplane) contact inductance and on the number of substrate contact package pins

The variation of the peak-to-peak noise voltage with the backside substrate contact inductance is shown in Fig. 2.13b. Zero inductance provides virtually zero noise, increasing to $\approx$ 8 mV for 9 nH [69, 71]. As the inductance increases, an increasingly larger ringing is observed on the noise waveforms. Multiple package pins for the backside contact is beneficial, reducing the inductance [69].

2.7.5 Placement of the Substrate Contacts

The placement of the substrate contacts influences the current flow lines as shown in Fig. 2.7. Poor placement of the substrate contacts can actually direct the noise towards the sensitive circuitry.

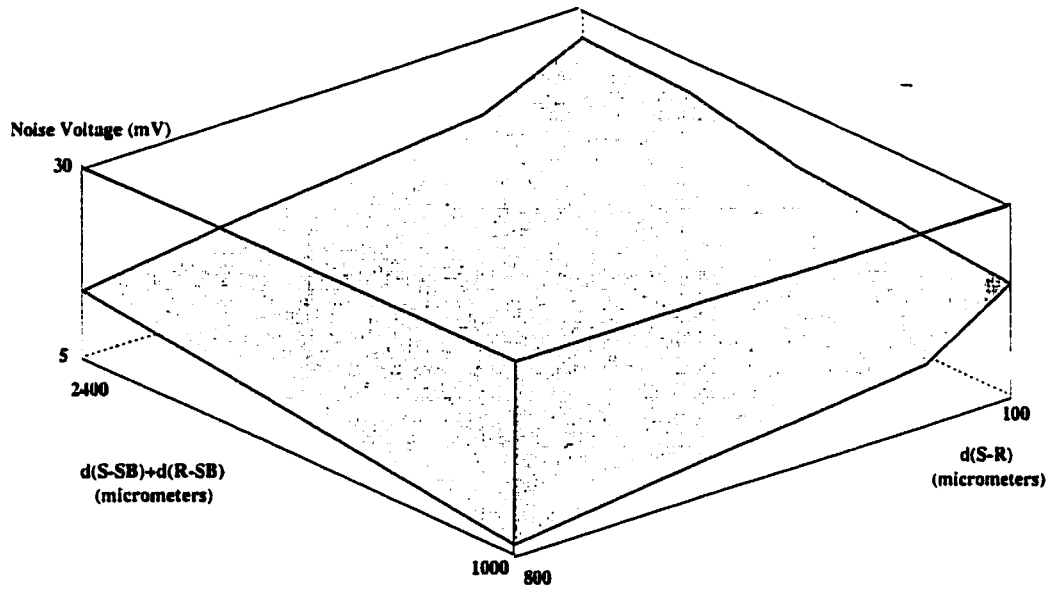


Figure 2.14: Dependency of noise on the placement of the substrate contacts

The analysis of the placement of the substrate contacts has been performed in [72] for the *lightly doped substrate* case. The discussion is based on the existence of three dominant resistances: between the noise source (S), the noise receptor (R),

and the substrate contacts or backside contact (SB), R_{S-R}, R_{S-SB}, and R_{R-SB}. Each of these resistances depend on the corresponding distances, d_{S-R}, d_{S-SB}, and d_{R-SB}. It is shown that the noise decreases as d_{S-R} increases and as $d_{S-SB}+d_{R-SB}$ decreases (Fig. 2.14). Accordingly, poor substrate contact placement can increase the noise, even if the other factors that influence the noise are chosen carefully.

2.7.6 The Influence of Switching Speed and Transition Times on Noise

The *heavily doped substrate* case is analyzed in [69]. An equation characterizing the voltage of the bulk node as a function of the switching transients is

$$\frac{V_{BULK}(s)}{V_{TRANS}(s)} = \frac{C_C}{C_C + C_S} \frac{s(s + \frac{R_S}{L_S})}{s^2 + \frac{R_S}{L_S}s + \frac{1}{L_S(C_C+C_S)}}. \qquad (2.13)$$

This equation provides a substrate resonance frequency (SRF) as a function of the technology characteristic resistances, inductances, and capacitances (R_S, L_S, C_S, C_C) [69],

$$SRF = \sqrt{\frac{1}{L_S(C_S + C_C)} - \frac{R_S^2}{L_S^2}}. \qquad (2.14)$$

C_C models the diffusion and interconnect capacitances coupling the switching noise sources to the substrate, C_S models the capacitances from different nodes, pads, and junctions of the circuit to the substrate, R_S models the spreading resistances through the epitaxial layer, and L_S models the bonding wire inductance. SRF is the resonance frequency of the substrate response described by (2.13). The switching clock frequencies and low order harmonics must not coincide with the SRF in order to provide good noise immunity with respect to the operating frequency of the circuit. Since the SRF depends upon technology factors which

are difficult to adjust (R_S, C_S, C_C), the noise can be reduced by controlling the characteristic inductance (L_S) through efficient packaging.

For a *lightly doped substrate* case, it is shown in [72] that by decreasing the frequency, the noise is reduced and the noise ringing is significantly decreased. It is shown in [70] that the noise increases by four orders of magnitude (0.1 mV to 1 V) when the transition times decrease over four orders of magnitude, from 10 ns to 1 ps (see Fig. 2.15).

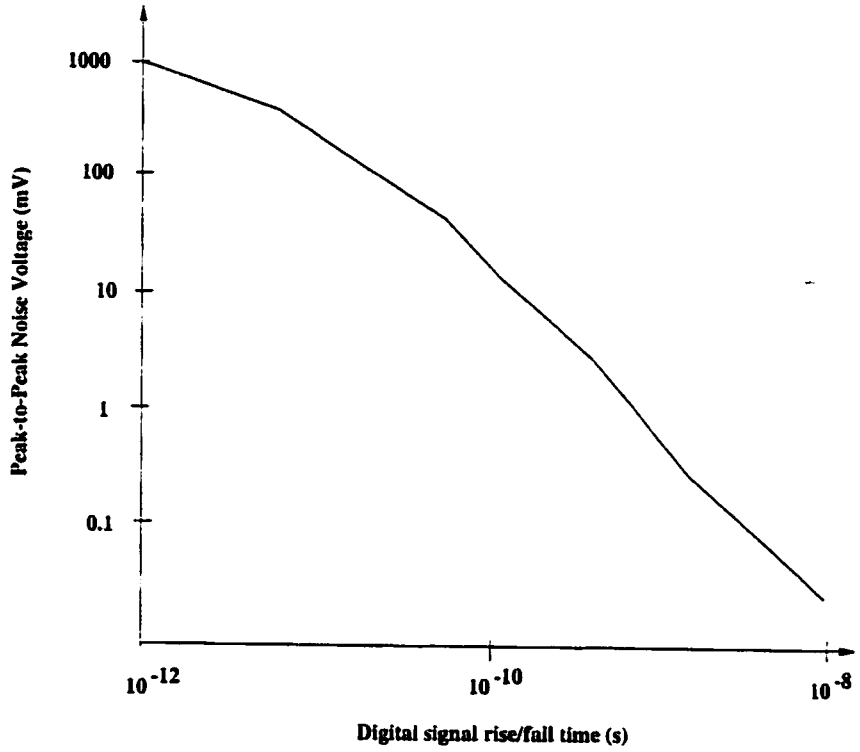


Figure 2.15: Dependency of noise on the digital signal transition times

2.7.7 Interactions Between Different Types of Transistors

For a typical CMOS N-well technology, the noise interaction between different combinations of NMOS and PMOS transistors based on MEDICI simulations has

been reported in [70]. In this analysis, independent of the transistor type, the noise source and the noise receptor consist of a transistor with a resistive load (an inverter with resistive load for the noise source and a current source for the noise receptor). These results are listed in Table 2.1.

Table 2.1: The noise levels quantifying the interaction between different types of transistors in a CMOS N-well process

Noise source	Noise receptor	Noise level (mV)
NMOS	NMOS	7.1
NMOS	PMOS	4
PMOS	PMOS	2.6
PMOS	NMOS	1.4

Experimental tests to confirm these MEDICI simulations have been performed in [70]. A discrepancy between the simulated and experimentally obtained results has been noted in [70]. The NMOS-to-NMOS and PMOS-to-PMOS interactions have a similar noise level in the experimental measurements, in contrast to the results derived from the MEDICI simulations (see Table 2.1). Also, the experiments show that if the distance between the noise source and the noise receptor is small, the noise received by the noise receptor, if it is parallel to the noise source, is about four times larger than if the noise source and the noise receptor are orthogonal.

2.7.8 The Influence of the Supply Voltage of the Noise Source

An analysis of the generated noise for different supply voltages of the noise source has not been reported in the literature. In the reported work, the noise source is digital and the power supply is typically 5 volts. However, in [72], noise levels for two different logic supply voltages of the digital noise source are men-

tioned. The experimental results shown in [72] include the effect of the variation of the power supply and the operating frequency (see Section 2.7.6). Accordingly, a complete description of the effect of the power supply voltage variation on noise has not been described within the literature. However, for the two combined effects, the noise level is shown to decrease when the power supply and the frequency decrease [72].

2.7.9 Logic Circuit Size

It is experimentally shown [73] for a 0.8 μm CMOS process that the amplitude of the noise measured in the analog portion of the circuit depends upon the number of activated logic gates. From the figures reported in [73], the peak-to-peak noise voltage level is approximately 40% higher when 7.4K gates are active as compared to when 3.9K gates are active.

2.7.10 Routing of Power (High Current) Distribution

Routing the power lines in a mixed-signal environment is a very delicate problem. The position and number of the power pins are important issues. Some of these aspects are discussed in Sections 2.7.2, 2.7.4, 2.7.5, and 2.7.11. An optimization problem for the power lines distribution is formulated in [91]. Some experimental rules for choosing a power distribution grid are given in [92]. For example, Olmstead and Vulih recommend in a *digital influencing analog* application to

- Have the V_{DD} bus serving the digital portions of the chip short and with a low impedance.

- Use extreme care in locating the substrate tie downs to keep the digital noise from entering the substrate.

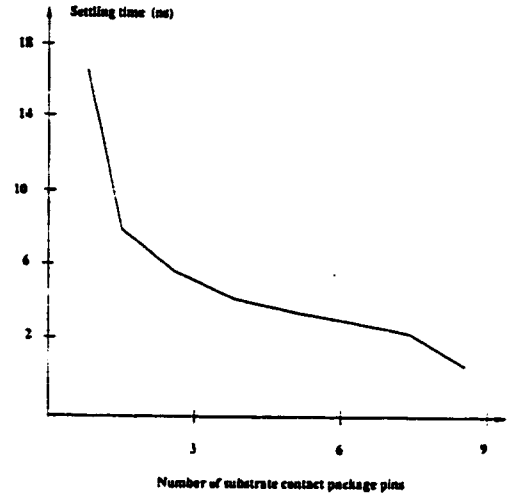
- Substrate tie downs from the sensitive busses should be eliminated in order to keep substrate noise from entering the analog V_{DD} busses.

2.7.11 Other issues influencing the generation, transmission, and reception of substrate noise

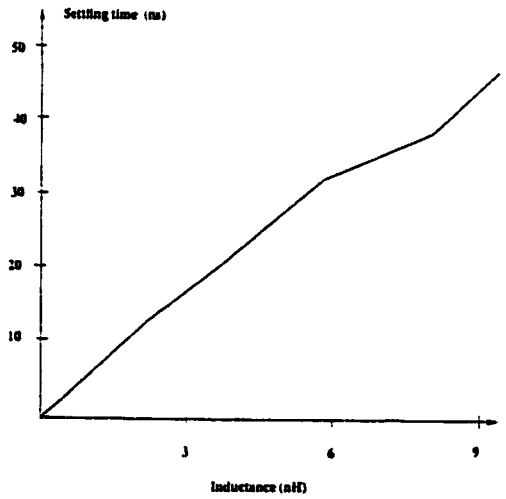
The inductance of the bonding wires greatly affects the noise behavior [69, 71, 91], especially for those wires connected to the backside contact, substrate contacts, or power/ground lines (see Sections 2.7.2, 2.7.4, 2.7.5). It is shown in [71] that the inductance on a V_{DD} line produces a ringing on the noise waveform with a frequency close to $1/2\pi\sqrt[3]{LC}$ where L is the parasitic inductance of the supply line and C is the equivalent n-well capacitance connected to the substrate. The noise amplitude as a function of the package inductance for both *highly* and *lightly doped substrates* using P+ substrate contacts or backside contacts are described in [71]. The higher noise level is obtained for a backside contacted, lightly doped substrate. A dramatic reduction in the noise level when multiple package pins are connected to the power supply (or to the substrate contacts) is reported in [91].

Noise settling time, defined according to Fig. 2.5, is shown to decrease dramatically as the number of package pins connected to the power supply (or to the substrate contacts) increases and as the inductance of the bonding wires decreases [69, 91] (see Fig. 2.16). Typical settling times are 3 ns for eight pins and up to 16 ns for one pin. The settling time is shown to be influenced by the noise reduction techniques [91] (Section 2.7.2). The P+ ring is demonstrated to be preferable for both a *highly doped substrate* (where the settling time is reduced by

a factor of two) and a *lightly doped substrate* (where the settling time is reduced by a factor of four).



a) Settling time to within 0.5 mV as a function of the number of substrate contact package pins.



b) Settling time to within 0.5 mV as a function of the inductance used to bias a backside substrate contact.

Figure 2.16: Settling time of noise as a function of the substrate contact package pins and inductance used to bias a backside substrate contact [69]

The noise received by the sensitive transistor as a function of its orientation with respect to the noise source transistor is studied in [70]. It is shown that if the transistors are transversal (their gates are perpendicular to each other), the

noise is reduced by a factor of two as compared to when the transistors are in parallel. It is also shown that if the source of the sensitive transistor is physically closer to the noise source, the noise is decreased by a factor of four as compared to when the drain is physically closer to the noise source.

The relative on-chip placement of the digital logic blocks (*i.e.*, the noise source) and the analog circuit blocks (*i.e.*, the noise receptor) greatly influences the noise received by the sensitive analog blocks (see Sections 2.7.1, 2.7.2, 2.7.5, 2.7.7, 2.7.9, and 2.7.10). The effect of the placement of the digital blocks to reduce the noise received by the analog blocks has been studied in [93].

On-chip inductors present in applications such as wireless communications can generate noise within the substrate [94]. This noise is generated due to issues such as magnetic effects and field propagation.

2.8 Highlights of the present work

The research discussed in this proposal focuses on the analysis of SCN when both high power analog circuitry and digital control circuitry are integrated on the same monolithic substrate, specifically for mixed-signal *Smart-Power* circuits. For reliable monolithic Smart-Power applications, problems such as SCN must be fully understood, modeled, and compensated. The cost of the final product, implying the process complexity, is also an important factor. Accordingly, solutions to control SCN in a low cost monolithic process are highly desirable, thereby eliminating expensive hybrid or high performance smart-power processes.

Substrate coupling noise in NMOS and CMOS smart-power circuits are investigated in this research project. These technologies have been chosen primarily for reasons of low cost, technological maturity, reliability, and availability rather than

for suitability for Smart-Power circuits. The primary focus of this research effort is to investigate the fundamental influences of substrate coupling noise on NMOS and CMOS mixed-signal smart-power circuits, and to determine design techniques to mitigate substrate coupling noise in these type of circuits and technologies.

Chapter 3

Design and Test of NMOS Mixed-Signal Circuits

An initial step in achieving the principal objective of this research effort, the characterization of the noise behavior of digital circuits for standard low cost technologies for use in smart-power applications, is the analysis of the behavior of digital circuits in an NMOS process. This technology is chosen primarily for cost reasons, availability, certain circuit advantages, and because the analog power blocks are most conveniently implemented in an NMOS technology.

An NMOS process is presently the lowest cost technology available which offers the advantages of MOS technologies. For the target mixed-signal application, the speed of the logic blocks is not an issue (the maximum required speed is below 1 MHz), and neither is the non-standby power dissipated by the logic blocks since the analog high power drivers dissipate the largest percentage of the total on-chip power. Accordingly, the well known advantages of CMOS do not represent a primary advantage for this smart-power application. A bipolar technology is not justified for this application, first due to the added technological complexity, and also for cost and circuit functionality reasons. An NMOS technology for this application has important advantages such as maturity, low cost (the lowest

number of masks), circuit simplicity, low number of transistors, and the analog power blocks are most conveniently implemented in an NMOS process.

A high voltage low cost standard NMOS process [95] is implemented here. The high voltage process uses a low doping substrate and a drift region for the high voltage transistors as shown in Fig. 2.2f. The standard channel length is 5 μm, the substrate thickness is $\approx$ 300μm without a backplane metalization, and the enhancement and depletion transistors have typical threshold voltages of $V_{TE} = 1$ volt and $V_{TD} = -3$ volts.

The test circuits are described and a test strategy is developed in this chapter. The circuit architecture, circuit details, and an overview of the circuit function and layout of the test circuits are discussed in Sections 3.1 and 3.2. The noise that is generated, transmitted, and received depends upon the technology of the application (see Sections 2.3 and 2.5), and on a variety of technology, circuit, and physical design issues (see Section 2.7). The NMOS technology is characterized in Section 3.3 from a noise point of view. The noise issues as presented in Section 2.7 are described in Section 3.3.1 for smart-power applications. Specific noise issues applicable to a smart-power application are described in Section 3.3.2. The test plan for analyzing the fabricated circuits is described in Section 3.4.1. The test set-up and equipment is described in Section 3.4.2.

3.1 Circuit description

Each of the test circuits consist of noise aggressors and noise victims. In these test circuits, a noise aggressor consists of an analog power driver, which is a high voltage, high current transistor, driving a resistor with a typical value of R = 500 Ω (see Fig. 3.1a). The supply voltage for the noise aggressors is 38 volts.

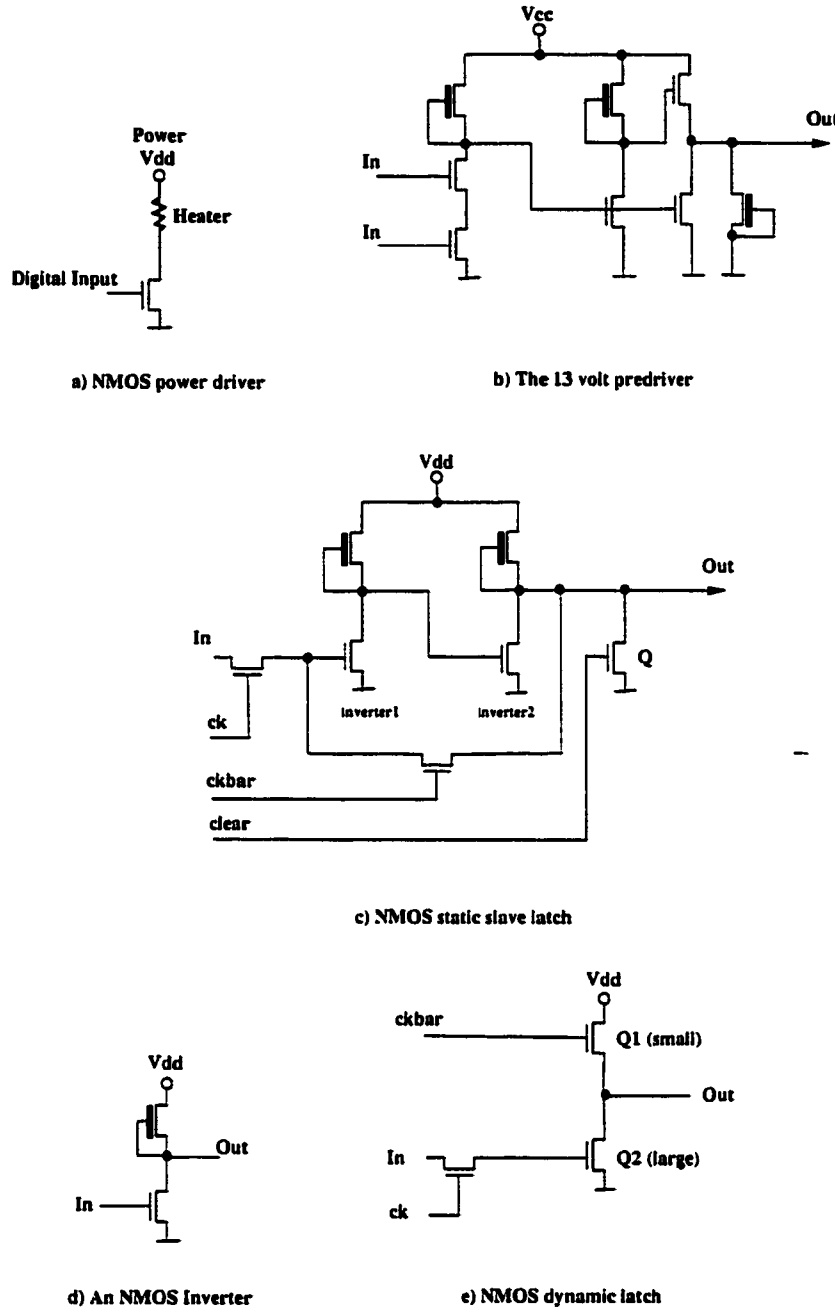


Figure 3.1: Circuit diagrams of the primary NMOS circuits

To efficiently drive this high voltage, high current transistor, a 13 volt predriver (shown in Fig. 3.1b) is used. The predriver receives digital control signals from

5 volt digital logic, consisting of inverters, gates, and static or dynamic latches (Figs. 3.1c, 3.1d, and 3.1e). Eight noise aggressors (or drivers) form a group. Each of the test circuits is composed of one or more such groups. Each driver of a group is individually selected by the 13 volt predriver and the 5 volt logic blocks. The noise victims that receive the substrate noise generated by the noise aggressors typically consist of a chain of serially connected 5 volt static or dynamic latches.

All of the 5 volt logic is typically static enhancement/depletion except the noise victim latches which could be either static enhancement/depletion or dynamic enhancement/enhancement. All latches are grouped in a master-slave configuration. Each static master-slave register can be reset (cleared). The role of the Q transistor of the slave latch, controlled by the clear signal (see Fig. 3.1c), is to return the master-slave register to zero. A block schematic of a test circuit is shown in Fig. 3.2.

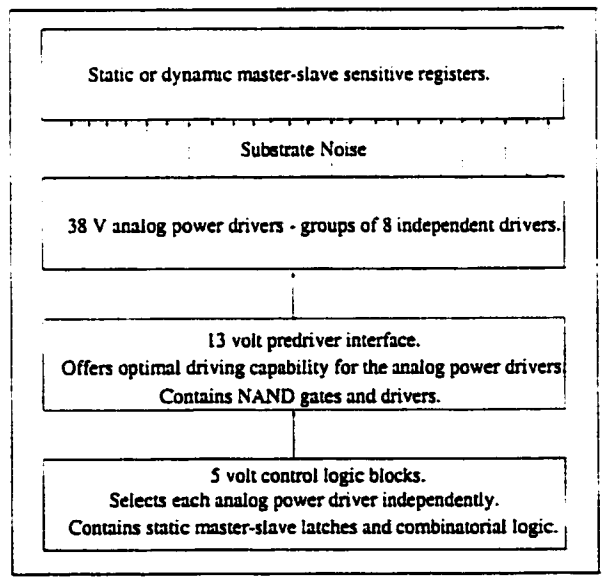
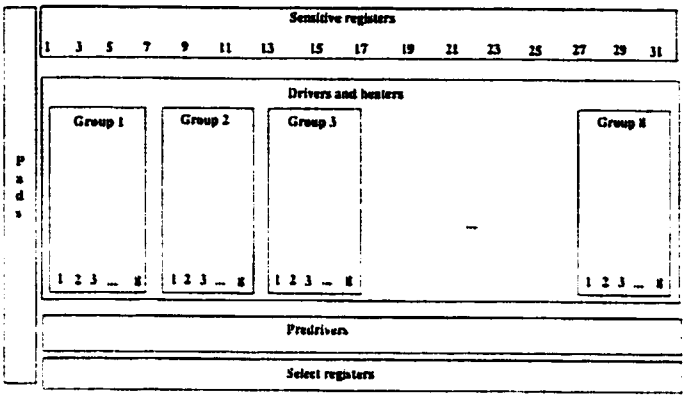


Figure 3.2: A block schematic of a typical NMOS test circuit

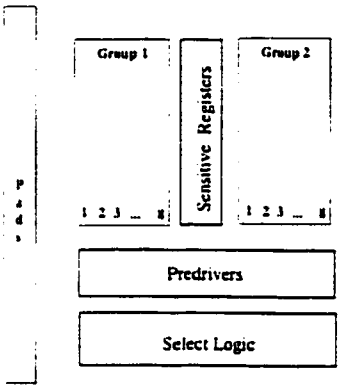
3.2 Overview of physical design issues

As shown in Section 3.3, a number of variables are chosen in order to study the influence of the generation, transmission, and reception noise processes over a digital logic family. These variables determine the number and nature of the test circuits necessary to analyze the substrate noise in NMOS digital circuits in a smart-power application.

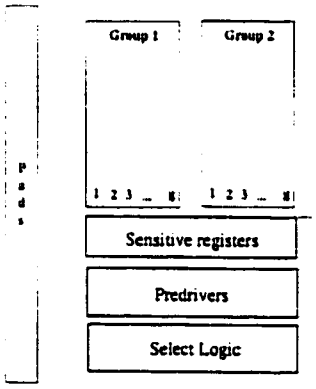
Fifty test circuits have been designed and fabricated in a single metal – single poly 5 μm NMOS process, to cover the principal aspects of substrate noise. The layout of some representative test circuits and circuit blocks are included in Appendix A. Each of the test circuits has 24 I/O pins. There are roughly four major groups of circuits as shown in Fig. 3.3. The first group of circuits as shown in Fig. 3.3a places the sensitive circuits in the upper side of the power drivers. These circuits are called the *upper* circuits. Note that these circuits are composed of eight groups of power drivers. The second group of circuits (see Fig. 3.3b) places the sensitive circuits between two groups of power drivers. The circuits of this group are called the *middle* circuits. The *lower* circuits, forming the third group of test circuits (see Fig. 3.3c), place the sensitive circuits in the lower side of the power drivers. The number of sensitive registers which monitor the substrate noise are: 32 for the upper group, five for the middle group, and nine for the lower group, where the registers are either static or dynamic. While the first three groups of circuits monitor the effects of noise on the static and dynamic registers, the fourth group (see Fig. 3.3d) is designed to measure the substrate noise voltage at different points of the substrate. Using the fourth group, the magnitude and characteristics of the substrate noise can be correlated with the victim static and dynamic registers.



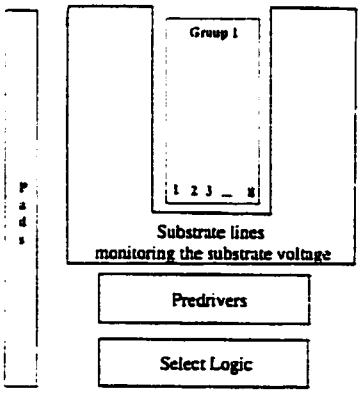
a) The floorplan of the upper circuits



b) The floorplan of the middle circuits



c) The floorplan of the lower circuits



d) The floorplan of the substrate voltage monitoring circuits.

Figure 3.3: The floorplan of the four major groups of test circuits

For the fourth group, since the substrate voltage levels are considerable (see Chapter 4) and high precision is not necessary, a rather simplistic approach to measure the substrate noise levels and the characteristic waveforms is applied. 14 metal lines connected to the substrate surround a group of eight drivers, each one of the lines having a dedicated pad to access the substrate voltage on that line. Accordingly, the noise distribution generated through the substrate by the switching of the drivers can be determined. The noise difference among different substrate points can also be determined. Each one of the eight drivers can be individually selected so that up to all eight drivers can be selected at a given time in order to vary the noise magnitude. For the circuits in this group, each of the eight drivers is $\approx 35\%$ the size of the drivers used in the first three groups.

3.3 Noise characterization of the test circuits

The sensitivity to noise of a logic family depends upon the amount of noise that is generated by the power drivers, transmitted through the substrate, and received by the logic circuits. The amount of noise that is generated depends primarily on certain design aspects of the power device (*i.e.*, the power driver). Issues such as the placement of the device substrate tiedowns, the placement of the substrate contacts, the shape of the polysilicon gate, and the device layout, influences the amount of noise that is generated by the power driver. For this analysis, a power device with a drain drift N- region (see Section 2.3.3) and self-isolation technique (see Section 2.3.7) is implemented. Four large width ($\approx 940\,\mu$m) transistors, connected in parallel, are used for the upper, middle, and lower groups to create one large driver. Two large width ($\approx 530\,\mu$m) transistors are used to create one large driver for the fourth group to determine the distribution of the substrate

voltage. In each case, the drain is symmetrically surrounded by the gate and source regions, as required by the self-isolation technique.

The transmitted and received noise depends upon a variety of issues such as those discussed in Chapter 2. In this section, the transmitted and received noise for the NMOS technology is qualitatively characterized according to the issues described in Chapter 2. Each of the issues which might influence the transmitted and received noise without changing the technological process is considered in the present analysis as a variable to be analyzed in the test circuits. Additional issues believed to influence the noise behavior of the digital circuits in a smart-power environment are considered in this analysis, and treated as variables in the test circuits. All of these variables determine the proper number of test circuits. The objective in analyzing these issues is to determine the effect of the noise present at a specific point within the substrate and the effect on the logic circuits of the distribution of the noise through the substrate.

3.3.1 Classic noise issues in smart-power circuits

A multitude of aspects which influence the generation, transmission, and reception of noise in a *digital influencing analog* type of application have been discussed in Chapter 2. The goal of this section is to determine which of these aspects are applicable to a smart-power application.

The target high voltage NMOS technology [95] can be characterized as a *lightly doped substrate* case (see Section 2.5). The technology is low cost and has not been optimized specifically for smart-power applications (see Sections 2.3.7 and 2.3.9).

- **Distance** For the *lightly doped substrate* case, the transmitted noise decreases linearly with increasing distance between the noise source and the noise receptor (as shown in Fig. 2.9a).

  Since a group of eight power drivers covers an area of approximately 700 x 1000 μm, and one test circuit could have up to eight groups, the distances between the the noise source and the noise receptor could be quite large. Accordingly, the test circuits cover a large distance between a noise source and noise receptor. Vertical distances of 200 μm to 500 μm (see Fig. 3.3a) between the sensitive registers and the power drivers are evaluated for each of the 32 registers. Horizontally, the distance between driver 1 of group 1 and register 32 (see Fig. 3.3a) can reach up to $\approx$ 6500 μm.

- **Substrate doping and thickness** The lightly doped substrate, required in a high voltage process, increases the transmitted noise (see Fig. 2.9b). The doping level is imposed by technological reasons, and therefore can not easily be modified. Increased substrate thickness, according to Fig. 2.12, also increases the noise transmission. Practically, however, a large substrate thickness is necessary due to mechanical support considerations.

- **Noise reduction techniques and placement of the substrate contacts** A multitude of noise reduction techniques have been mentioned in Section 2.7.2. The influence of substrate contacts is analyzed in the present test circuits. For the four major groups of circuits shown in Fig. 3.3, the substrate contacts satisfy the following rules:

  - For the upper, middle, and lower groups, the substrate contacts are placed as shown in Fig. 3.4a.

- For the fourth group, each metal line (see Fig. 3.4b) has substrate contacts that can be grounded or connected to different bias voltages, while the noise is monitored on other lines.
- Each power driver has individual substrate contacts. The power drivers in the fourth group of circuits may or may not have individual substrate contacts.

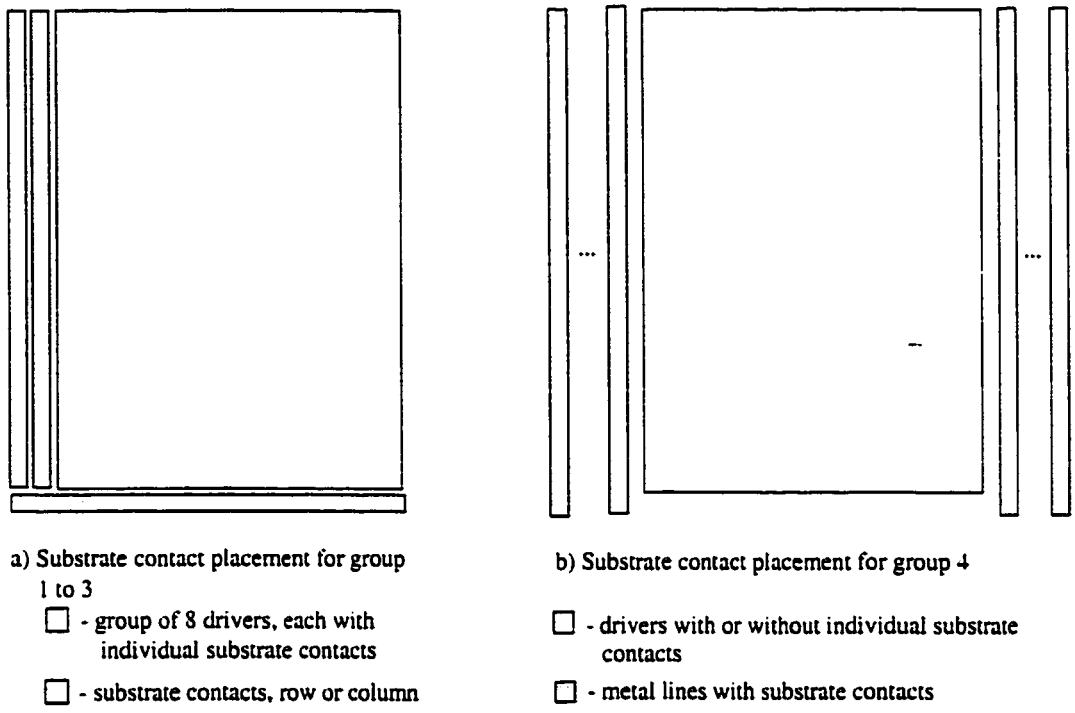


Figure 3.4: The placement of the substrate contacts for the four major circuit groups

- The substrate contacts are P+ and can be used as P+ rings (Section 2.7.2) if the contacts are placed sufficiently dense. The substrate contacts are diffusions of 6 x 12 μm. If the distance between the contacts is, for example, 12 μm, these contacts are sufficiently dense to act as a continuous ring.

Note that there are no substrate contacts between the noise source and the noise receptor for the upper circuits (see Figs. 3.3a and 3.4a). For the middle circuits, there are substrate contacts between the power drivers on the right side and the sensitive circuits (see Figs. 3.3b and 3.4a). For the lower circuits, there are always substrate contacts between the noise source and the noise receptor (see Figs. 3.3c and 3.4a). Customized substrate contacts can be placed for group 4 (see Figs. 3.3d and 3.4b) between the noise source and any of the 14 metal lines on which the noise is observed, since any of these 14 lines can be connected to ground or another bias voltage.

The test circuits contain no other substrate contacts besides the aforementioned contacts. The closest substrate contact for either the sensitive registers, the logic blocks, or the predrivers depends upon the distance between the circuit and any other existing substrate contact, and is determined by the placement of the sensitive register, logic block, or predriver. The presence, number, position, and proximity of the substrate contacts to the digital sensitive circuitry, as discussed above and in Chapter 2, are analyzed.

- **Backplane substrate contact** The test circuits do not employ a backplane substrate contact (see Section 2.7.4).

- **The influence of switching speed and transition times on noise:** The operating frequency in these smart-power circuits is typically 500 KHz with slow transition times. None of the problems discussed in Section 2.7.6 are applicable. As mentioned in Section 3.3, the power drivers have a large width, and accordingly, the polysilicon gates have a significant distributed RC impedance. The consequence of the distributed RC line is that the power driver turn-on and turn-off signal, derived from the predriver, propa-

gates along the line, successively turning on segments of the power driver as shown in Fig. 3.5. Due to this effect, the current may overcrowd at turn-on near the predriver, and may overcrowd at turn-off at the opposite side of the predriver. Besides the increased risk of failure of the power driver, this effect may also cause excessive and nonuniformly distributed substrate noise. To prevent this effect, several solutions may be employed: a special design of the gate layout of the power driver or a predriver that creates slow transition turn-on and turn-off signals for the power driver. Both approaches permit the signal to reach the same voltage level over the entire polysilicon gate. Another solution that employs a process adjustment is the use of a low resistivity doped gate, eliminating the distributed RC characteristic of the polysilicon gate. For the test circuits, the first two solutions are used. The predriver (shown in Fig. 3.1b) achieves adjustable, slow transition signals through transistor sizing. Typically, for a $2\,\mu s$ on-pulse derived from the power driver, an $\approx 5\%$ transition time is sufficient to equalize the signal over the entire polysilicon gate, while not affecting the functionality of the pulse. The crowding effect, which may generate noise nonuniformities or device breakdown, is monitored in the test circuits in the upper, middle, or lower sides of the power driver.

- **The interaction between different types of transistors** as described in Section 2.7.7 is not applicable here. However, it may be of interest to determine the effect of an equivalent amount of noise on a depletion or enhancement transistor. Also, the size of the depletion and enhancement transistors, depending on their tolerance to noise, may affect the noise behavior of the circuit (such as an inverter or latch).

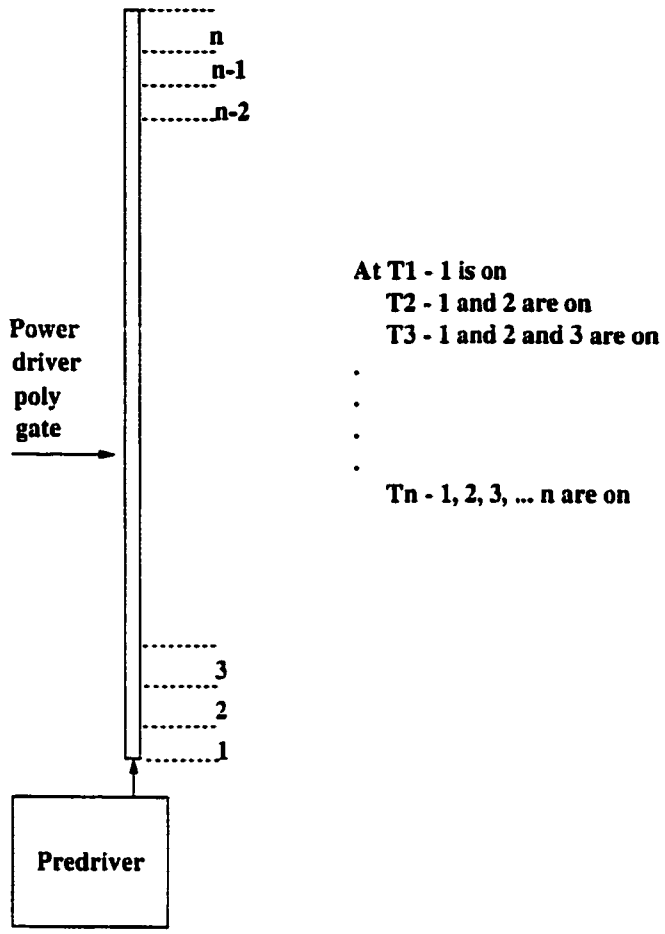


Figure 3.5: The successive power driver turn-on due to the distributed *RC* characteristics of the long polysilicon gate

- **The influence of the supply voltage of the noise source** (see Section 2.7.8). For these smart-power test circuits, the supply voltage of the power drivers has a major functional role by creating a specific dissipated power in the power resistors (see Fig. 3.1a). Different supply voltages can be used while maintaining the same dissipated power level in the resistor by modifying the value of the resistor. Accordingly, it is of interest to determine the noise that is generated by the power drivers for different supply voltages.

- **Logic circuit size** as described in Section 2.7.9 is not applicable here. The magnitude of the noise source defined as the number of power drivers that are active at any one time is of interest here.

- **Routing of the power lines:** The routing of the power and ground lines for the power drivers is constrained by the power drivers and the power heating resistors having a specific on-chip position to satisfy the chip function. However, the routing of the power and ground lines of the predrivers and logic blocks can be varied, which may significantly influence the noise that is received by the different circuit blocks. Therefore, the influence of the routing of the power and ground lines of the predrivers and logic blocks on noise is studied. Particularly, the influence of common or separate grounds between the power drivers and the rest of the circuitry is investigated.

- **Among the other issues** mentioned in Section 2.7.11, only the sensitivity of the register orientation is studied in the present analysis. In the test circuits, the registers are placed in different orientations with respect to the power drivers (the noise source).

  RF effects, such as the noise induced in the substrate from the RF or high frequency switching through the skin effect are not applicable here, since the frequency of operation is much too low (below 500 KHz).

  As mentioned in Section 2.7.11, multiple pads reduce the inductance of the bonding wires, reducing the noise and settling time. However, due to packaging constraints, only one pad is used for each of the power and ground lines and for all of the substrate contacts (see Figs. 2.13 and 2.16). Since a probe card is used in the tests, the inductance, as compared to a bonding

wire, is reduced. However, this advantage is reduced by the set-up used for testing which requires long wires between the test equipment and the probe card. These wires introduce an additional inductance. A combination of these two factors, the reduced inductance introduced by the probe card and the increased inductance introduced by the long wires, introduce a medium inductance effect as discussed in Sections 2.7.4 and 2.7.11.

3.3.2 Specific noise issues in smart-power applications

Specific issues that may influence the generation, transmission, and reception of noise specifically in sensitive digital circuits in a smart-power environment are defined and discussed in this section. Due to the specific nature of the smart-power applications, issues such as distance, substrate contacts, switching speeds, the distributed *RC* poly gate, the supply voltage of the noise source, the size of the noise source, the power line routing, and the placement and orientation of the digital blocks (see Section 3.3.1), have completely different effects as compared to the *digital influencing analog* type of applications, and therefore are topics which need to be investigated in a smart-power application. Additional issues, specific to digital circuits in a smart-power environment, require investigation, such as the clock and signal conditioning of the digital circuits, the dependence of the noise magnitude on the duration of the noise pulse, the influence of the noise pulse skewing among the power drivers, and the influence of the chip temperature. These new issues are described next.

- **Clock and signal conditioning of digital circuits:** The clock and clock-bar signals, necessary for the operation of both the static and dynamic registers, are generated internally by a non-overlapping clock generator fed by

an external clock. The sensitivity of the digital logic blocks to noise depends upon the data input and the clock and clockbar state while the power drivers are switching, become active, and remain active.

The noise affects an enhancement and a depletion transistor differently due to issues such as different threshold voltages and geometric sizes. As shown in Section 4.1.5, different noise levels are necessary to induce a parasitic low-to-high and high-to-low transition at the output of an inverter. Also, as shown in Chapter 5, for a static register, a parasitic transition can be practically induced only when the input is high. Accordingly, the noise behavior of the logic blocks depends on the input data. Also, as shown in Fig. 3.1c and discussed in Section 3.1, the Q transistor in the static slave latch is used to reset the register when the clear signal is high. This Q transistor increases the sensitivity of the slave latch output to noise as compared to the master latch output, since, due to the noise induced V_T variations and increased *forward biasing effects* (see Section 4.1 for more details), the Q transistor may sink more current from the output node of the slave latch to the ground as compared to the master latch output. If ckbar is active (see Fig. 3.1c), the slave latch provides a closed loop and a parasitic transition is latched. If ck is active, the master latch provides a closed loop, but is less susceptible to latching a parasitic transition due to the absence of a similar Q transistor on the latch output. Since the ck and ckbar states depend on the state of the input clock that feeds the non-overlapping clock generator, the sensitivity of the latches to noise depends upon the state of the input clock.

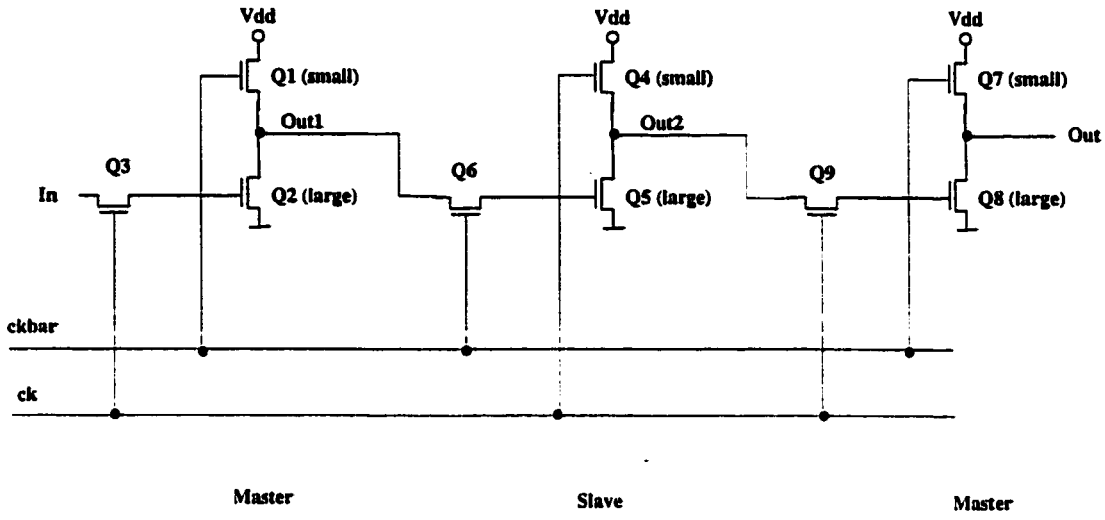


Figure 3.6: A chain of dynamic master and slave latches

A similar analysis can be made for dynamic latches, this time the emphasis being placed on the different sizes of the transistors, and on the operation of the circuit. As shown in Fig. 3.6, Q2, Q5, and Q8 are large transistors, while Q1, Q4, and Q7 are small transistors. For a master latch, the gate of the large transistor is controlled by ck for a master latch and by ckbar for a slave latch. When ckbar is active, the gate of the large transistor of a master latch is floating, making the transistor more sensitive to noise. Note that the information stored in the master latch is available at the output of the register (of the slave latch) when ckbar is active. These two issues demonstrate that a master-slave register is more sensitive to noise when ckbar is active than when ck is active.

- **Influence of the duration of the noise pulse:** The amount of time during which the power drivers are on (the noise pulse duration) may affect the logic circuitry. The typical noise waveform, as reported in the literature and shown in Fig. 2.5, suggests that noise is present only during the signal

transitions, and therefore is independent of pulse duration. However, the data shown in Fig. 2.5 are obtained for a low voltage noise source. For a high voltage and high current device, the influence of the pulse duration on noise requires additional investigation.

- **Influence of the noise pulse skewing.** As shown in Section 3.1, each test circuit contains at least one group of independently controlled power drivers (noise sources). The on/off control signals of these power drivers may be skewed due to different gate and interconnect delays. According to Fig. 2.5, skewed on/off pulses determine skewed noise spikes induced by skewed substrate noise. The skewed pulses may produce a smaller amplitude and/or a longer duration noise voltage signal. The high voltage and high current drivers may also produce different noise effects that can be amplified by the skewed on/off noise pulses.

- **Influence of chip temperature:** The temperature can affect the behavior of the noise sensitive circuitry due to issues such as threshold voltage dependency on temperature and increased temperature induced electron lattice vibration. In these smart-power IC applications, high voltages and currents are switched. These power pulses generate large temperatures and temperature gradients within the substrate. The noise induced temperature gradients further increase the problem of high temperatures and temperature gradients.

3.4 Test-plan and set-up

A test plan is presented in this section, that describes various issues that are considered in the present investigation. Approximately fifty test circuits have been designed, fabricated, and tested to satisfy the requirements of this test plan. The test set-up and equipment used for the analysis are also summarized in this section.

Table 3.1: Test plan for analysis of substrate coupling noise. Each issue is evaluated for both static and dynamic registers.

Test No.	Issue
1.	Distance
2.	Substrate contacts and layout aspects
3.	Power drivers turn-on/turn-off transition times, and the distributed *RC* line effect of the polysilicon gate of the power driver
4.	The noise behavior of an enhancement transistor as compared to a depletion transistor
5.	Power driver supply voltage and current
6.	The size of the noise source (the number of active power drivers at a given moment)
7.	Ground layout and connectivity
8.	Position and orientation of the sensitive registers
9.	Clock and data signal conditioning
10.	Noise pulse duration (the time during which the power drivers are on)
11.	Skewing of noise pulse between power drivers
12.	Influence of temperature

3.4.1 The test plan

The issues that have been proposed for the analysis of noise in a smart-power environment are summarized in Table 3.1. Each issue is evaluated individually and in combination with other issues depending upon the particular test being conducted.

3.4.2 The test set-up

The principal equipment used during testing is an *Electroglas 2001X Automatic Wafer Prober.* A 24 pin probe card is used to probe the test circuits on the wafer. The input signals are generated by an HP Programmable signal generator which can generate up to 15 independent programmable signals. Software has been written in an equipment specific language to generate the signals for each individual test configuration. The circuit output signals are acquired using an *HP 16500A Programmable Logic Analysis System,* permitting the observation of up to four independent channels. Also, on certain occasions, a Tektronix digitizing oscilloscope is used to analyze these test circuits.

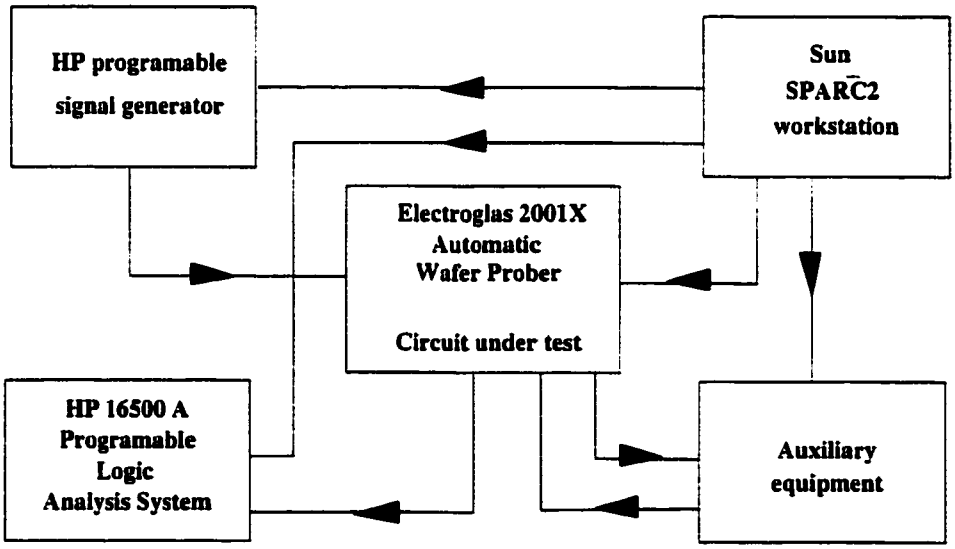


Figure 3.7: The experimental test set-up

Several programmable power supplies, multimeters, and a printer are also used. All of this equipment is controlled by a Sun Sparc2 workstation. Software has been written in the C programming language to support the equipment programming, communication, and synchronization. The experimental set-up is depicted

in Fig. 3.7. A complete list of the equipment that is used with photos of the actual test laboratory at Xerox Corporation as well as relevant equipment characteristics are provided in Appendix B.

Chapter 4

Theory of the Noise Behavior of Digital Circuits

A digital circuit is insensitive to the presence of substrate noise if the output of the digital circuit does not change state. Therefore, the circuit may tolerate a certain amount of substrate noise without any disturbance in the operation of the circuit. The amount of substrate noise that can be tolerated by a digital circuit depends upon a multitude of factors related to the particular digital logic family. Certain phenomena relating to the noise behavior of digital circuits determine the amount of noise that can be tolerated by a digital family. In this chapter, several models and mechanisms are developed to explain how substrate noise affects a digital circuit. The validity of these models and mechanisms are also verified in Chapter 5 by simulations of the NMOS circuits, and in Chapter 6 by experimental test data.

The models and mechanisms are discussed in this chapter. The objective is to explain the process in which substrate noise that is received by a digital logic element affects the integrity of a digital signal. In Chapter 5, the noise behavior of NMOS circuits is analyzed by means of circuit level simulations according to the proposed models and mechanisms.

4.1 Models and mechanisms

As described in Sections 3.3.1 and 3.3.2, various aspects contribute to the generation, transmission, and reception of noise. These aspects affect the noise distribution throughout the substrate. In this section, several models and mechanisms are discussed to explain how a digital circuit is affected by the amount of noise existent throughout the substrate.

A model describing the noise transmission process through the substrate is first described in Section 4.1.1. The importance of the operating point and region of operation of a transistor to the noise immunity is briefly discussed in Section 4.1.2. Another issue that affects the noise immunity of a digital circuit specific to smart-power circuits, herein called *noise induced forward biasing effects*, is discussed in Section 4.1.3. The importance of the logic family type, the body effect, and the voltage transfer characteristic of a digital family are discussed in Sections 4.1.4 and 4.1.5, respectively. All of these topics are integrated in Section 4.1.6 into a general process that explains the manner in which digital circuits are affected by substrate noise.

4.1.1 A model for noise transmission through the substrate

As described in the literature (see Section 2.6), the substrate can be modeled as a mesh of resistors or R mesh [77–79], or as a mesh of parallel resistors and capacitors or RC mesh [80–83]. These models have been developed to analyze substrate coupling in circuits where the digital circuitry generates noise that influences the highly sensitive analog circuitry.

In the present work, substrate coupling in smart-power circuits is described where the noise receptor is the digital circuitry. It is argued here that, compared to the influence of noise in an analog circuit, the distribution of the noise within the substrate is the principal issue that significantly influences the noise behavior of a digital circuit. While an analog circuit is affected by both uniform as well as by a non-uniform distribution of substrate noise, a digital circuit is believed to be affected predominantly by a non-uniform distribution of substrate noise. This assumption is demonstrated by simulations and confirmed by experimental data. Therefore, the following aspects are considered for the substrate model and for the noise transmission process through the substrate:

1. The negative and positive substrate voltage transients generated during the on-off switching by the power drivers are transmitted through the substrate.

2. The substrate in the direction of the transmitted noise signal can be modeled as a distributed RC line.

3. The delay of the noise signal between two substrate points depends upon the RC characteristics of the substrate.

An assumption that the noise source can be characterized as a *point source* is made, meaning that the size of the noise source is negligible as compared to the distance between the noise source and the noise receptor (as shown in Fig. 4.1).

Note in Fig. 4.1 that different transistors acting as noise receptors are placed at different distances with respect to the noise source. L_k is among the shortest distances. The transistors belonging to line 1 are closer than the transistors belonging to line 2. Since the process in which noise propagates through the substrate is similar to the process in which a signal propagates along a distributed

RC interconnect line, the transistors that are closer to the noise source are affected first by the noise. The delay of the noise signal between two neighboring transistors therefore depends upon the RC characteristics of the substrate.

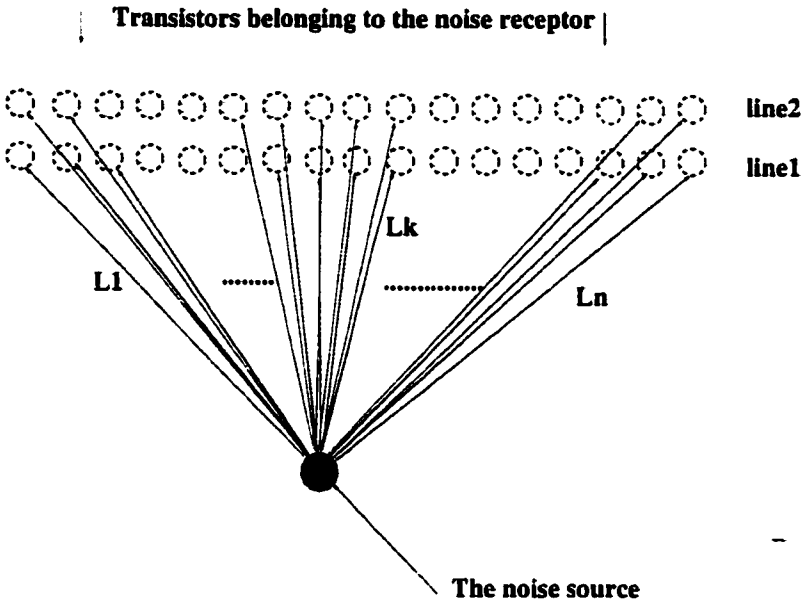


Figure 4.1: The noise distribution where the size of the noise source is negligible as compared to the distance between the noise source and the noise receptor (characterizing a *point source*)

For the target mixed-signal application, the power drivers (the noise sources) are large. Due to the distributed RC characteristic of the polysilicon gate of the power driver, the power driver is progressively turned on and off in small segments as the signal propagates through the highly resistive polysilicon gate. Therefore, for the most sensitive registers, the noise source can not be considered as a *point noise* source, except for particular situations such as where the driver 1 of group 1 is active and register 32 is the noise receptor (see Fig. 3.3a). These effects are amplified since each noise receptor receives a burst of noise corresponding to the turn-on of different sections of a power driver (see Fig. 3.5) and to the skewing between the power drivers as explained in Section 3.3.

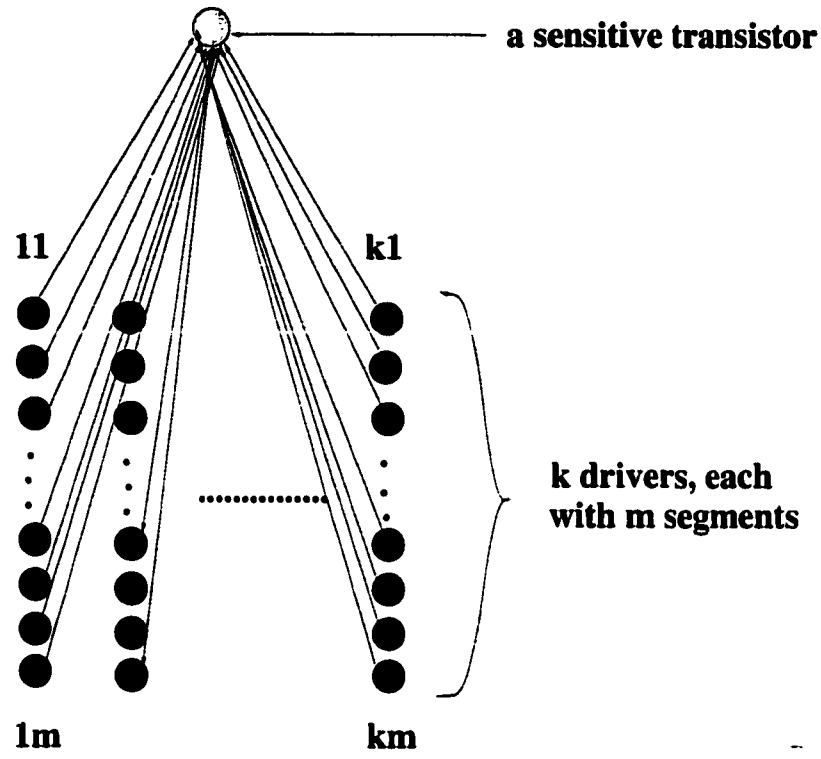


Figure 4.2: The noise received by a sensitive transistor from k active drivers. Each segment of each power driver turns-on at a different time due to the *RC* characteristics of the polysilicon gate

As described above, the noise through the substrate is non-uniform. Each transistor of a sensitive register receives a different amount of noise, which is the sum of the noise coming from different segments of a driver and from different drivers, and is amplified by the temperature gradients as described in Section 3.3. If k drivers are considered active at a given moment, the amplitude of the substrate noise received by a sensitive transistor at a certain point in time (see Fig. 4.2) is

$$V = \sum_{i=1}^{m} \sum_{j=1}^{k} \sigma V_{ij}. \tag{4.1}$$

The first summation in (4.1) is from 1 to m, corresponding to the m segments of a driver, and the second summation is from 1 to k, corresponding to the k active drivers. The coefficient σ depends upon the transmission characteristics

of the substrate, on the time at which each segment of a certain driver becomes active, and on the RC characteristics of the substrate between a segment of the driver and the sensitive transistor. V_{ij} is the noise voltage that is generated by the segment i of driver k. The transmission characteristics of the substrate incorporate the issues described in Sections 3.3 and 3.3.1, such as, for example, the dependence of the noise on distance. The other two aspects incorporated in σ, the time when each segment of a particular driver becomes active and the RC characteristics of the substrate between the segment and the sensitive transistor, describe the noise propagation characteristics through the substrate and the noise amplitude that is seen by a sensitive transistor at a particular time depending upon each of the $m*k$ noise waveforms generated by the power driver segments, as implied by (4.1). As mentioned, the RC characteristics of the substrate between each segment and the sensitive transistor determines the delay characteristics of the noise signal.

4.1.2 The importance of the transistor operating point and region of operation

Consider Q an NMOS transistor, as shown in Fig. 4.3, which makes up part of an analog circuit. As discussed in Section 2.4, the V_{pp} noise voltage at the output of the current source, as illustrated in Fig. 2.5, is generated by the V_T variations of the Q transistor due to the negative and positive voltage transients present within the $P-$ substrate. Any value of V_{pp} can affect an analog circuit. Accordingly, any noise voltage transients that are present within the $P-$ substrate are important if the Q transistor is behaving as an analog circuit.

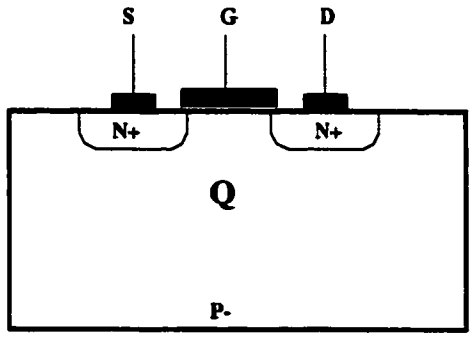


Figure 4.3: An NMOS transistor

A current source, in order to provide a constant current, is typically designed to operate in the saturation region. Accordingly, the I_{DS} current is

$$I_{DS} = K_E(V_{GS} - V_T)^2(1 + \lambda V_{DS}), \tag{4.2}$$

where I_{DS} is the drain-to-source current, V_{GS} is the gate-to-source voltage, V_{DS} is the drain-to-source voltage, λ is a MOSFET parameter characterizing the channel length modulation, and K_E is given by

$$K_E = \frac{1}{2}\mu_n C_{ox}\frac{W_E}{L_E}. \tag{4.3}$$

In (4.3), μ_N is the electron surface mobility, C_{ox} is the gate oxide capacitance per unit area, and W_E and L_E are the channel width (W) and length (L) of an enhancement (E) transistor, respectively. $K_E^{'}$ is defined as a constant independent of the W and L of a transistor,

$$K_E^{'} = \frac{1}{2}\mu_n C_{ox}. \tag{4.4}$$

Note that for the same noise induced V_T variations, the same process (λ and $K_E^{'}$), and same I_{DS}, a small size transistor and a large V_{GS} produces a smaller V_{pp} (V_{DS}) than a large size transistor and small V_{GS}. An analog process with small λ is also beneficial for noise immunity. For a same size transistor with the same operating

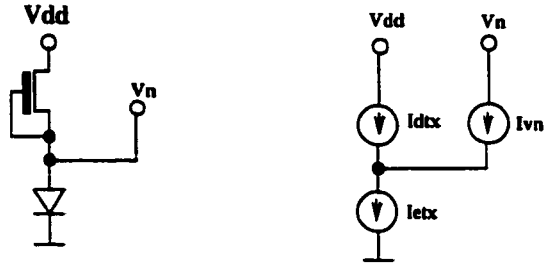
point (V_{GS}), V_T noise induced variations, and process technology, as the current I_{DS} increases, the V_{pp} variations (V_{DS}) increase. Also, a transistor operating in the linear region with the same V_{GS} as an equal size transistor operating in the saturation region is less sensitive to V_T variations (and thereby to noise), producing a smaller V_{pp}.

4.1.3 Noise induced forward biasing effects

The noise voltage transients generated within the substrate in a mixed-signal smart-power circuit [as described by (4.1)] can be significant as compared to a mixed-signal circuit where the sensitive circuitry is analog and the noise is generated by the digital circuitry. Accordingly, this discussion is not applicable to a *digital influencing analog* type of application.

Consider the Q transistor shown in Fig. 4.3 as part of a logic element such as an inverter (see Fig. 3.1d). If $V_{in} = high$, then the Q transistor is in the linear region (small V_{DS} and a continuous channel from drain-to-source) and $V_{out} = low$. A positive substrate voltage transient greater than approximately 0.7 volts can forward bias the substrate-to-drain, substrate-to-source, and substrate-to-channel junctions. The equivalent schematic of the inverter in this situation is shown in Fig. 4.4.

If V_n, which is the amplitude of the substrate transient voltage, is greater than 0.7 volts, then V_n forward biases the aforementioned junctions ($V_F \approx 0.7$ volts), and a current I_{vn} is injected from the substrate into the enhancement transistor. The I_{vn} current depends upon the value of V_n. If V_n is smaller than typically 0.7 volts, $I_{vn} = 0$.



a) Circuit schematic **b) Equivalent circuit schematic**

Figure 4.4: The equivalent schematic of the NMOS inverter shown in Fig. 3.1d for a large positive substrate noise transient

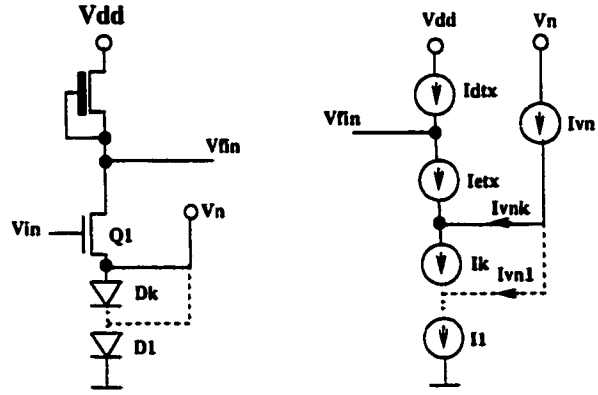
In the absence of noise ($V_n = 0$),

$$I_{etx} = I_{dtx}. \tag{4.5}$$

I_{etx} is the current through the enhancement transistor shown in Fig. 3.1d which operates in the linear region, and I_{dtx} is the current through the saturated depletion transistor. The inverter output $V_{out} = V_{equilibrium} = low$. In the presence of noise ($V_n \geq 0.7V$),

$$I_{vn} + I_{dtx} = I_{etx}. \tag{4.6}$$

Due to I_{vn}, I_{dtx} decreases, inducing V_{out} to increase to V_{fin}. Depending upon the value of V_n, V_{fin} can reach V_{dd}. Accordingly, it is demonstrated that through this mechanism, a positive substrate noise transient voltage can induce a parasitic transition at the output of the logic element as shown in Fig. 3.1d, where the output is normally at logic low. The parasitic transition can reach a level that can be interpreted as a logic high by the next logic element. In the final state, an equivalent schematic of the inverter under noise is shown in Fig. 4.5.



a) Circuit schematic b) Equivalent circuit schematic

Figure 4.5: The equivalent schematic of an NMOS inverter for a large positive substrate noise transient

Note in Fig. 4.5a that, depending upon the value of V_n, up to k diodes, D1...Dk, are connected between the source of Q1 and ground. The number of diodes ensures that the drain of Q1 is not forward biased, and Q1 operates primarily in the linear region, satisfying the conditions,

$$I_{dtx} = I_{etx}, \tag{4.7}$$

and

$$I_{etx} + I_{vnk} = I_k. \tag{4.8}$$

The channel length of Q1, L1, is always smaller than the channel length of the initial Q transistor, $L1 \leq L$. The Q1 transistor therefore has a larger transconductance than Q since $W/L1 \geq W/L$.

4.1.4 The influence of the logic family on the noise behavior of the logic circuits

A parasitic transition at the output of a logic element can be induced by the substrate noise voltage transients that reach different transistors of the logic ele-

ment (Section 4.1.1) either through V_T variations (Section 3.1) or through forward biasing effects (Section 4.1.3). In both cases, the noise sensitivity of a logic element, for the same amount of transient noise voltages, depends upon the family in which the logic element is implemented. Issues such as 1) the type of transistors that constitutes the logic element [NMOS and PMOS transistors such as in a CMOS logic element, or enhancement and depletion transistors such as in a static NMOS logic element (Fig. 3.1d), or only enhancement transistors such as in a dynamic NMOS logic element (Fig. 3.1e)], 2) the presence or absence of a DC current during any of the logic states (NMOS vs. CMOS), 3) the magnitude of the DC current (Section 4.1.2), or 4) the transistor sizes (Section 4.1.2), affect the sensitivity of a logic element to noise.

4.1.5 The influence of the Voltage Transfer Characteristic (VTC) on the noise behavior of a logic element

The behavior of logic primitives such as inverters and static and dynamic latches in a noisy environment is discussed in this subsection. As mentioned briefly in Chapter 1 and Section 2.1, in a noisy environment the behavior of circuits that process logic signals is quite different from the behavior of circuits that process analog signals. While any amount of noise will affect an analog signal, the same amount of noise for a digital signal is significant only if the change in the output signal of a digital element under the influence of noise is sufficient to affect the binary logic state.

For an equivalent amount of substrate noise, the nature of the circuit influences the likelihood of a digital circuit to change state. The noise behavior varies greatly from digital logic family to digital logic family, depending upon the voltage transfer

characteristic of a particular logic family. A classical voltage transfer characteristic of a digital circuit is shown in Fig. 4.6 [96, 97].

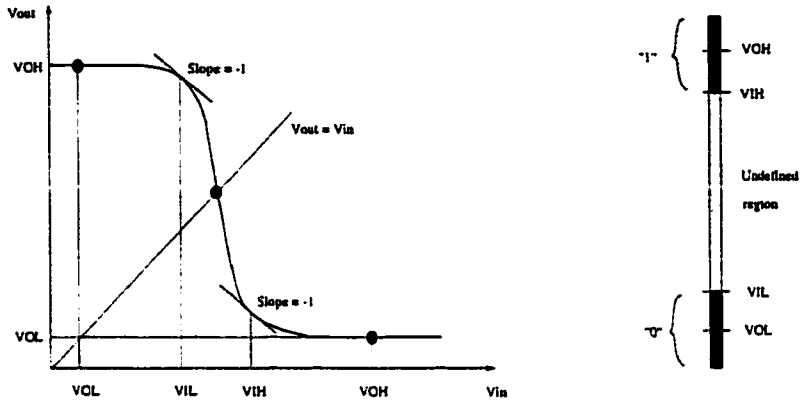


Figure 4.6: A general voltage transfer characteristic

The standard definitions for V_{OH}, V_{OL}, V_{IH}, and V_{IL} are:

- V_{OH}: Maximum output voltage when the output level is logic "1"
- V_{OL}: Minimum output voltage when the output level is logic "0"
- V_{IL}: Maximum input voltage which can be interpreted as logic "0"
- V_{IH}: Minimum input voltage which can be interpreted as logic "1"

The noise margins for a logic family are depicted in Fig. 4.7, NM_L being the low noise margin and NM_H being the high noise margin.

$$NM_L = V_{IL} - V_{OL}, \tag{4.9}$$

and

$$NM_H = V_{OH} - V_{IH}. \tag{4.10}$$

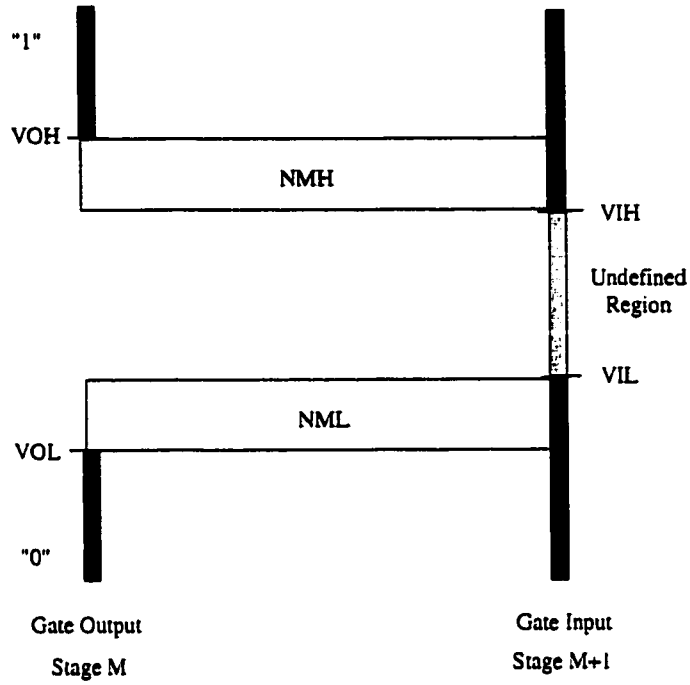


Figure 4.7: Definition of noise margins of a digital logic family

Consider an inverter L1 (see Fig. 4.8) for an arbitrary logic family that drives a logic element L2 such as an inverter. If $V_{in} = high$, then $V_{out} = low$. Consider a positive noise voltage transient V_{pp+} induced at the output of L1 either through V_T variations or through forward biasing effects. The limiting condition for V_{pp+} to not affect the logic element L2 is

$$V_{OL} + V_{pp+} \geq V_{IH}. \tag{4.11}$$

Similarly, if $V_{in} = low$, $V_{out} = high$. A negative transient noise voltage V_{pp-} which is similarly induced at the output of L1 generates a similar limiting condition to ensure that the logic element L2 is not affected,

$$V_{OH} + V_{pp-} \leq V_{IL}. \tag{4.12}$$

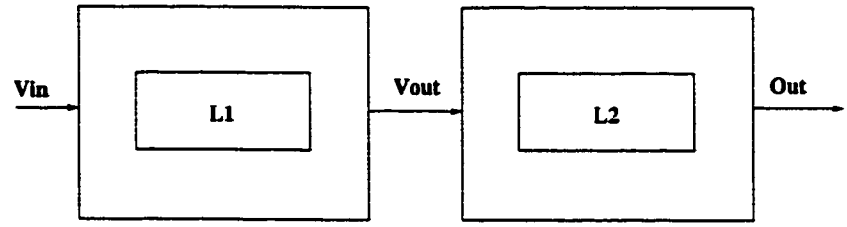


Figure 4.8: Two serially connected logic elements (such as inverters)

V_{pp-} and V_{pp+} could be seen as equivalent to the negative and positive spikes of V_{pp} shown in Fig. 2.5. Note that, according to (4.11) and (4.12), for the same amount of noise (same V_{pp+} and V_{pp-}), a logic circuit may or may not be affected, depending upon the voltage transfer characteristics of the logic family (V_{OH}, V_{OL}, V_{IH}, and V_{IL}).

The static NMOS family under discussion in this chapter is a standard enhancement/depletion family (depletion load family). The voltage transfer characteristic analysis of an NMOS inverter with a depletion type load (see Fig. 3.1d) in the absence of substrate noise (zero substrate bias) generates the following VTC expressions [97],

$$V_{OH} = V_{DD}, \tag{4.13}$$

$$V_{OL} = V_1 - \sqrt{V_1^2 - \frac{k_E}{k_D}|V_{TDB}|^2}, \tag{4.14}$$

$$V_{IH} = V_{TE} + 2V_{out} + \frac{k_E}{k_D}|V_{TDB}|\frac{dV_{TD}}{dV_{out}}, \tag{4.15}$$

$$V_{IL} = V_{TE} + \frac{k_E}{k_D}(V_{out} - V_{DD} + |V_{TDB}|), \tag{4.16}$$

where

$$V_1 = V_{OH} - V_{TE}, \tag{4.17}$$

$$V_{TDB} = V_{TD} + \gamma(\sqrt{|2\Phi_F| + V_{out}} - \sqrt{|2\Phi_F|}), \tag{4.18}$$

k_E is given by (4.3), and

$$k_D = \frac{1}{2}\mu_N C_{ox}\frac{W_D}{L_D}. \tag{4.19}$$

γ is the substrate bias (or body-effect) coefficient, Φ_F is the substrate Fermi potential, and W_D and L_D are the channel width (W) and length (L), respectively, of the depletion mode (D) transistor. For a zero substrate bias and a 5 volt power supply, typical values for VTC are $V_{OH} = 5$ volts, $V_{OL} = 0.2$ volts, $V_{IH} = 2$ volts, and $V_{IL} = 1.4$ volts. The high and low noise margins are, accordingly, $NM_H = 3$ volts and $NM_L = 1.2$ volts.

The substrate noise, through the body effect, can influence the threshold voltages of the transistors, and according to (4.13)–(4.18), the voltage transfer characteristic of the logic family (V_{OH}, V_{OL}, V_{IH}, and V_{IL}). If, in a first approximation, the only effect of noise is the presence of V_{pp} at a logic output without affecting the threshold voltages of the transistors such that V_{OH}, V_{OL}, V_{IH}, and V_{IL} are essentially constant, then, for this logic family and according to (4.11) and (4.12), the values of the negative and positive spikes of V_{pp} that can induce a parasitic transition are

$$V_{pp-} \geq 3.6 \; volts \tag{4.20}$$

to induce a parasitic high-to-low transition, and

$$V_{pp+} \geq 1.8 \; volts \tag{4.21}$$

to induce a parasitic low-to-high transition. Note that according to (4.20) as well as (4.21), for this logic family, if an output is low, the necessary peak noise voltage (V_{pp+}) that can induce a parasitic low-to-high transition is smaller than the peak noise voltage (V_{pp-}) necessary to induce a high-to-low transition when the output is high.

In a complete analysis, V_{OH}, V_{OL}, V_{IH}, and V_{IL} vary due to aspects such as the effect of the load at a logic output, the transistor threshold voltage variations due to the substrate noise, and the influence of transistor size through k_E and k_D. These variations further affect the V_{pp-} and V_{pp+} values. The particular VTC and noise margins of the target logic family may have a major effect on the noise immunity of a logic family.

As mentioned in Section 4.1.2, V_{pp-} and V_{pp+} generated at the output of a logic element depend upon the current through the output transistors of the respective logic element, increasing as the output current increases. For an NMOS inverter (see Fig. 3.1d), a current flows through the two transistors when the output is low, amplifying the deleterious effect of the substrate noise. When the output is high, both transistors are off. The substrate bias, present due to the substrate noise (see Fig. 2.7), must first turn on the enhancement transistor (see Fig. 3.1d) through the body effect, and then must produce a sufficient bias current through the two transistors, thereby generating a sufficient V_{pp-} variation to induce a parasitic transition.

These explanations, (4.20), and (4.21), demonstrate that for a static NMOS logic element, a parasitic transition is more likely to be induced when the input is high (a low-to-high parasitic output transition). The high-to-low parasitic output transition (the input is low) is less sensitive to noise.

4.1.6 The mechanism of affecting the digital circuits by substrate noise

If a sensitive digital circuit has m transistors, according to (4.1), each transistor receives a substrate noise voltage V_j, where j is 1 to m. Depending upon the magnitude of V_j, V_j can affect the threshold voltages of the enhancement and depletion transistors through the body effect according to

$$V_{TEN} = V_{TE} + \gamma(\sqrt{|2\Phi_F| + V_j} - \sqrt{|2\Phi_F|}), \tag{4.22}$$

and

$$V_{TDN} = V_{TD} + \gamma(\sqrt{|2\Phi_F| + V_{out} + V_j} - \sqrt{|2\Phi_F|}), \tag{4.23}$$

or induce forward biasing effects as well as affect V_{TE} and V_{TD}. These threshold voltages affect the voltage transfer characteristic of the logic circuits as discussed in Section 4.1.5.

To exemplify this discussion, consider in Fig. 4.9 two inverters structured as an open loop static latch (such as the circuit shown in Fig. 3.1c) together with the distributed RC substrate impedances among the four transistors all in the direction of the traveling noise signal. Note the value of RC between the noise input and the first transistor along the noise path, Q1, and the values of $RC1$ and $RC2$ between each subsequent transistor.

If $In = high$ (Fig. 4.9), Out1 is low and Q1 operates in the linear region. The dependency of I_{DS} on V_T for a linear transistor is

$$I_{DS} = k_E[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]. \tag{4.24}$$

As discussed in Section 4.1.2, this dependency is weak as compared to when the transistor operates in the saturation region. As described in Sections 4.1.2

and 4.1.5, this dependence implies that for the same amount of noise, a smaller V_{pp} is generated for a transistor operating in the linear region as compared to a transistor operating in the saturation region, even if a large I_{DS} current is present for the linear transistor due to issues such as the transistor sizes of Q1 and Q2 (see Fig. 4.9). Therefore, for this logic family, it is unlikely that a substrate noise transition that does not induce any significant forward biasing effects (a noise transition smaller than 0.7 volts) can induce a value of V_{pp+} that is sufficiently large to induce a low-to-high parasitic transition as described by (4.11). Accordingly, when Out1 in Fig. 4.9 is low, only forward biasing effects can induce a possible parasitic transition.

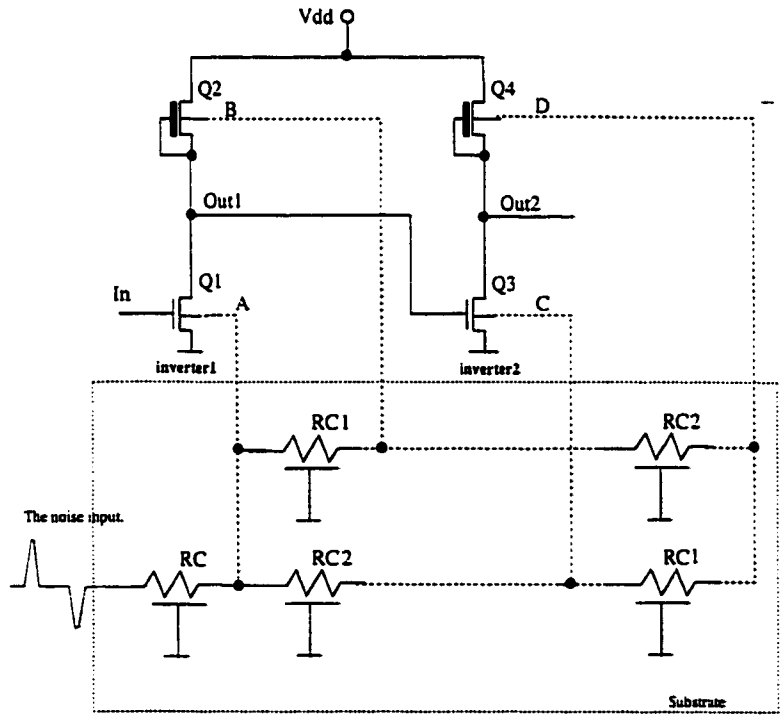


Figure 4.9: Two NMOS inverters with substrate noise. The noise path is shown. The substrate is modeled as a distributed RC mesh.

If $In = low$ in Fig. 4.9, both Q1 and Q2 are off and $Out1 = high$. While the source-to-substrate junction of Q1 may be forward biased for a positive noise

transient, the state of Out1 cannot change. The variations of V_T only, also cannot change the state of Out1. Accordingly, an inverter as shown in Fig. 4.9 can not change state when $In = low$ due to substrate noise. Therefore, this inverter can only change state when $In = high$ through forward biasing and V_T variation effects.

Table 4.1: Possible situations for the traveling noise wave to affect the four transistors, where A or B are the noise inputs.

No.	Situation	Comments
1.	RC1, RC2 negligible	The noise wave affects all transistors at the same time
2.	RC1 negligible	Q1, Q2 are affected first, then Q3, Q4 after a delay
3.	RC2 negligible A input	The affected order is Q1 and Q3, than Q2 and Q4
4.	RC2 negligible B input	The affected order is Q2 and Q4, than Q1 and Q3
5.	A input	The affected order is a) Q1, Q2, Q3, Q4 b) Q1, Q2 and Q3, Q4 c) Q1, Q3, Q2, Q4
6.	B input	The affected order is a) Q2, Q1, Q4, Q3 b) Q2, Q1 and Q4, Q3 c) Q2, Q4, Q1, Q3

Returning to Fig. 4.9, RC is considered negligible, effectively placing the noise input at point A. When the inverters are physically placed such that the depletion transistors are closer to the noise source, the noise input point is B. Depending upon the position of the on-chip register with respect to the noise source, the noise input can also be at nodes C or D. The possible situations for the traveling noise signal to affect the four transistors are listed in Table 4.1 for the A or B noise inputs. As described in Section 4.1.1 and shown in Fig. 4.9, each of the four

transistors receive a substrate noise signal V_1 for Q1 in A, V_2 for Q2 in B, V_3 for Q3 in C, and V_4 for Q4 in D that affects the transistors, the threshold voltages, and the voltage transfer characteristics, (4.13)–(4.16). For the circuit schematic shown in Fig. 4.9, the conditions under which a parasitic glitch present at Out1 is transmitted to Out2 are shown in Table 4.2, where V_{TEN} and V_{TDN} signify the V_T variation effects and the *"noise"* signifies the forward biasing effects. Practically, as shown in this section, no transition is possible when $In = low$ for the conditions listed in Table 4.2.

Table 4.2: Possible conditions under which a parasitic glitch at Out1 is transmitted to Out2.

No.	Input	Condition
1.	High	$V_{out1} \geq V_{IH}(V_{TEN}, V_{TDN}, noise)$ $V_{out1}(V_{TEN}, V_{TDN}, noise) \geq V_{IH}$ $V_{out1}(V_{TEN}, V_{TDN}, noise) \geq V_{IH}(V_{TEN}, V_{TDN}, noise)$
2.	Low	$V_{out1} \leq V_{IL}(V_{TEN}, V_{TDN}, noise)$ $V_{out1}(V_{TEN}, V_{TDN}, noise) \leq V_{IL}$ $V_{out1}(V_{TEN}, V_{TDN}, noise) \leq V_{IL}(V_{TEN}, V_{TDN}, noise)$

Any of the master or slave latches may latch a parasitic transition when the loop of the respective latch is closed by a pass transistor that is controlled by the ck and ckbar signals (see Fig 3.1c). The parasitic transition is produced at Out1, transmitted to Out2 (see Fig. 4.9), and returned at the latch input through the pass transistor from the loop. Note that the input of the respective latch is either 0 volts (output low) or a maximum of 4 volts (output high) due to the V_T drop across the pass transistor. If the output is smaller than 4 volt, than the input is equal to the output.

A parasitic transition at Out2 of the previous master (slave) latch may also be latched into the next slave (master) latch (see Fig. 4.10) without the parasitic transition at Out2 being latched into the previous master (slave) latch. However,

there is a small probability that a parasitic transition present at Out2 of the current latch may not be latched by the current latch but rather is latched by the following latch. This condition may occur due to issues such as the relative timing of the ck and ckbar signals. Also, any of the master or slave latches may latch a parasitic transition produced at Out2 and transmitted at Out1 when the loop of the respective latch is closed by the pass transistor.

Note, however, that in the latter two cases the Out2 parasitic transition amplitude (V_{pp-} and V_{pp+}) reaches the input of the corresponding latch a threshold voltage drop (V_{TE} or V_{TEN}) smaller due to the pass transistor present between the victim output and the corresponding input. Also, the parasitic transition reaches the corresponding input after a larger delay as compared to when a parasitic transition at Out1 reaches inverter2, due to the delay through the pass transistor. Note also that if $Out1 = high$ ($In = low$), a parasitic transition may be induced, albeit with a smaller probability than for $In = high$ ($Out1 = low$).

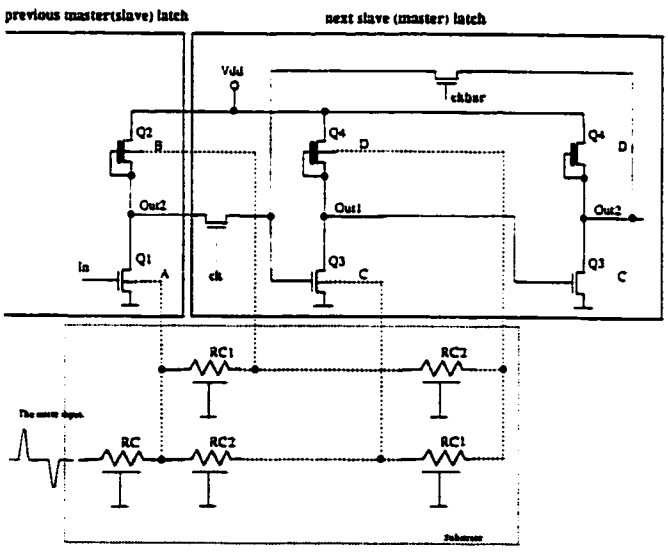


Figure 4.10: A parasitic transition at the output of a previous latch can be latched into the following latch

The above analysis demonstrates that for the circuit illustrated in Fig. 3.1d, a parasitic transition is more likely to be latched when Out1 is low ($In = high$) and the low-to-high parasitic transition is present at Out1 of any latch. In particular, a parasitic transition will be latched at Out1 of a slave latch (due to the Q transistor as shown in Fig. 3.1c and Section 3.3.2).

Chapter 5

Simulation Results of the Noise Behavior of Digital Circuits

In this chapter, the models, mechanisms, and circuit considerations discussed in Chapter 4 describing how substrate noise affects a digital circuit are analyzed by simulations using Cadence Spectre [98]. The principal objective is to analyze the validity of the developed models and mechanisms. If the models and mechanisms describing the noise behavior of the digital circuits under noise in a mixed-signal smart-power environment are accurate, then the simulation results developed in this chapter are expected to match the experimental data from Chapter 6. As shown in Chapter 6, good agreement is obtained among the expected noise behavior derived according to the models, mechanisms, and simulation results, and the noise behavior derived from the experimental data.

An exhaustive analysis based on the aforementioned models and mechanisms for the noise behavior of the NMOS static inverter shown in Fig. 3.1d is provided in Section 5.1. In Section 5.2, a similar analysis for the static NMOS latch is described.

Certain NMOS technology parameters are described in [95]. The transistor ratios used during the present simulations are $k_E/k_D = 4$ and $k_E/k_D = 8$. The

nominal threshold voltages are V_{TE} = 1.2 volts and V_{TD} = -3.3 volts. Substrate voltage transients from +5 to -5 volts are considered. These substrate voltage transients are experimentally observed (see Chapter 6). Depending upon the size of the noise source (the number of active power drivers), the noise transients can be even larger than the above mentioned values.

5.1 The noise behavior of an NMOS inverter

An analysis of the inverter shown in Fig. 3.1d is performed for substrate voltage transients between +5 and -5 volts. As shown in Section 4.1, different transistors receive different amounts of noise depending upon their on-chip position with respect to the noise source(s). For the simulations presented here, the noise distribution as described by Fig. 4.9 is implemented as shown in Fig. 5.1, which is equivalent to Fig. 4.9 for only one inverter.

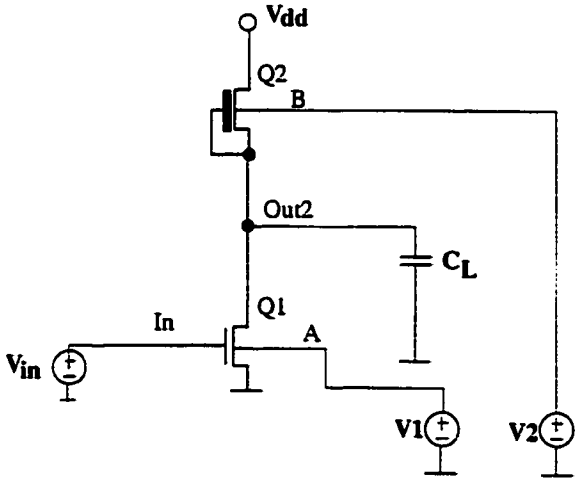


Figure 5.1: A circuit schematic used to simulate the noise behavior of an NMOS inverter

V1 and V2 are the noise signals for Q1 and Q2 according to (4.1). In Fig. 5.1, if A (B) is the noise input (Section 4.1.6), V2 (V1) is delayed with respect to V1

(V2) by a delay related to RC_1. If RC_1 is negligible, V1 and V2 are in-phase. A phase difference between V1 and V2 can also be caused by on-chip temperature gradients or by a noise distribution due to the different noise sources as described in Section 4.1.6. When a phase difference between V1 and V2 exists, it may be either as shown in Fig. 5.2a or as depicted in Fig. 5.2b. In both cases, a voltage difference between the substrate of the Q1 and Q2 transistors exists. The time during which this voltage difference exists depends on issues such as the RC characteristics of the substrate and the physical placement of Q1 and Q2.

Note in Fig. 5.2a that for large RC_1 delays the voltage difference between V1 and V2 is important, and may have a value equal to either $max(V1)$ or $max(V2)$. For small RC_1 delays (see Fig. 5.2b), the voltage difference between V1 and V2 is smaller. In both cases, V1 (V2) can lag V2 (V1), depending upon whether A or B is the noise input node.

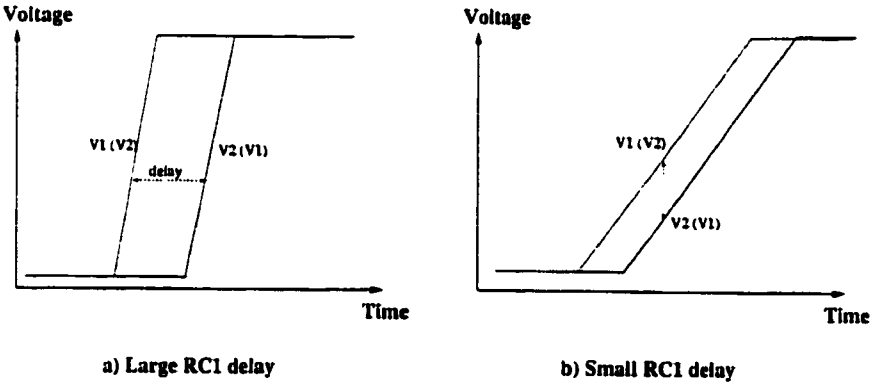


Figure 5.2: V1 and V2 noise voltages

If V1 and V2 are the noise voltages received by the two transistors shown in Fig. 5.1, the threshold voltages of the enhancement (Q1) and depletion (Q2) transistors vary. If V1 and V2 are larger than 0.7 volts, forward biasing effects are added to the V_T variations. In Table 5.1, the static behavior of an NMOS

inverter as depicted in Fig. 5.1 under the influence of noise is listed for $In = high$, $In = low$, and $k_E/k_D = 4$. For the static analysis, the load capacitance C_L has no influence. In Table 5.1, *High* is 5 volts and *Low* is 0 volts.

Table 5.1: Inverter analysis as a function of substrate bias

No.	In	V1 (V)	V2 (V)	V_{out} (V)	V_{TEN} (V)	V_{TDN} (V)
1.	High (Low)	5	5	5 (5)	0.91(0.92)	-2.8 (-3.2)
2.	High (Low)	4	4	4.6 (5)	0.91 (0.9)	-2.8 (-2.6)
3.	High (Low)	3	3	2.8 (5)	0.93 (0.88)	-3.3 (-2.2)
4.	High (Low)	2	2	1.6 (5)	0.94 (0.86)	-3.4 (-1.8)
5.	High (Low)	1	1	0.6 (5)	0.95 (0.84)	-3.4 (-1.4)
6.	High (Low)	0	0	0.2 (5)	1.2 (1)	-3 (-1)
7.	High (Low)	-1	-1	0.16 (5)	1.6 (1.46)	-2.6 (-0.7)
8.	High (Low)	-2	-2	0.12 (5)	1.9 (1.75)	-2.2 (-0.35)
9.	High (Low)	-3	-3	0.09 (5)	2.1 (2)	-1.8 (0)
10.	High (Low)	-4	-4	0.06 (5)	2.3 (2.2)	-1.4 (0.3)
11.	High (Low)	-5	-5	0.04 (5)	2.5 (2.4)	-1 (0.63)
12.	High (Low)	-5	-4	0.07 (5)	2.5 (2.4)	-1.4 (0.3)
13.	High (Low)	-3	-4	0.07 (5)	2.2 (2)	-1.4 (0.3)
14.	High (Low)	-3	-2	0.14 (5)	2.1 (2)	-2.1 (-0.35)
15.	High (Low)	-1	-2	0.12 (5)	1.6 (1.45)	-2.1 (-0.35)
16.	High (Low)	-1	0	0.22 (5)	1.6 (1.45)	-3 (-1)
17.	High (Low)	1	0	0.55 (5)	0.95 (0.84)	-2.9 (-1)
18.	High (Low)	1	2	1.4 (5)	0.93 (0.84)	-3.4 (-1.8)
19.	High (Low)	3	2	2.7 (5)	0.93 (0.88)	-2.8 (-1.8)
20.	High (Low)	3	4	3.4 (5)	0.92 (0.88)	-3.4 (-2.6)
21.	High (Low)	4	3	4.5 (5)	0.91 (0.9)	-2.4 (-2.2)

Note that for any range of combinations of V1 and V2, no parasitic transition at the output of the inverter can be induced when $In = low$, as is theoretically described in Section 4.1.6. However, as shown in Sections 4.1.5 and 4.1.6, there are values of V1 and V2 for which a parasitic transition at the output of the inverter can be induced by noise. The situations for which the output of the inverter can be interpreted by the following logic element as a parasitic *High* according to the conditions listed in Table 4.2 are listed in Table 5.1 [1, 2, 3, 4, 18, 19, 20, and 21

(4 and 18 are close to this condition)]. Note that in all of these situations both V_T variations and forward biasing effects are present, as is theoretically described in Section 4.1.6. No parasitic transitions are possible when only V_T variations are present (situations 5 to 17).

As described in Section 4.1.3, when forward biasing effects are present, the equivalent schematic in the final state is as shown in Fig. 4.5, with Q1 operating in the linear region for most of the cases due to the D1 to Dk diodes. To demonstrate this behavior, V_{DS} across the Q1 transistor (see Fig. 4.5), the voltage at the source of Q1 (V_{SQ1}, determined by the number of D1 to Dk diodes), V_{GS} of Q1 (V_{GSQ1}), and the source-to-substrate voltage of Q1 ($V1'$) for representative situations listed in Table 5.1, are listed in Table 5.2.

Table 5.2: Inverter analysis as a function of substrate bias

No.	Situation of Table 5.1	V_{DSQ1} (V)	V_{SQ1} (V)	V_{GSQ1} (V)	$V1'$ (V)
1.	2	≈ 1.2	≈ 3.4	≈ 1.6	≈ 0.6
2.	3	≈ 0.3	≈ 2.5	≈ 2.5	≈ 0.5
3.	4	≈ 0.05	≈ 1.6	≈ 3.4	≈ 0.4
4.	5	≈ 0.05	≈ 0.6	≈ 4.4	≈ 0.4

Note that for case 1 in Table 5.2, Q1 of Fig. 4.5 is saturated. Also, note that in all cases where forward biasing effects appear, Q1 has a body effect voltage ($V1'$) below 0.7 volts, explaining the limit on V_{TEN} variations (see Table 5.1) for a positive V1 (situations 1 to 6 and 17 to 21). Note in Table 5.1, however, the V_{TEN} variations for a negative V1 (situations 7 to 16).

When $In = low$, $Out = high$, and the source of the depletion transistor Q2 is at the output potential. Accordingly, for the entire range of the V2 variation from +5 volts to -5 volts, the body effect voltage of Q2 varies from 0 to -10 volts producing the V_{TDN} variations as listed in Table 5.1 (situations 1 to 11). The

threshold voltages of Q1 and Q2 are described by (4.22) and (4.23), where V_j from (4.22) is replaced by V_1' from Table 5.1, and V_j from (4.23) is replaced by $V_2 - V_{out}$. V_1' is smaller or equal to 0.7 volts for a positive V1, or is equal to V1 for a negative V1. The voltage transfer characteristic of the inverter under the influence of noise is described by (4.13)–(4.16), where V_{TE} and V_{TDB} are replaced by V_{TEN} and V_{TDN}. For those situations where forward biasing effects are present, a current flows from the substrate through the forward biased source junction (D1 to Dk) of Q1 (the magnitude of the current is on the order of milliamperes), increasing as the noise amplitude increases (the current through the inverter in normal operation is in the order of microamperes).

The situations, 1 to 11, listed in Table 5.1 characterize the case where the noise for the two transistors of Fig. 5.1 is in-phase, while the situations, 12 to 21, briefly characterize the case shown in Fig. 5.2b where RC_1 is small. The case shown in Fig. 5.2a is generally less likely in practice (RC_1 large), since Q1 and Q2 are generally close to each other. However, the case shown in Fig. 5.2a can exist also for RC_1 small (or for a brief time), especially for those cases where a highly non-uniform substrate noise distribution exists, as is the case in this target application.

Situations 12, 14, 16, 17, 19, and 21 listed in Table 5.1 consider A as the noise input node, while situations 13, 15, 18, and 20 consider B as the noise input node. Note that the negative noise voltage (negative substrate bias) does not induce any parasitic transitions for both in-phase or not in-phase noise. Situations 18 and 20 for $V_{in} = high$ are special situations, since the source junction of the depletion transistor is forward biased, potentially affecting the reliability of the circuit. Besides reliability problems, additional substrate noise is injected into the

substrate in these situations. Situations 18 and 20 occur for any positive substrate bias when the substrate of the depletion transistor is more positively biased than the substrate of the enhancement transistor (or when the noise input is B, and particularly, for a large phase difference between the noise at Q1 and Q2). The equivalent schematic for these situations is shown in Fig. 5.3.

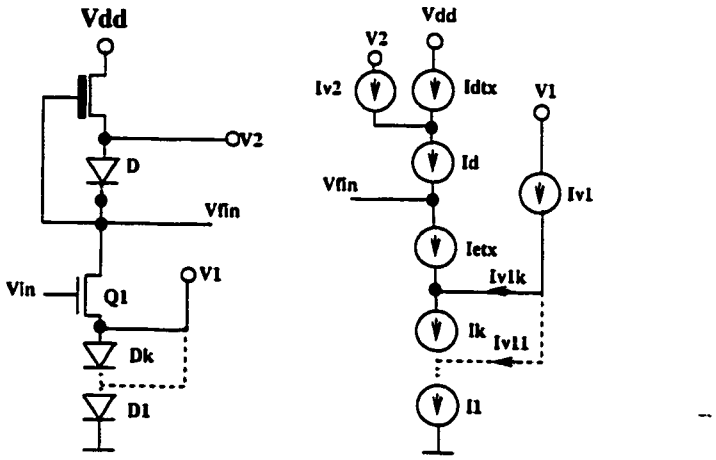


Figure 5.3: The equivalent schematic of the NMOS inverter shown in Fig. 3.1d for a large positive substrate noise transient, where V2 is greater than V1

For $k_E/k_D = 8$, the output parasitic transition decreases slightly in amplitude. For example, situation 2 in Table 5.1 changes to $V_{out} = 4.1$ volts, situation 5 becomes $V_{out} = 0.5$ volts, situation 21 becomes $V_{out} = 3.9$ volts, and situation 20 remains unchanged. If the noise is not in-phase and is consistent with Fig. 5.2a (a large phase difference), and if A is the noise input node, the larger the voltage difference between V1 and V2, the larger the difference between the V_{out} voltage for the $k_E/k_D = 8$ and the V_{out} voltage for the corresponding situation of Table 5.1 where $k_E/k_D = 4$. For example, for V1 = 4 volts and V2 = 0 volts, $V_{out} = 3.7$ volts from 4.6 volts in Table 5.1 (situation 2), while for V1 = 2 volts and V2 = 0 volts, $V_{out} = 1.52$ volts from 1.6 volts in Table 5.1 (situation 4). If B is the noise

input node, the output is 0.6 volts below V2, forward biasing the source junction of the depletion transistor. The larger the difference between V1 and V2, the larger the injected current into the substrate, since, according to Fig. 5.3,

$$V_{DSQ1} \approx V2 - V1 - 0.7. \tag{5.1}$$

Accordingly, fast noise transients, large non-uniformities in the substrate noise, or large RC_1 delays, each can create the worst case substrate voltage bias as shown in Fig. 5.2a. In this situation, if B is the noise input, important supplemental problems as shown (situations 18 and 20 from Table 5.1) are created.

A dynamic characterization of the inverter shown in Fig. 5.1 under noise can be summarized according to the following considerations (with reference to Figs. C.1 to C.12 of Appendix C). In all of these figures, V1, V2, and V_{out} are specified.

- For small load capacitance C_L (see Fig. 5.1), the steady state voltage at the inverter output corresponds to the values listed in Table 5.1 (see Figs. C.1a, C.1b, C.2a, C.4a, C.4b, and C.6b).

- For large load capacitances, the output voltage reaches the steady state values listed in Table 5.1 after a specific time that depends on C_L, k_E/k_D, V1, V2, and V_{in} (see Figs. C.2b, C.3a, C.3b, C.5a, C.5b, C.6a, C.7a, C.7b, C.8a, C.9a, C.10a, C.10b, C.11b, and C.12b). If the noise pulse duration is short, the steady state value may not be reached.

- The output voltage sharply follows the V1 and V2 waveforms for small output load capacitances (see Figs. C.1a, C.1b, C.2a, C.4a, C.4b, C.6b, C.8b, C.9b, C.11a, and C.12a).

- For $k_E/k_D = 4$ and large load capacitances, the rising edge of the output waveform is delayed with respect to V1 and V2, while the falling edge is

distorted (see Figs. C.2b, C.3a, C.3b, C.5b, and C.6a). An explanation for this behavior is the forward biasing effects as described in Section 4.1.3. Another explanation is that when the noise voltage (and the D1 to Dk forward biases) disappear, the recombination process to turn-off the diodes depends upon the transconductance of the Q1 transistor. The channel length of the Q1 transistor increases from L1 corresponding to the Q1 transistor shown in Fig. 4.5 to L corresponding to the Q1 transistor shown in Fig. 5.1 (see Section 4.1.3). Accordingly, the transconductance decreases from a value proportional to W1/L1 to a value proportional to W1/L. Note that the transconductance variation is proportional to the noise magnitude through the D1 to Dk diodes.

- A larger transconductance for the enhancement transistor ($k_E/k_D = 8$) improves the output waveform transition times and decreases the steady state output voltage (see Figs. C.5a, C.10a, C.11a, and C.11b).

- When V2 is greater than V1, the output is always $\approx$ 0.6 volts lower than V2. This behavior is shown in Figs. C.3a and C.4b for the entire noise pulse duration, in Figs. C.4a, C.5a, C.5b, C.7a, C.7b, C.8a, C.8b, and C.11b immediately after the rising edge of V2 when V1 is zero, and in Figs. C.6a and C.6b immediately after the falling edge of V1 when V1 is zero. The transition times depend upon the capacitive load (for example, compare Fig. C.4a with Fig. C.5a).

- As V_{in} decreases, while Q2 (see Fig. 5.1) pulls high similarly for any V_{in} value, Q1 pulls low differently for different values of V_{in}. Q1 requires more time to reach a low state as V_{in} decreases, slowing down the noise induced

high-to-low parasitic output transition (see Figs. C.7a, C.7b, and C.8a). The reason for this behavior is because as V_{in} decreases, V_{GS} of Q1 of Fig. 4.5 could be zero or negative, depending upon the value of V1, and Q1 could be off. When V1 becomes zero (the noise disappears), the D1 to Dk diodes are turned off, and V_{GS} of Q1 (V_{GSQ1}) becomes significant, the discharge process of the capacitive load of the inverter can start and the high-to-low transition of the output can be completed. Accordingly, this process is slower as V_{in} is smaller. Note also the difference of the output waveform with small and large capacitive loads (see Fig. C.7a as compared to Fig. C.8b, Fig. C.8a as compared to Fig. C.9b, Fig. C.11a as compared to Fig. C.11b, and Fig. C.12a as compared to Fig. C.12b).

- The output remains high for input voltages smaller than 2 volts (see Figs. C.9a, C.10a, C.10b, C.11a, C.11b, C.12a, and C.12b). Note that as Q1 increases in size (k_E/k_D increases), the equilibrium steady state output voltage level in the absence of noise decreases due to the increased transconductance of Q1 (see Fig. C.10a as compared to Fig. C.10b, and Figs. C.11a and C.11b as compared to Figs. C.12a and C.12b).

Several conclusions can be drawn from this inverter analysis.

- Only a positively biased substrate (positive V_{pp+} noise spikes as illustrated in Fig. 2.5) can induce a parasitic output transition for an NMOS inverter as shown in Fig. 5.1.

- Long duration noise spikes are more damaging than short duration noise spikes. The output steady state voltage level is reached even for large capacitive loads, and this output level is present for longer periods of time.

This behavior increases the likelihood that the parasitic transition will be propagated to the following logic element.

- A large capacitive load may improve the noise behavior of the logic elements particularly if the noise spikes are of short duration. This behavior occurs because the parasitic output transition has distorted edges for large capacitive loads, and the high steady state voltage level may not be reached or may be reached for a shorter amount of time which may not be sufficient to induce a parasitic transition in the next logic element. As shown, the higher the steady state voltage (the higher the input voltage for the following logic element), the more likely a significant parasitic transition will occur at the output of the next logic element. The drawbacks of using large capacitive loads are increased power dissipation, and, due to the poor high-to-low transition of the output, the noise behavior for noise spikes of long duration may also deteriorate.

- Large k_E/k_D ratios decrease the maximum steady state voltage and improves the high-to-low transition edges, with beneficial effects on the noise behavior. However, higher ratios increase the power dissipation and decrease V_{IH}.

- Depending on the phase of V1 and V2, the logic elements may generate extra noise into the substrate.

5.2 The noise behavior of an NMOS static latch

The static latch used in this analysis is shown in Fig. 3.1c. As described in Section 4.1.6, the most likely situation to latch a parasitic transition occurs when

the parasitic transition is induced at Out1 (Fig. 4.9) and transmitted to Out2. This situation is exhaustively characterized in this section.

The circuit illustrated in Fig. 5.4 is used in this investigation to simulate the noise distribution through the substrate under different noise voltages and phases for the transistors within a latch. The circuit shown in Fig. 5.4 is equivalent to the circuit illustrated in Fig. 4.9. Note that each of the four transistors, Q1, Q2, Q3, and Q4, has a different noise voltage source, V1, V2, V3, and V4, respectively, as discussed in Section 4.1.1. The situations shown in Table 4.1 are analyzed and correlated with the results deduced in Section 5.1 for the noise behavior of an inverter.

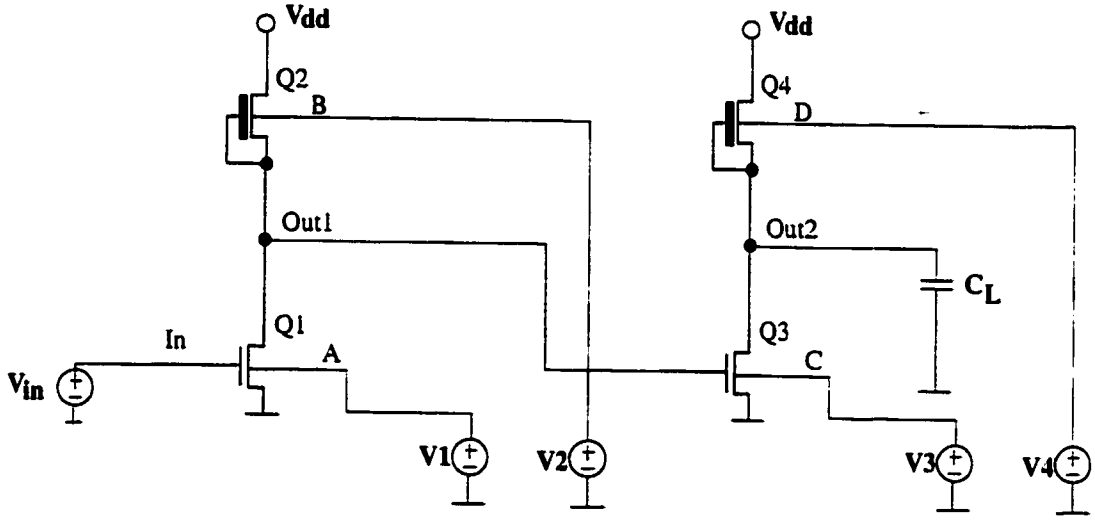


Figure 5.4: An open loop static latch used in the noise analysis

For these simulations, V_{in} is 4 volts so as to simulate the V_T voltage drop across the pass transistor in the loop. The transistor size and the $k_E/k_D = 4$ ratio are standard for this logic family. Observations are also made for $k_E/k_D = 8$.

1. Situation 1 listed in Table 4.1 is characterized by the Out2 output waveform of Fig. 5.5. Note that no parasitic transition occurs at Out2 when the noise

voltages, V1, V2, V3, and V4, of the four transistors, Q1, Q2, Q3, and Q4 (see Fig. 5.4), are in-phase. However, noise spikes are present when the noise signal transitions to a maximum value as well as when the noise signal transitions back to zero. In equilibrium (for zero noise), since V_{in} is high, V_{out2} is high (5 volts). Note in Fig. 5.5 that when the noise transitions from zero to the maximum value V_n, a positive overshoot appears at V_{out2} with a voltage equal to V_1 for a duration equal to t_1. While the noise is equal to the maximum value V_n (for the noise duration), V_{out2} is stable at a steady voltage as listed in Table 5.1 (V_2 is less than 5 volts). When the noise transitions from the maximum value to zero, a negative overshoot appears at V_{out2} of amplitude V_3 and duration t_2. V_{out2} becomes 5 volts when the noise becomes zero. The following observations are noted for different load capacitances at Out1 and Out2, different noise values V_n, and different k_E/k_D ratios:

- V_1 and particularly V_3 increase as the noise V_n increases. For example, for $V_n = 2$ volts, $V_1 \approx V_3$ and reaches up to 0.4 volts depending upon the capacitive load, while for $V_n = 4$ volts, V_1 reaches up to 0.7 volts and V_3 reaches up to 5 volts.
- V_1 and V_3 depend strongly on the capacitive load at Out1 (C_1) and Out2 (C_2). The values of V_1 and V_3 for different simulation conditions are listed in Table 5.3.
- As k_E/k_D increases, V_2 and V_3 increase. This relation is also dependent upon the load capacitances, C_1 and C_2. The dependencies are also listed in Table 5.3.

Cases 1, 5, and 9 listed in Table 5.3 are the most common practical situations (no significant load on any output), such as the case for the serial chain of latches in the test circuits. Cases 2, 6, and 10 characterize the situation where the output of a latch has a large fan-out. Note in Table 5.3 that an improved noise behavior is achieved as compared to situations 1, 5, and 9 (a smaller V_3). Cases 3, 7, and 11 demonstrate, as expected, that large capacitances at the output of each inverter of a latch do not benefit the noise behavior (see Figs. C.2b, C.3a, C.3b, C.5a, and C.5b). Cases 4, 8, and 12 are the most unfavorable cases for the noise behavior. However, none of the cases, 3, 4, 7, 8, 11, and 12, are commonly found in practice.

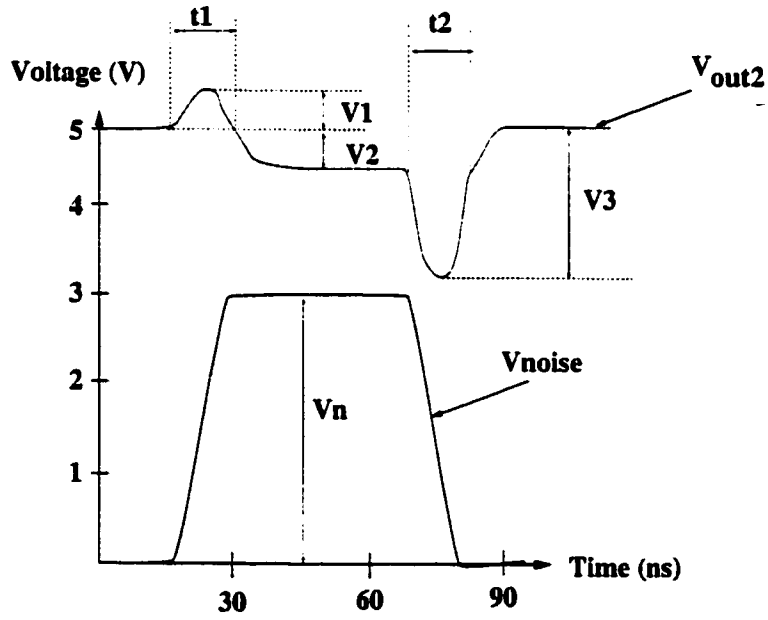


Figure 5.5: A typical Out2 waveform when the V1, V2, V3, and V4 noise voltages derived from the circuit shown in Fig. 5.4 are in-phase.

In addition to the magnitude, the duration of V_1 and particularly V_3 (t_1 and t_3, respectively) is also highly important. A large duration of V_3 returns a smaller V_{in} from V_{out2} through the feedback pass transistor, which according

to Figs. C.7a, C.7b, C.8a, and C.8b create a slower low-to-high transition at Out1. This situation permits Out2 to pull to a full low state, inducing a full parasitic transition. The duration of the V_1 and V_3 spikes depends upon issues such as the speed of the technology and the capacitive load at each node.

Table 5.3: Open loop static latch analysis for situation 1 as listed in Table 4.1.

No.	V_n (V)	k_E/k_D	C_1	C_2	V_1 (V)	V_2 (V)	V_3 (V)	t_1 (ns)	t_2 (ns)
1.	2	4	10 fF	10 fF	0.4	0	0.4	10	10
2.	2	4	10 fF	1 pF	0.05	0	0.05	10	10
3.	2	4	1 pF	1 pF	0.05	0	0.05	10	10
4.	2	4	1 pF	10 fF	0.35	0	0.55	9	18
5.	4	4	10 fF	10 fF	0.55	0.4	2	12	16
6.	4	4	10 fF	1 pF	0.2	0.3	0.6	11	45
7.	4	4	1 pF	1 pF	0.2	0	2	90	200
8.	4	4	1 pF	10 fF	0.5	0	5	12	35
9.	4	8	10 fF	10 fF	0.6	0.8	2.6	12	18
10.	4	8	10 fF	1 pF	0.2	0.6	1	15	20
11.	4	8	1 pF	1 pF	0.2	0	2	90	200
12.	4	8	1 pF	10 fF	0.6	0	5	12	35

An improved noise behavior is listed in Table 5.3 for a large C_2 when V_{in} is high. However, when V_{in} is low, Out2 is normally (in the absence of noise) low and a noise induced transition at Out2 behaves similarly to Cases 4, 8, and 12 of Table 5.3 with respect to Out1. Accordingly, an equivalent V_3 at Out1 could be significant, generating a full swing parasitic transition at Out2, which may possibly be latched. Note that due to the feedback pass transistor, situations 4, 8, and 12 are less probable for Out1 than for Out2 (Section 4.1.6), but for large durations of V_3, an incorrect signal can be latched.

Concluding, situation 1 of Table 4.1 is characterized by:

- A parasitic transition is probable only in unusual situations, such as for large substrate noise, for large capacitive loads, or for a poor design (incorrect transistor sizing).
- If both high and low output states are equally probable, an improved noise immunity is obtained for small load capacitances at Out1 and Out2.
- To reduce the duration of V_1 and V_3, large transistors (for the same k_E/k_D ratio) are desirable to obtain a fast charge/discharge of the load capacitances at each node. A ratio of $k_E/k_D = 4$ is preferable to $k_E/k_D = 8$ due to smaller values of V_2 and V_3 which translates to less sensitivity to noise at the output.
- If a high (low) output state is more probable than a low (high) state, than a larger load capacitance at Out2 (Out1) is desirable. If the circuit driven by Out2 (Out1) represents a small capacitance, this effect can be realized with a specific on-chip CMOS capacitor inserted at the respective nodes.

2. Situation 2 of Table 4.1 is characterized by the Out2 output waveform shown in Fig. 5.6. Note that a full swing parasitic transition is possible. In equilibrium (for zero noise), since V_{in} is high, V_{out2} is high (5 volts). A parasitic transition of amplitude V_a is present at Out2 when inverter1 (see Fig. 5.4) is affected by noise ($V_1 = V_2 = V_n$) and inverter2 is not affected ($V_3 = V_4 = 0$). When $V_1 = V_2 = V_3 = V_4 = V_n$, V_{out2} is equal to the steady state voltage (see Table 5.1, V_b is less than 5 volts). While $V_1 = V_2 = 0$ and $V_3 = V_4 = V_n$, V_{out2} is equal to 5 volts (since V_{out1} is low). When V_3 and V_4 return to 0, a

noise spike similar to V_3 of Fig. 5.5 but smaller in amplitude is present at Out2. V_{out2} finally returns to 5 volts when the noise is zero. The following characteristics are noted for different simulation conditions:

- The amplitude of V_a (see Fig. 5.6) depends upon the value of V_n, k_E/k_D, C_1, and C_2. These dependencies are shown in Table 5.4. Note that a large C_1 and C_2 is beneficial, since a large capacitance does not permit fast transitions at Out1 and Out2. However, a large C_1 and C_2 is beneficial for small t (which is the difference of phase between V_1-V_2, and V_3-V_4, as shown in Fig. 5.6). A large phase difference permits the parasitic transition V_a to reach full swing (from 5 volts to ground), while a small phase difference and/or a large capacitive load does not permit this full swing. Note that a small k_E/k_D ratio produces a larger V_a, while a large k_E/k_D ratio produces a smaller V_a for the same V_n, C_1, and C_2.
- For $C_1 = C_2 = 10$ fF (a practical capacitance) and $k_E/k_D = 4$, a V_n of ≈ 1.7 volts produces a V_a of ≈ 2.5 volts, which represents a significant parasitic transition.

Table 5.4: Open loop static latch analysis for situation 2 of Table 4.1

No.	V_n (V)	k_E/k_D	C_1	C_2	V_a (V)	V_b (V)	V_c (V)	t_a (ns)	t (ns)
1.	4	4	10 fF	10 fF	5	0.5	0.7	25	30
2.	4	4	1 pF	10 fF	5	0.3	0.7	20	30
3.	4	4	1 pF	1 pF	3.5	1	0.1	15	30
4.	4	4	10 fF	1 pF	5	1	0.1	15	30
5.	2.4	4	10 fF	10 fF	4.7	0	0.5	25	30
6.	1.7	4	10 fF	10 fF	2.5	0	0.5	25	30
7.	2	2	10 fF	10 fF	4.1	0.5	0.6	20	30
8.	2	8	10 fF	10 fF	1	0	0.5	25	30

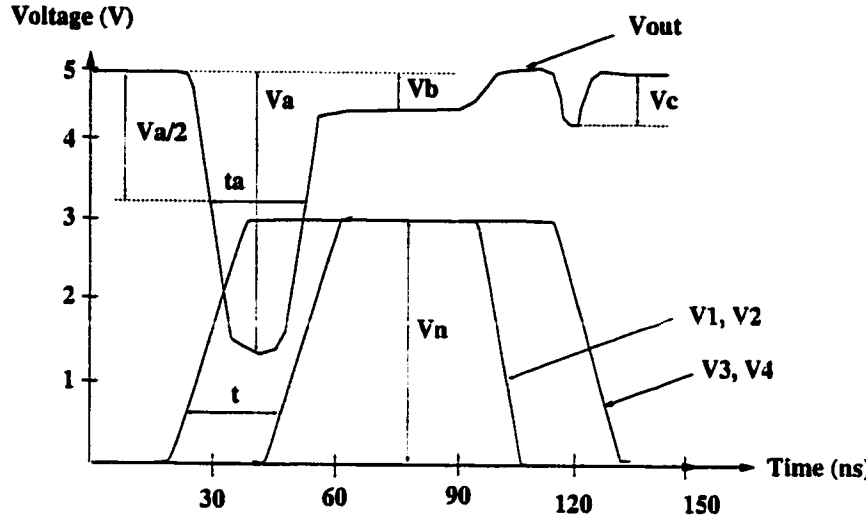


Figure 5.6: Typical Out2 waveform when the V1, V2, V3, and V4 noise voltages derived from the circuit shown in Fig. 5.4 satisfy situation 2 of Table 4.1

If V_{in} is low, in the absence of noise, Out1 is high and Out2 is low. In the presence of noise, the Out1 output waveform is shown in Fig. 5.7.

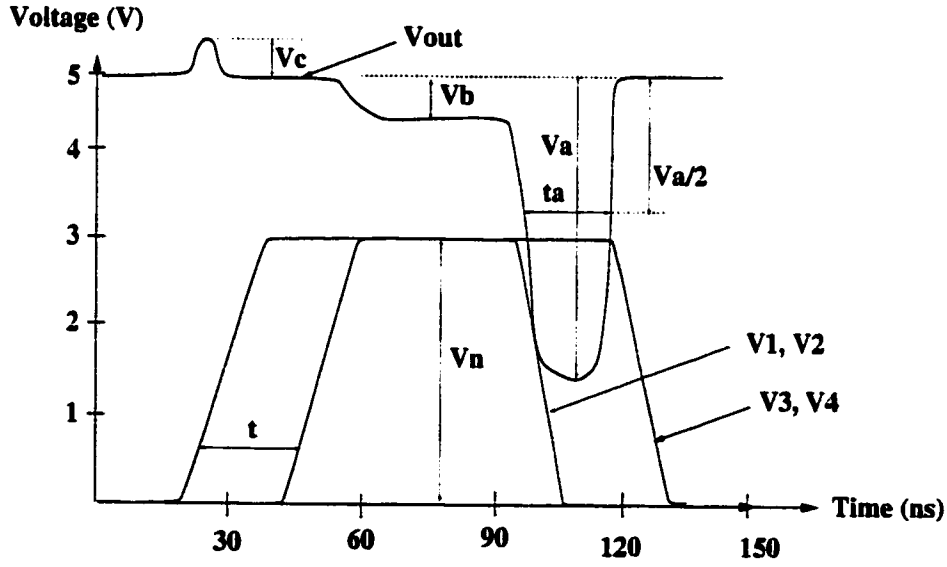


Figure 5.7: Typical Out1 waveform when the V1, V2, V3, and V4 noise voltages derived from the circuit shown in Fig. 5.4 satisfy situation 2 of Table 4.1 and V_{in} is low

Note that the latch is open loop in Figs. 5.5, 5.6, and 5.7. For a closed loop latch, a parasitic transition at Out2 is returned to the latch input through the feedback pass transistor and can be latched. Accordingly, Out2 shown in Fig 5.6 and Out1 shown in Fig. 5.7 are latched low after the V_a noise induced transition, and Out2 shown in Fig. 5.5 is latched low after the V_3 noise induced transition.

Note also that due to the feedback pass transistor (see Fig. 3.1c), latching a parasitic $Out2 = low$ ($V_{in} = high$ in Fig. 5.6) is more likely than latching a parasitic $Out2 = high$ ($V_{in} = low$ in Fig. 5.7). Latching a parasitic $Out2 = high$ necessitates a larger phase difference between the noise at inverter1 and inverter2 and a larger noise amplitude V_n, than latching a parasitic $Out2 = low$, as discussed in Section 4.1.6.

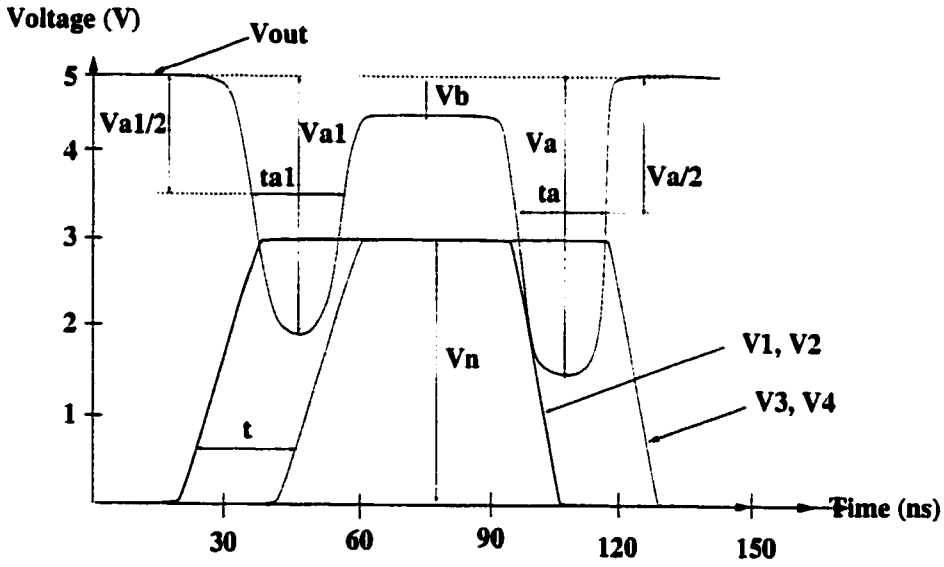


Figure 5.8: A possible Out2 waveform for $V_{in} = high$, for large noise voltages and phase differences between the noise at inverter1 and inverter2, and for the case where the V1, V2, V3, and V4 noise voltages derived from the circuit shown in Fig. 5.4 satisfy situation 2 listed in Table 4.1

Referring to Fig. 5.8, for $V_{in} = high$, note that it is possible to latch $Out2 = low$ according to Fig. 5.7 during *ta*. During *ta1*, it is possible to return to the original state and latch $Out2 = high$. However, as discussed previously, due to the asymmetric probability of latching each of the two states, a high magnitude noise pulse (V_n) with large phase differences is required for this situation to occur. The Out2 output waveform shown in Fig. 5.8 is also depicted for an open loop latch.

Concluding, situation 2 of Table 4.1 is characterized by:

- A parasitic transition will more likely be latched when a phase difference exists between the noise at inverter1 and the noise at inverter2 (see Fig. 5.4).
- An oscillation between the high and low output states of a latch is possible for $V_{in} = high$ and when a large noise amplitude V_n with large phase differences between the noise at inverter1 and inverter2 of a latch (Fig. 5.4) is present throughout the substrate.
- Large load capacitances for both inverters of a latch (case 3 listed in Table 5.4) improve the noise behavior of a latch. However, the presence of large load capacitances is not favorable when the noise for the two inverters is in-phase, as listed in Table 5.3.
- The $k_E/k_D = 8$ case offers improved noise behavior as compared to $k_E/k_D = 4$, which is better than $k_E/k_D = 2$ (see Table 5.4). Note that if the noise is in-phase (Table 5.3), $k_E/k_D = 4$ is preferred over $k_E/k_D = 8$. Design tradeoffs depending upon the estimated substrate noise are possible. These tradeoffs permit the size of the transistors in the logic blocks and/or the capacitive loading at the outputs of the

logic elements to be optimized, both with the objective to minimize the noise sensitivity of the digital circuits.

3. Situation 3 of Table 4.1 is equivalent to situation 1 as discussed above. Furthermore, each inverter injects noise into the substrate when $V_2 = V_4 = V_n$ and $V_1 = V_3 = 0$ as described in Section 5.1 (see Figs. C.6a and C.6b).

4. Situation 4 of Table 4.1 is equivalent to situation 1 as discussed above. Furthermore, each inverter injects noise into the substrate when $V_2 = V_4 = V_n$ and $V_1 = V_3 = 0$ as described in Section 5.1 (see Fig. C.4a).

5. Situation 5a, 5b, or 5c is equivalent to situation 2 as discussed above. Each inverter injects noise into the substrate as discussed for situation 3.

6. Situation 6a, 6b, or 6c is equivalent to situation 2 as discussed above. Each inverter injects noise into the substrate as discussed for situation 4.

7. The C and D noise input cases are similar to the A and B noise input cases (5 and 6). However, note that for both the C and D noise input cases, inverter2 (see Figs. 3.1c and 5.4) is affected first.

   - If $V_{in} = low$, $Out1 = high$, and the Out1 output waveform appears as shown in Fig. 5.7. If V_a has a sufficient amplitude and the noise between inverter2 and inverter1 has a sufficiently large phase difference (as discussed for $V_{in} = low$ for situation2), then a latched transition through inverter2 during *t1* (see Fig. 5.9) for the closed-loop latch can be induced.

     As a result, V_{in} becomes *high*. As shown for situation 2, the $V_{in} = high$ case is more sensitive to noise than the $V_{in} = low$ case. Since the

noise conditions are such that a parasitic transition can be latched for $V_{in} = low$ at *t1*, there is a high probability that the noise will return the state of Out2 back to *low* during *t2* through inverter1. If the noise conditions are such that during *t1* a parasitic transition cannot be induced, then during *t2* a parasitic transition can also not be induced since $V_{in} = low$ (see Section 5.1). Accordingly, if $V_{in} = low$ and the noise input at the latch (see Fig. 5.4) is C or D, Out2 will likely remain unchanged (*low*), either by switching *high* during *t1* and back to *low* during *t2*, or by not changing at all.

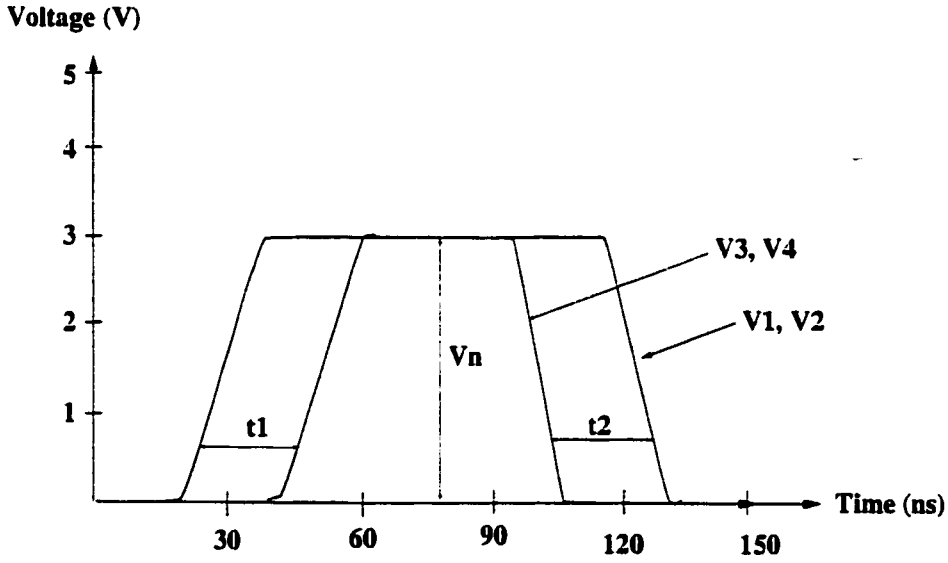


Figure 5.9: The noise waveforms at inverter2 and inverter1 shown in Fig. 5.4 where the noise inputs are nodes C or D

- If $V_{in} = high$, during *t1*, inverter2 cannot be affected since the input is *low*. During *t2*, inverter1 is affected and Out2 may parasitically switch.

It is demonstrated that for the C and D noise inputs, a latch is also more likely to be affected by noise when $V_{in} = high$.

Concluding, it has been demonstrated in this section by a variety of comprehensive circuit simulations that the noise behavior of a latch composed of two inverters as shown in Fig. 3.1c can be characterized by two primary situations,

- the noise for the two inverters is in-phase,
- the noise for the two inverters is not in-phase.

Each situation has been fully characterized and compared. The noise sensitivity for a latch as shown in Fig. 3.1c for $V_{in} = high$ and $V_{in} = low$ is analyzed and specific conclusions are drawn. Summarizing, the influence of the amplitude of the substrate noise, the phase difference between the noise signal at the two inverters, the noise duration, the transistor size, and the capacitive loading of each inverter on the sensitivity of a latch to noise is analyzed and discussed in this chapter.

Chapter 6

NMOS Experimental Data

Fifty test circuits have been designed and fabricated in a 3.5 μm NMOS technology. The issues chosen for investigation in these circuits, as well as the test strategy and the test plan, have been presented in Chapter 3. The experimental results gathered from the measurements of the test circuits are presented in this chapter. In presenting the data, the emphasis is placed on illustrating the effects of each of the analyzed issues, on comparing the results with the expected behavior as described in Chapters 2, 3, and 5, and on discussing possible noise mitigation techniques.

As described in Chapter 5, the difference of phase between the noise affecting different transistors has a significant importance on the noise immunity of the on-chip sensitive registers. Several test chips have been fabricated to experimentally determine the principal characteristics of the noise generation process within the substrate for these NMOS circuits such as the substrate noise amplitude and difference of phase throughout the substrate, and to sample characteristic substrate noise waveforms. The results obtained from the analysis of these test chips are discussed in Section 6.1 in connection with the operation of the power drivers. These results are important for better understanding the nature and origin of

the mechanisms that generate the substrate noise which affect the logic registers, while also increasing insight into the results obtained for each of the analyzed issues (see Section 3.4). In Section 6.2, the data for each of the analyzed issues are presented, the principal effects are noted, and any discussions and explanations are provided. To experimentally demonstrate the connection between the substrate noise waveforms determined in Section 6.1 and the number of affected registers as a function of different issues as determined in Section 6.2, the number of registers that are affected in correlation to the R_{test} waveform (the substrate noise waveform) is described in Section 6.3. This dependency has been theoretically described in Chapter 4. Finally, several noise mitigation techniques based on the models, simulations, and experimental data are presented in Section 6.4.

6.1 Characterization of the substrate noise waveforms

The test results obtained from the experimental analysis of the circuits from group 4 (see Section 3.2) are described in this section. The principal objective of the experimental analysis of this group of circuits is to determine the substrate noise waveforms in the analyzed NMOS circuits, the phase difference for the noise waveforms at different substrate points, and the typical amplitude of the substrate noise throughout the substrate. Another important objective is to determine methods to decrease the noise level in the substrate, influence the substrate noise waveforms (see Sections 6.1.5 and 6.1.6), and to determine the mechanisms in which the power drivers generate substrate noise.

A typical noise waveform as reported in the literature [69–73] (see Fig. 2.5) for a *digital influencing analog* type of application is discussed in Section 6.1.1. Also in Section 6.1.1 it is noted, that to the author's knowledge, it has not been reported in the literature which region of operation of a switching transistor is the region where the noise is generated. This aspect is important for the present application, since an active power NMOS transistor is required to operate in the linear region. The effects of substrate noise and ground bounce can easily shift the operating point of the power transistor into the saturation region (see Sections 6.1.4 and 6.1.5). Accordingly, it is important to determine which region of operation the maximum amount of noise is generated. A brief review of the specific characteristics of the test circuits is provided in Section 6.1.2. Experimental substrate noise waveforms derived under different test conditions are shown in Section 6.1.3. To determine the relation between the observed substrate noise waveforms and the region of operation of the power driver, V_{DS} across the power driver is observed and correlated with the substrate noise waveforms. The observed substrate noise waveforms are explained by analyzing the circuit schematic and the physical layout of the test circuit in Section 6.1.4. The dependence of the substrate noise waveform on the power supply voltage, the number of active power drivers, the routing of the ground lines, the placement of the power driver, and the placement of the substrate contacts are discussed in Section 6.1.5. The consequence of an oscillatory noise waveform on the noise immunity of the digital circuits is discussed in Section 6.1.6. Experimental circuits that obtain non-oscillatory substrate noise waveforms are described, highlighting their disadvantages together with solutions to minimize these disadvantages.

6.1.1 Issues related to substrate noise waveforms

The effect of the substrate noise generated by the switching of the digital blocks on the output of a current source, observed in a *digital influencing analog* type of application, is shown in Fig 2.5. The noise waveform, at the output of the current source, has been discussed in the literature [69–71] (see Section 2.4). Note in Fig. 2.5 that the noise is present at the output of the current source only when the digital blocks switch. Accordingly, the noise is present within the substrate only when the digital circuitry is switching. The noise becomes zero after a settling time once the switching is completed. The digital blocks that generate the noise in [69–71] are CMOS. For the low-to-high or the high-to-low transition at the input of a CMOS inverter, either the NMOS transistor or the PMOS transistor switches from saturation to linear to cut-off, while the other transistor switches from cut-off to linear to saturation, generating the substrate noise. Between transitions, no current flows from V_{DD} to GND in static CMOS digital circuitry. Note that for a CMOS logic circuit it is not important to determine in which region of operation of the transistor the noise is generated, since when one transistor is linear, the other transistor is saturated. Also, the absence of noise between transitions can be attributed to there not being any current flow in the CMOS circuits between transitions.

The NMOS transistor of the power driver used in the present application (see Fig. 3.1a) is cut-off if the input is low, switches from cut-off to saturation to linear when the input switches low-to-high, and is required to be linear when the input is high. As shown in Chapter 3, to efficiently drive this high voltage and high current power driver, a 13 volt predriver is used as an interface between the 5 volt logic circuitry and the 38 volt power driver [95]. The objective is to provide

a sufficient voltage swing on the gate of the NMOS power transistor to obtain a low V_{DS} across the power transistor. A low V_{DS} is important to minimize the power dissipated by the NMOS power transistor while on, since a large current flows from V_{DD} to GND. A large V_{DS} would dissipate a power according to

$$P = V_{DS} I_{DS}. \tag{6.1}$$

Note that obtaining a low V_{DS} across the power NMOS transistor depends upon the value of V_{GS} and the value of the load resistor R (see Fig. 3.1a). While R and V_{GS} are optimized by design for normal operating conditions, V_{GS} may vary due to the substrate noise, producing variations in V_{DS} and inducing undesirable effects (as described in the following sections). Accordingly, for the present application, it is important to determine which region the power transistor operates in during the time when the maximum amount of noise is generated, and, if possible, to develop solutions to operate the transistor in that region of operation for the least amount of time. Also, it is important to determine the typical characteristics of the substrate noise waveforms in each of the two regions of operation of the power transistor in order to understand and explain the effects produced by the generated noise in each of the two regions of operation of the power transistor. As shown above, the substrate noise waveforms reported in the literature are obtained for a CMOS noise source, and, as described, the region of operation of the noise source is not important.

6.1.2 Circuit and physical design aspects of the test circuits

The floorplan shown in Fig. 3.3d is representative of the group4 circuits. The generated substrate noise may affect the sensitive registers as well as any registers

present in the logic blocks that select the power drivers. If a register in the *select logic* block is affected, the power driver that generates noise may be erroneously turned off, and the substrate noise waveform will be erroneously observed. Since the observance of a correct noise waveform is an important objective for this part of the research, this uncertainty is eliminated by not including any registers in the *select logic* blocks. The cost is an increase in the number of pads necessary to select the power drivers.

As described in Section 3.2, the *substrate lines monitoring the substrate voltage* block consists of 14 equally distant metal lines, increasingly distant from the power drivers in the order from line 1 (the closest to the power drivers) to line 14. Each metal line is connected to the substrate through substrate contacts and is also connected to a dedicated pin to monitor the substrate noise waveform of the respective metal line. Two of the eight power drivers (see Figs. 3.1a and 3.3d) monitor V_{DS} across the power driver transistor through dedicated pads. The signals at the metal lines 1 to 14 are called *line1* to *line14*, while the signals at V_{DS} of the two power driver transistors are called R_{test-l} and R_{test-r} or simply R_{test} or V_{DS} if no distinction between R_{test-l} and R_{test-r} is necessary. These signals are measured with respect to the sources of the power drivers which is the reference GND point.

6.1.3 Experimentally derived substrate noise waveforms

An interesting experimentally observed effect is shown in Fig. 6.1. The power driver transistor, operating in the linear region, generates an approximately constant substrate noise level that biases the substrate continuously over the duration for which the power driver is on. The substrate bias level increases as the current

through the power driver increases, and as the distance from the power driver to the line that monitors the substrate noise increases. The effect of a 6 mA current, corresponding to a power supply of 4 volts, is shown in Fig. 6.1. V_{DS} across the power transistor for this situation is $\approx$ 1.5 volts. The substrate bias measured for line2 is equal to $\approx$ 700 mV, while for line14, farther from the noise source, is $\approx$ 900 mV. These values are obtained when eight power drivers are active.

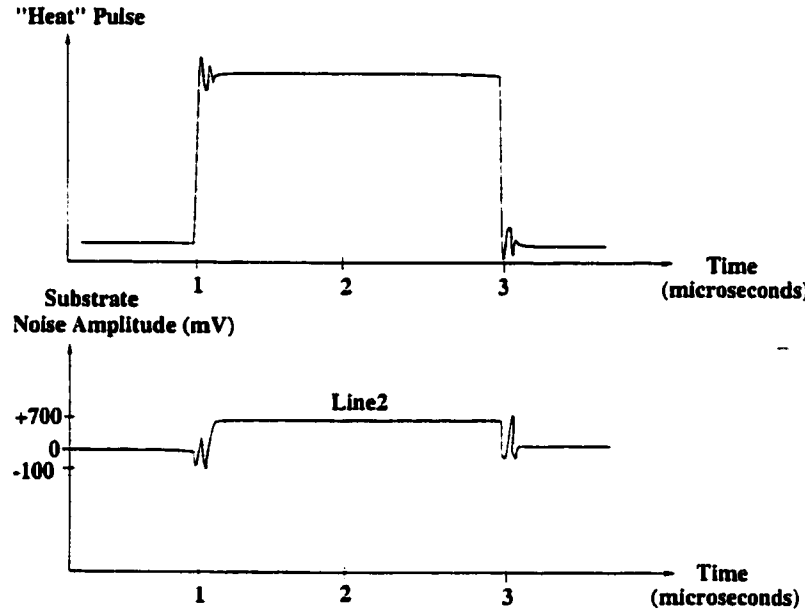


Figure 6.1: The substrate bias generated by a power transistor operating in the linear region

The noise generated in the substrate by the switching of the 13 volt circuitry while all the power drivers are off is shown in Fig. 6.2. The noise spikes reach an amplitude of +/− 200 mV for line2, while for line14 this amplitude is +/− 400 mV. No constant substrate noise bias is detected due to the low level of current through the on NMOS inverter. Accordingly, the substrate noise generated by the 13 volt logic is as predicted by Fig. 2.5, the substrate noise being observed only during transitions.

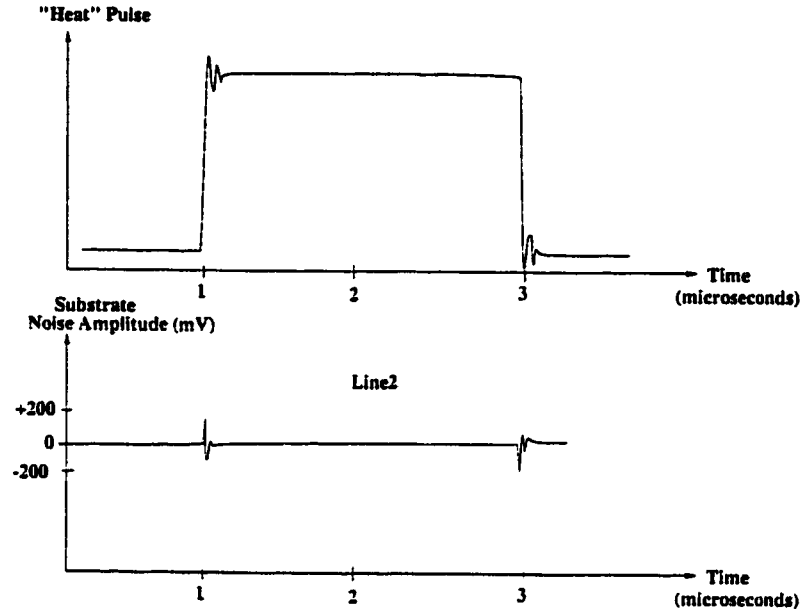


Figure 6.2: The substrate bias generated by the switching of the 13 volt logic circuitry.

For large power driver power supplies (larger than 6 volts), an interesting effect is noted as exemplified in Fig. 6.3. The substrate noise amplitude oscillates around the approximately constant noise level as shown in Fig. 6.1. This oscillation is related to the V_{DS} variations of the power driver transistor as shown in Fig. 6.3. In Fig. 6.3, the power supply voltage of the power driver is 34 V (the V level). The substrate noise varies between $V_a = 4$ volts and $V_b = -3.2$ volts, while V_{DS} varies between $V_1 = 62$ volts and $V_2 = 12$ volts. Note the overshoots in V_{DS} ranging up to more than 60 volts. Undershoots up to -800 mV have also been observed. While these values are measured for line2, the same values are within 15% for each of the fourteen lines. A difference in phase of up to 80 ns is noted between the noise waveforms for any two lines. Eight power drivers are active.

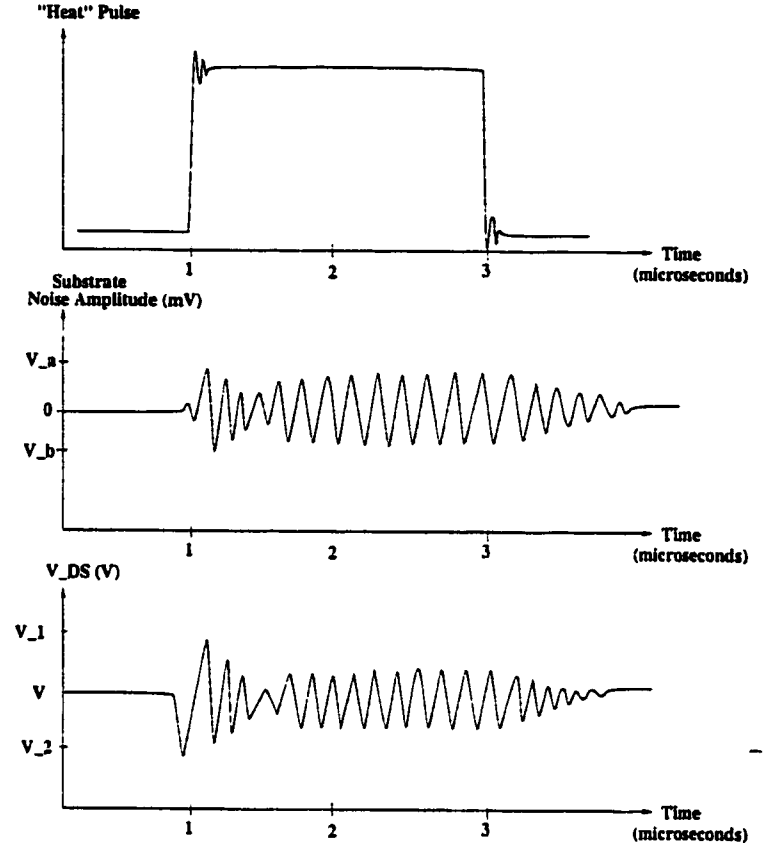


Figure 6.3: Oscillation of the substrate bias in relation to the V_{DS} variations across the power driver transistor.

Note that the substrate noise waveforms generated by a power driver and controlled by a predriver, with the circuit schematics of the power driver and of the predriver as shown in Fig. 3.1, are characterized by a steady state value superimposed over an oscillation. All of these waveforms are correlated with the saturation and linear regions of operation of the power transistor and with the V_{DS} variations across the power transistor. From Figs. 6.1, 6.2, and 6.3, it can be concluded that a linear transistor generates a constant substrate bias that, according to Chapter 5, does not affect the noise immunity of the digital circuits. It can also be concluded that important noise spikes with large phase differences

throughout the substrate are produced when the power transistor transitions from the linear region to the saturation saturation and from the saturation region to the linear region. No conclusion is obtained regarding the noise generated by the power transistor while operating in the saturation region since the power transistor can not remain saturated for a sufficient amount of time for a clear determination. Accordingly, the linear-to-saturated and saturated-to-linear transitions of the power driver should be reduced to a minimum to improve the noise behavior of the digital circuits.

6.1.4 Theoretical aspects for the observed substrate noise waveforms

To better explain the observed substrate noise waveforms that are generated by the power driver, the circuit shown in Fig. 6.4 is used. A predriver connected to a power driver is depicted. As described in Chapter 3, substrate contacts are present in the vicinity of the power drivers, connecting the sources of the power drivers to the substrate. Due to physical placement constraints, the ground of the predriver is a long metal line that connects to the high power ground line. The high power ground line is then connected to a pad.

Due to these circuit and physical design aspects, the following effects are created:

- An initial positive substrate noise spike generated during an initial transition reaches the source of the power drivers.
- The initial V_{GS} at the input of the power driver transistor is reduced by the magnitude of the positive noise spike.

- A decrease in V_{GS} creates a decrease in I_{DS} and an increase in V_{DS} which shifts the power transistor from the linear region into the saturation region.

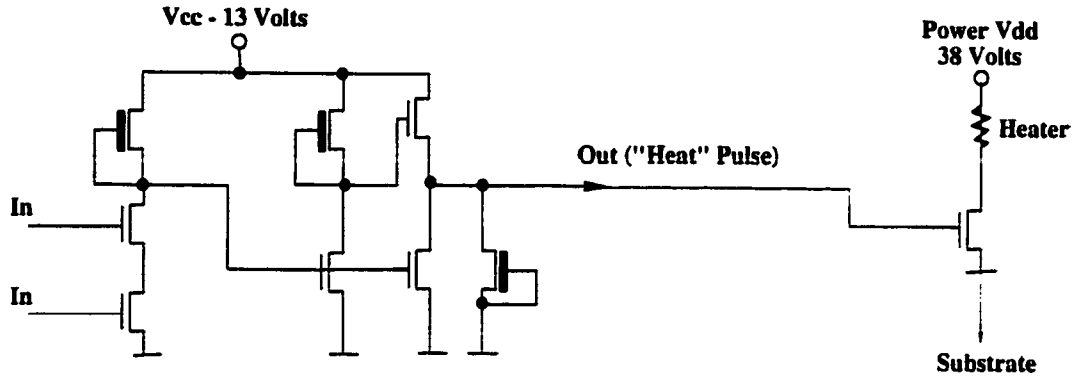


Figure 6.4: The predriver-driver circuit that is used to describe the shape of the substrate noise waveforms

These aspects are modeled by the equivalent circuit schematic shown in Fig. 6.5, where the V_{noise} voltage source models the noise induced V_{GS} variations which are responsible for the experimentally observed V_{DS} variations. The effect of V_{noise} as well as the relation to the V_{DS} variations can be modeled by the equations,

$$I_{DS} = K\frac{W}{L}[(V_{GS} - V_T - V_{noise})V_{DS} - \frac{V_{DS}^2}{2}], \tag{6.2}$$

and

$$I_{DS} = K\frac{W}{L}(V_{GS} - V_T - V_{noise})^2(1 + \lambda V_{DS}). \tag{6.3}$$

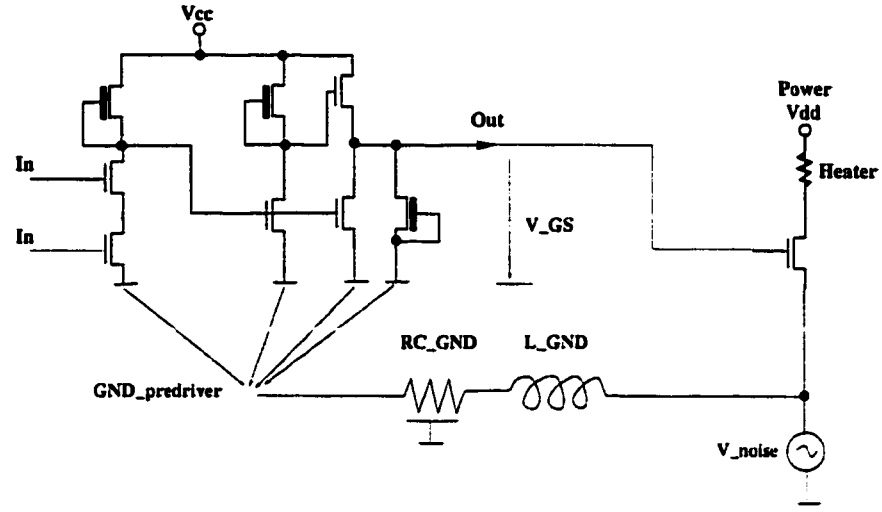


Figure 6.5: The equivalent schematic of the predriver-driver circuit that models the substrate noise

Based on Fig. 6.5, (6.2), and (6.3), the noise generation process can be characterized by the following statements:

- Decreasing V_{GS} and increasing V_{DS} is equivalent to turning off the power transistor.
- Accordingly, the amount of generated noise decreases, decreasing V_{noise}, increasing I_{DS} according to (6.2), and returning the transistor from the saturation region to the linear region and to a small V_{DS}.
- This situation generates a large amount of noise as in the initial phase. This cycle, where the power transistor switches from the linear region to the saturation region and back to the linear region, repeats until the predriver signal turns off and V_{GS} becomes zero.
- The oscillation remains present while decreasing in amplitude after the predriver signal turns off. These decreasing oscillations are called herein

tails. This behavior is explained by the fact that V_{noise} of (6.2) is sufficiently large to act as a bias for the power transistor. V_{noise} decreases in amplitude with each cycle until the oscillations completely disappear.

6.1.5 Observed dependencies of the substrate noise waveforms

The substrate noise waveform characteristics are shown here to depend on a number of issues. These variations have been experimentally observed and are presented below.

By decreasing the power supply voltage from 34 volts to 4 volts, the following effects are noted:

- The frequency and the amplitude of the oscillation, as shown in Fig. 6.3, decrease.
- The oscillation begins when the power supply exceeds 6 volts.
- The time during which the oscillation occurs after the predriver signal turns off decreases.

The approximately constant substrate bias observed for low supply voltages is due to the equilibrium among V_{GS}, V_{DS}, V_{noise}, and I_{DS} (see Section 6.1.4) that is reached after the initial noise (V_{noise}) generation. Experimental data also show that the same effects obtained for the case when the power supply decreases are also obtained for the case when the number of active power drivers decreases. For example, the oscillation is first noted when the power supply reaches 6 volts when eight drivers are active, at 8 volts for five drivers, at 12 volts for three drivers, while for one driver there are negligible oscillations even at 34 volts.

Experimental data also shows that

- Due to the high switched currents, any voltage drop on the metal lines is significant, creating ground bounce and/or substrate voltage nonuniformities that are interpreted as V_{noise} voltages by different power drivers (see (6.2) and Fig. 6.5).

- If the circuit contains more than one group of power drivers, the group closest to the pads (see Fig. 3.3) is the most sensitive to V_{noise} effects, and produces the substrate noise waveforms with the largest oscillation amplitude.

Experiments characterizing the effects on noise reduction due to the presence of substrate contacts in different points of the substrate have been performed. To analyze this aspect, any of the fourteen metal lines (connected to the substrate) have been connected to the sources of the power transistors through a low resistivity contact, while the noise is observed at any of the other unconnected metal lines. The conclusions can be summarized as:

- The noise level is reduced by up to 400% if the line that monitors the noise is adjacent to a line that is grounded (17 μm distance).

- The noise reduction decreases in efficiency as the distance between the monitor line and the grounded line increases.

- If the distance between the monitor line and the grounded line is more than 70 μm (four lines), almost no reduction in noise is noted.

6.1.6 Conclusions and solutions

As described in Chapter 4, digital circuits in general and in particular the analyzed NMOS circuits are affected by substrate noise primarily through positive

substrate noise transients. The principal mechanism for affecting a digital circuit has been shown to be the existence of a phase difference between the noise received by the different transistors of the circuit.

Consider two transistors affected by a noise waveform at a difference of phase T. Two situations for the shape of the noise waveform are considered as shown in Fig. 6.6.

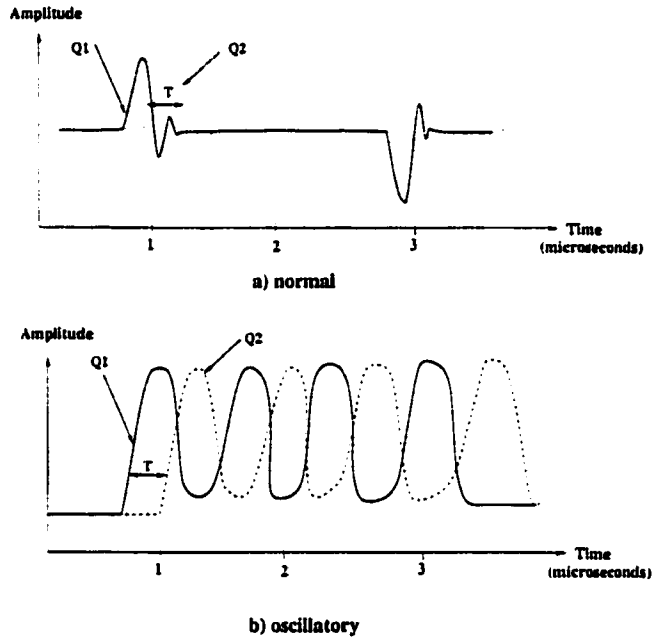


Figure 6.6: Two examples of noise waveforms affecting two transistors of a logic element a) normal b) oscillatory

For the normal noise waveform shape there are four moments when a difference of phase is noted between the noise affecting transistor Q1 and the noise affecting transistor Q2. For the oscillatory waveform, in this example, there are eight time points when a difference of phase is noted between the noise affecting the two transistors. The probability a logic element is affected by noise increases for the oscillatory waveform, and as the frequency of oscillations increases.

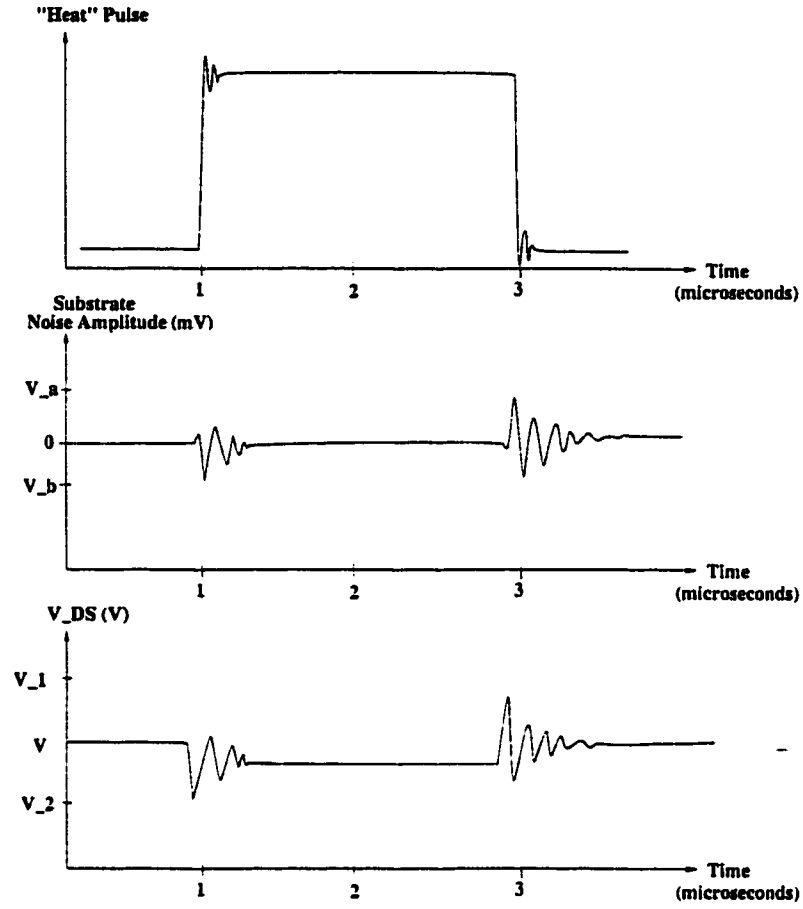


Figure 6.7: The substrate bias oscillation in relation to the V_{DS} variations of the power driver transistor for the circuits with no substrate contacts attached to the power transistors

The following circuits have been designed to eliminate the oscillatory substrate noise waveform. For these circuits, the substrate contacts in the vicinity of the power drivers (see Fig. 3.4b) have been eliminated. These circuits do not have the substrate connected near the sources of the power drivers as shown in Fig. 6.4. This absence of a substrate contact eliminates the influence of V_{noise} on the V_{GS} of the power transistor as shown by (6.2) and in Fig. 6.5. Accordingly, for these circuits, no substrate noise oscillation should be obtained.

Experimental results depict a typical substrate noise waveform for these circuits as shown in Fig. 6.7. The ranges of V_a, V_b, V_1, and V_2 are approximately similar to those shown in Fig. 6.3. Also, the amplitude and the "tail" time (for both tails) are demonstrated to decrease as the supply voltage and/or number of active drivers decreases, or with the presence of substrate contacts in the vicinity of the monitor line.

Note the major differences for the generated noise by the power transistors for these circuits, such as:

- A non-oscillatory substrate waveform
- The tails exist for a much shorter period of time
- There is no observable steady state noise for the duration of the driver turn-on pulse
- For the rising edge of the turn-on pulse, negative substrate noise is primarily generated, while for the falling edge both positive and negative noise is present equally. Accordingly, for these circuits the positive noise does not dominate as shown in the previous case.

All of these notable advantages, however, have as major drawbacks that the absence of substrate contacts for the power driver creates reliability problems for the power transistor, and, as shown by the experimental data, particularly produces a smaller V_{DS} voltage swing. Accordingly, while this solution is not practically feasible, the approach demonstrates the possibility of changing the shape of the substrate waveform. An alternative solution which is practically feasible while maintaining the aforementioned beneficial effects, is to strap the ground of the power transistors and the ground of the predriver with a low resistivity metal

while substrate contacts are included for at least the power driver but preferably also for the predriver (see Fig. 6.4). In this way, the influence of V_{noise} on the V_{GS} of the power transistor is reduced to a minimum by the low resistivity metal strap.

6.2 High level results

The experimental data characterizing the importance of each of the issues discussed in Chapter 3 and chosen for the test plan is presented and discussed in this section. All the results presented here are in terms of the *number of affected registers*, as compared to Section 6.1 where the results are presented in terms of the amplitude of the substrate noise. While the noise amplitude and the shape of the noise waveform are important in order to understand the mechanisms in which the registers are affected by noise, it is of interest to determine the sensitivity of the registers to noise.

6.2.1 Data signal conditioning

Experimental data confirm the simulation results described in Chapter 5 and the circuit considerations discussed in Chapter 3 regarding the appearance of a parasitic transition at the output of a logic element as a function of data conditioning. The following experiments have been performed to emulate and demonstrate the results of Chapter 3 and Chapter 5: both static and dynamic master-slave sensitive registers are loaded with a "1" or "0"; once the registers are loaded with data, a significant noise is generated by the power drivers; the final data residing in the registers are analyzed after the noise signal returns to zero. The conclusions are:

- For a static register, a parasitic transition is induced only when the registers are initially loaded with a "1". No parasitic transition can be induced when the registers contain a "0" data signal.

- For a dynamic register, a parasitic transition can be induced when the registers are loaded with a "1" as well as when the registers are loaded with a "0". However, the probability of inducing a parasitic transition when the registers are loaded with a "0" is higher than the probability of inducing a parasitic transition when the registers are loaded with a "1".

Therefore, in all of the remaining experiments unless otherwise specified, the static registers are loaded with a "1" and the dynamic registers are loaded with a "0".

6.2.2 Clock signal conditioning

Experimental data confirm the simulation results described in Chapter 5 and the circuit issues discussed in Chapter 3 regarding the conditioning of a parasitic transition at the output of a logic element by the register clock. To experimentally demonstrate the dependency of the parasitic transition on the clock signal conditioning of the register, both static and dynamic registers are clocked according to the timing regimes shown in Fig. 6.8. The clocking regimes shown in Fig. 6.8 satisfy two objectives:

- To verify the conclusions derived from the circuit and simulations analysis, such as the different behavior to noise of the master as compared to the slave latch depending on the nature of the clocking regime.

- To determine the behavior of the registers to the noise generated by turning on the power driver transistor (the rising edge of the driver pulse, which is

the pulse derived from the output of the predriver to the gate of the power transistor, as shown in Fig. 6.4), and to the noise generated by the power driver transistor turn-off (the falling edge of the driver pulse), as well as the relationship of the noise generated in these two cases to the clocking of the register.

As shown in Fig. 6.8, eight clocking regimes are defined:

- For clocking regime 1, clock is "0" for both the rising and falling edges of the driver pulse.
- For clocking regime 2, clock is "1" for the rising edge and "0" for the falling edge of the driver pulse.
- For clocking regime 3, clock is "0" for the rising edge and "1" for the falling edge of the driver pulse.
- For clocking regime 4, clock is "1" for both the rising and falling edges of the driver pulse.
- Clocking regime 5 is similar to clocking regime 4 with the difference that the effect of a "0" clock in-between transitions is integrated in the analysis.
- Clocking regime 6 is similar to clocking regime 1 with the difference that the effect of a "1" clock in-between transitions is integrated in the analysis.
- Clocking regime 7 is similar to clocking regime 4 with the difference that the effect of larger set-up and hold times are integrated in the analysis.
- Clocking regime 8 considers the effect of different set-up and hold times for any of the 1 to 4 clocking regimes.

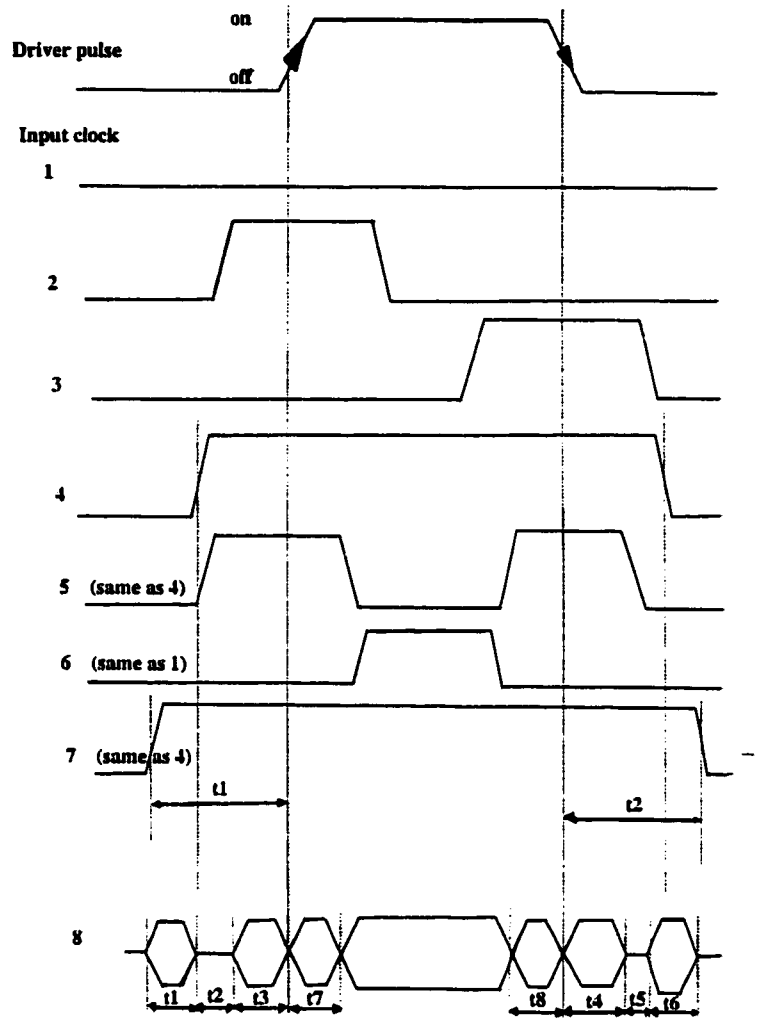


Figure 6.8: The relationship between the external input clock signal (the clock phases) and the driver on-time. Different clocking regimes for these circuits are generated

The noise behavior of both static and dynamic registers has been analyzed for each of these clocking regimes and the following conclusions drawn, as shown in Fig. 6.9:

- For static registers, the noise behavior is best for clocking regime 4 and degrades for clocking regime 3, 2, and 1 in this order. For clocking regime 5, the noise behavior is similar to the behavior noted for clocking regime

4, and clocking regime 6 is similar to clocking regime 1. The behavior of clocking regimes, 7 and 8, depending upon the set-up and hold times, can be the same as any of the 1 to 4 clocking regimes.

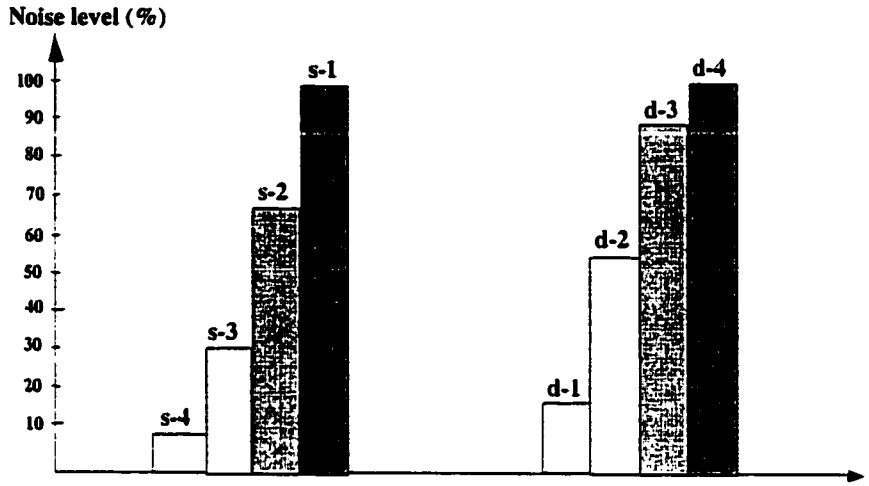


Figure 6.9: The noise tolerance as a function of clocking regime for static and dynamic registers. s=static, d=dynamic, and 1, 2, 3, 4 are the clocking regimes. The s-1 and d-4 represent the 100% noise level and is relative to each other. The d-4 dynamic registers level is $\approx$ 1.3X larger than the s-1 static register level.

- For dynamic registers, the noise behavior is best for clocking regime 1 and degrades for clocking regime 2, 3, and 4 in this order. For clocking regime 5, the noise behavior is similar to the behavior noted for clocking regime 4, and clocking regime 6 is similar to clocking regime 1. The behavior of clocking regimes, 7 and 8, depending upon the set-up and hold times, can be the same as any of the 1 to 4 clocking regimes.

6.2.3 Distance

Multiple aspects characterizing the influence of the distance between the noise source and the noise receptor are discussed in Chapters 3 and 4. In Section 6.1, it is shown that the noise waveforms are approximately constant over all of the substrate for this application.

The experimental data characterizing the influence of distance for the static and dynamic registers are shown in Fig. 6.10. Two distances, 350 μm and 500 μm, are shown, however, the full range of distances (see Chapter 3) was studied experimentally. Note the weak dependence of the register sensitivity to noise as a function of distance. No significant sensitivity is noted for large distances. Actually, the investigation of the influence of distance includes the effects of substrate thickness, substrate doping, and other process variables as discussed in Chapter 3.

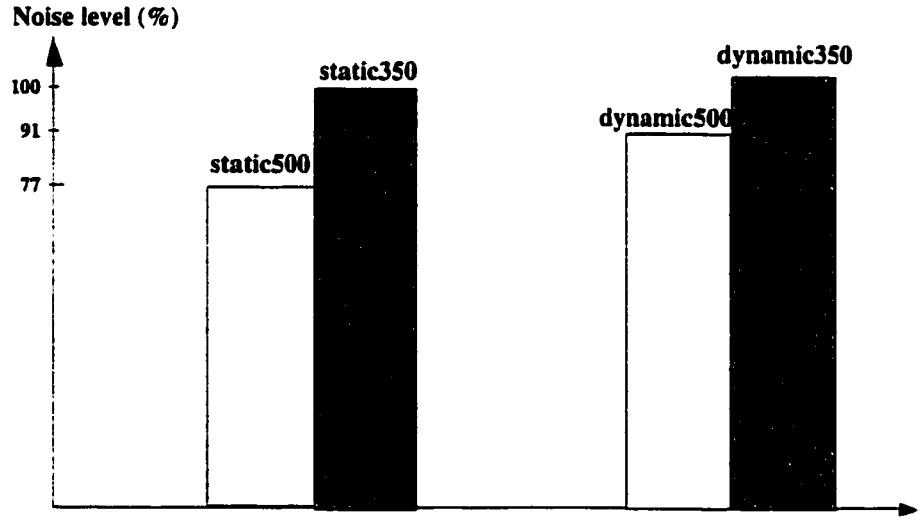


Figure 6.10: The dependence of the received noise on physical separation for static and dynamic registers. Two distances, 350 μm and 500 μm, are shown. The static350 and dynamic350 represent the 100% noise level and is relative to each other. The dynamic350 dynamic register noise level is $\approx$ 1.15X larger than the static350 static register level.

6.2.4 Placement of substrate contacts and other layout aspects

The results of this research as described in Chapter 4 and Section 6.1 demonstrate the importance of the placement of the substrate contacts, as well as the importance of a proper physical layout design. The experimental results for the test circuits demonstrate that the placement of the substrate contacts and the physical design have a major influence on the primary noise issues such as the:

- Phase difference between the noise affecting different on-chip transistors.
- Noise magnitude at different points of the substrate.
- Generation of an oscillatory substrate noise waveform.

6.2.5 Power transistor turn-on/turn-off times

The experimental results demonstrate that fast transition times for the pulse signal that turns on and off the driver (see Fig. 6.4) generate significant overshoots and undershoots for the V_{DS} across the power transistors, generating significant substrate noise. These effects, together with the current crowding effect mentioned in Chapter 3 and ground bouncing effects, are shown to produce reliability problems in the power driver transistors such as voltage breakdown and junction short-circuits.

6.2.6 Position and orientation of the sensitive registers

Several aspects related primarily to the noise phase distribution among the different transistors of a logic element as well as through the substrate, as a

function of the distance between the noise source and the noise receptor (see Chapter 4), are experimentally demonstrated in this section.

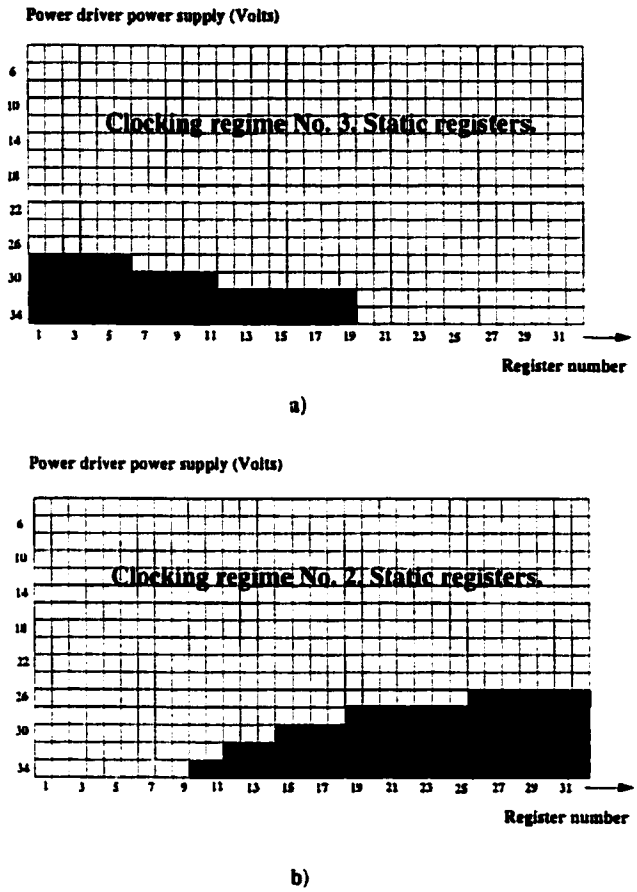


Figure 6.11: Noise tolerance in terms of the affected register location as a function of power driver voltage, substrate bias, clocking regime, ground bias, and active power driver group. Group 2 is active. The black shaded area represents the affected registers. a) Static registers, clocking regime No. 3. b) Static registers, clocking regime No. 2.

It is experimentally shown that different registers are affected depending on the position and orientation with respect to the group of active power drivers. For example, the situation when the drivers from group2 are active is shown in Fig. 6.11 for clocking regimes 2 and 3.

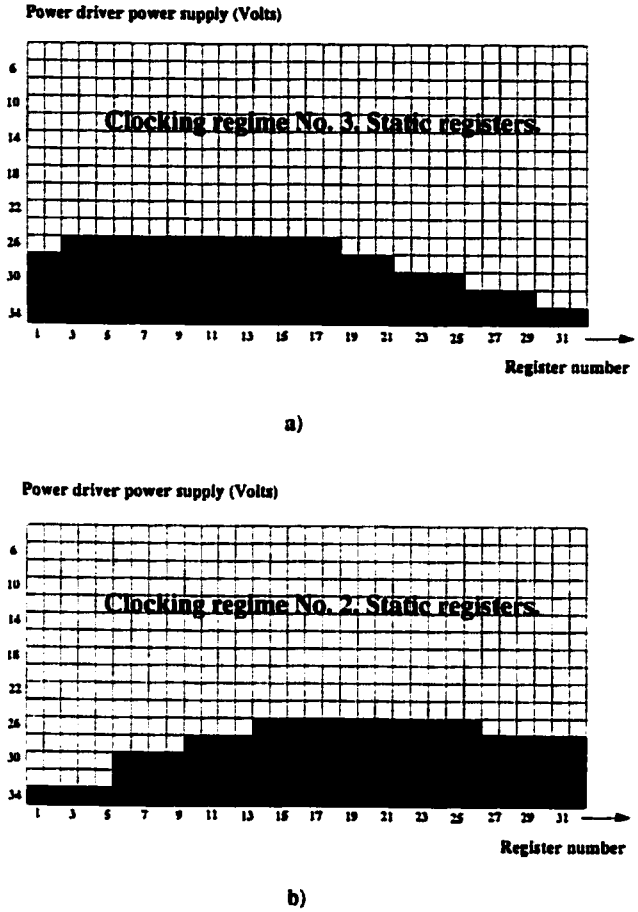


Figure 6.12: Noise tolerance affecting register location as a function of power driver voltage, substrate bias, clocking regime, ground bias, and active power driver group. Group 5 is active. The black shaded area represents the affected registers. a) Static registers, clocking regime No. 3. b) Static registers, clocking regime No. 2.

The situation when the drivers from group5 are active is shown in Fig. 6.12. Test results demonstrate that the more the active group of drivers is to the right of the chip (see Fig. 3.3a), the impact of the noise consists in a less biased distribution of the affected registers.

Experimental data also confirm the models and simulation data presented in Chapter 4 demonstrating that particular registers can be randomly affected by

noise from one noise pulse to another. This behavior is related to the distribution of the substrate noise and to the fact that the noise phase difference for the transistors of certain registers may not be sufficient to produce a parasitic transition for each noise pulse. Two examples of this random behavior are shown in Figs. 6.13 and 6.14.

It is also shown that if the registers are placed with the depletion transistors closer to the noise source and the enhancement and pass transistors farther (see Fig. 3.1), the noise tolerance improves by up to 10%.

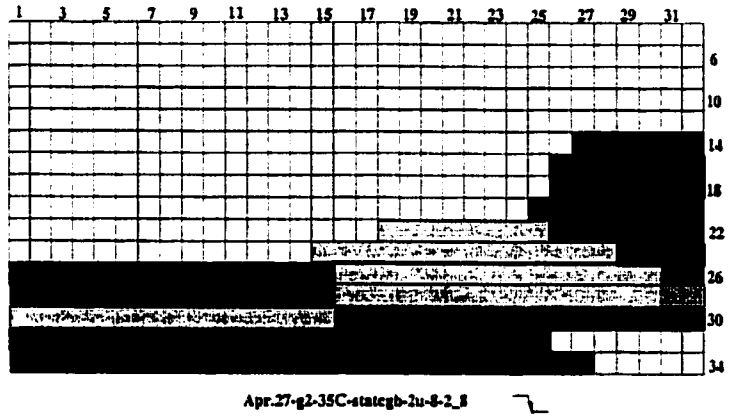


Figure 6.13: Particular registers can be randomly affected by noise. The grey area represents the randomly affected register locations, while the dark area represents the location of the registers that are constantly affected. Group2 is active and clocking regime 2 is used.

6.2.7 Effects of ground bounce

Due to the magnitude of the switched currents, ground routing is a delicate issue in the noise behavior of digital circuits. Ideally, ground routing should be realized in a dedicated low resistivity metal layer. However, as mentioned in Chapter 3, tradeoffs among the physical design, functionality (the heaters must be aligned), and the noise behavior affects the physical layout and in particular the

ground routing, particularly if a single metal layer is used. The experimental data show that ground bounce does occur, inducing substrate noise nonuniformities and generating phase differences and oscillatory substrate noise waveforms through V_{noise} effects as shown in Section 6.1. The more groups of drivers that are on, the larger these problems become.

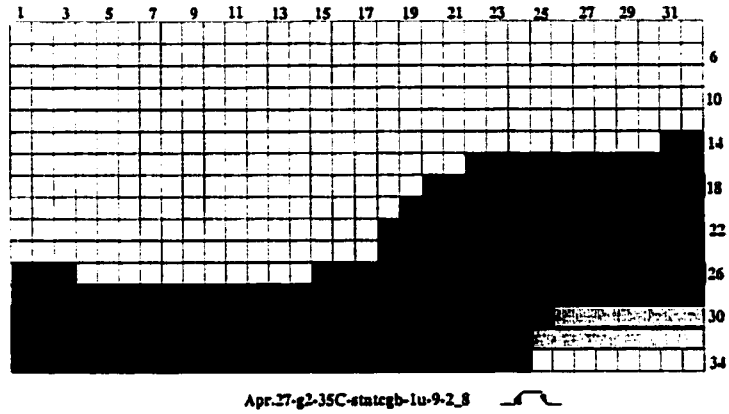


Figure 6.14: Particular registers can be randomly affected by noise. The grey area represents the randomly affected register locations, while the dark area represents the location of the registers that are constantly affected. Group2 is active and clocking regime 1 is used.

The effects of ground bounce are illustrated in Fig. 6.15. Note that substrate contact 2 shown in Fig. 6.15 positively biases the substrate with a voltage equal to $V = R_{metal}I$, creating V_{noise} as shown in Section 6.1.

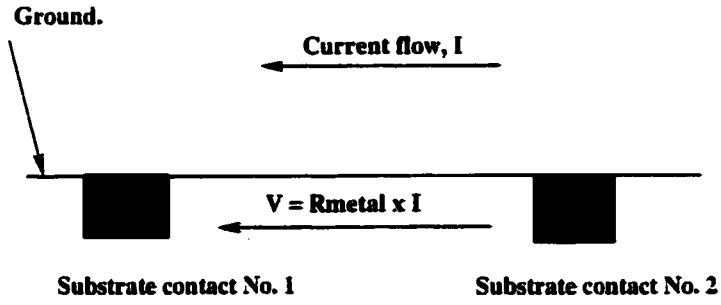


Figure 6.15: High switched currents biasing the substrate through the ground distribution.

The experimental data also show that the connections between the ground of the power drivers and the ground of the logic circuitry play a major role in the noise behavior of both the static and dynamic registers. It is shown that the noise behavior is significantly deteriorated when the grounds are connected off-chip versus when the grounds are connected on-chip, contrary to expectations when viewed from an analog circuit perspective, where for off-chip connected grounds, the logic ground remains quiet which could be regarded as beneficial. However, according to the models presented in Chapter 4 and the effects of V_{noise} discussed in Section 6.1, the following considerations elucidate the improved noise behavior of the digital circuits that is experimentally observed for the on-chip connected grounds:

- For on-chip connected grounds, the internal nodes of the digital circuitry are discharged to a positively biased ground level (due to the high switched currents). This voltage level can be sufficient to leave the circuit operational in an unaffected state once the switching process is complete.

- A quiet digital ground increases the V_{noise} effects, since any substrate voltage transients only affect the sources of the power drivers which are not immediately seen by the predriver (see Fig. 6.5).

6.2.8 Power driver supply voltage and current

An experimental analysis has been performed to derive the noise sensitivity of the registers as a function of the supply voltage and current of the power drivers. This analysis also considers the dependency of the noise on the clocking regimes. The results are illustrated in Fig. 6.16. Note that as the supply voltage increases, the number of affected registers increases. Note also the dependency on

the clocking regimes, and for a particular clocking regime, the dependency on the power supply.

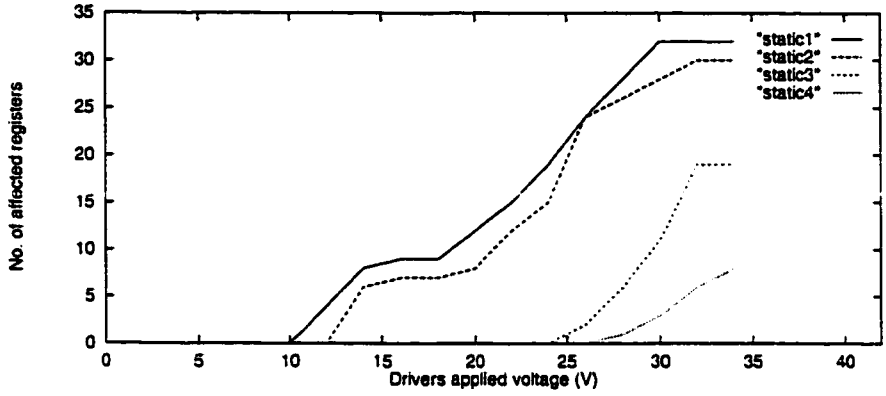


Figure 6.16: The number of affected registers as a function of the driver power supply voltage for four clocking regimes (for static registers).

It has also been experimentally confirmed that more registers are affected as the time during which the power drivers are on (the duration of the driver pulse shown in Fig. 6.8) increases. This behavior can be explained by the increase in the number of transitions of the substrate noise waveform as shown in Section 6.1. Accordingly, the probability that a register is affected by noise increases as the driver pulse duration increases due to the higher probability of a significant difference of phase during the oscillatory substrate noise waveform while the driver pulse is active.

The number of affected registers increases by less than 5% for static registers when the chip temperature is varied between 25°C and 55°C. The variation is further insignificant for dynamic registers. For temperatures greater than 60°C, however, the proper operation of the circuit is significantly affected due to an increase in the ambient temperature of the circuit affecting the operation of the transistors.

6.2.9 The size of the noise source

The number of affected registers increases as the number of active drivers increases. This behavior is expected according to a multitude of issues as discussed in Chapter 4 and Section 6.1. This behavior is experimentally shown in Fig. 6.17.

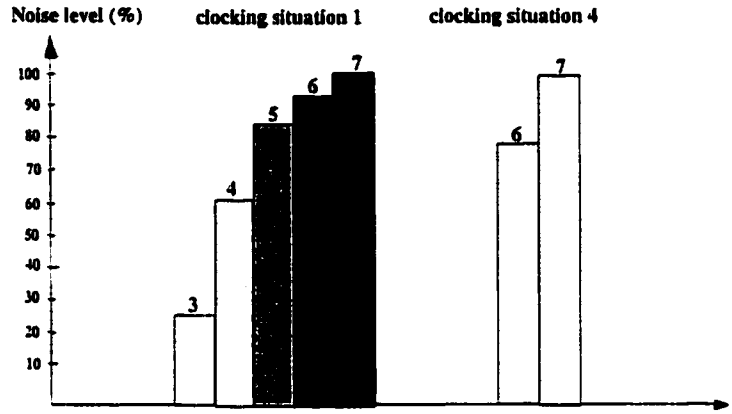


Figure 6.17: The relationship between the active drivers (the numbers above each column) and the generated noise for the 1 and 4 clocking regimes and for static registers. The seven active drivers, in both clocking situations represents the 100% noise level and is relative to each other. The noise level is $\approx$ 30X smaller for clocking regime 4 as compared to clocking regime 1.

By skewing the noise pulses (or the driver pulses) as discussed in Chapter 3, no significant effect on the noise sensitivity of the registers is obtained, due to the oscillatory substrate noise waveform, as shown in Fig. 6.2. The initial noise spikes, which significantly influence the noise sensitivity, are not significantly reduced by skewing the noise pulses. The duration of the oscillatory noise waveform is larger by the skew time, but since the skew time is insignificant as compared to the total duration of the noise pulse, this increase in the duration of the oscillatory noise waveform is insignificant in terms of creating increased noise effects. However, for a non-oscillating substrate noise waveform, skewing the noise pulses could have a significant effect as discussed in Chapter 3.

6.3 The connection between the substrate noise waveforms and the high level results

The primary objective of this section is to demonstrate that the results obtained in Section 6.2 are related to the substrate noise waveforms shown in Section 6.1. To accomplish this objective, two circuits with a similar layout as the circuits shown in Fig. 3.3b have been designed to simultaneously monitor the substrate noise waveforms and the sensitive registers. However, since from Section 6.1 the relationship between the substrate noise waveforms and the V_{DS} (or R_{test}) waveforms is known, V_{DS} for a number of drivers is monitored for convenience.

The experimental data demonstrate the following results:

- For a V_{DS} waveform without any oscillation, there is no effect on the registers *i.e.*, for a constant substrate noise level as shown in Fig. 6.1, no registers are affected.

- When the oscillation on a V_{DS} waveform begins and the amplitude of the oscillation increases (see Fig. 6.3), the number of affected registers increases, *i.e.*, an increased substrate noise amplitude and/or substrate oscillation affect the data stored in the registers by inducing parasitic transitions.

- The registers could be randomly affected by noise.

Tests have been performed that show that the oscillation and/or magnitude of the noise spikes increases as the power driver supply voltage increases and/or the size of the noise source increases while the number of affected registers increases. To clearly determine the effects of ground bounce, one of the circuits features a power driver ground line routed to create large voltage drops and ground bounce.

The experiments demonstrate that the oscillation and substrate noise waveforms are much higher than for a standard ground network. This increased oscillation and substrate noise amplitudes result in an increased likelihood of affecting the sensitive registers. The substrate noise is shown to be reflected in both the 5 volt and 13 volt power supply lines, with noise amplitudes up to +/− 20%. The noise waveforms induced into the power supply lines resemble the noise waveforms derived from the substrate.

6.4 Noise mitigation techniques

The discussion in Chapter 3 of the issues that influence the generation, transmission, and reception of noise, the models and mechanisms from Chapter 4, the simulations from Chapter 5, and the experimental data from Chapter 6, permit the development of several noise mitigation techniques that achieve the primary objective of improving the noise behavior of a digital circuit in a mixed-signal smart-power environment (and generally in any noisy environment). These techniques are for a given technology and amount of substrate noise, in which circuit and physical design techniques are applied without any process alterations. The following noise mitigation techniques are summarized:

- Static registers are preferably used since the noise behavior of the static registers is more predictable than for dynamic registers.

- Design the logic circuitry such that "zero" states are stored wherever needed since the "zero" states are immune to noise. For example, inverters should be used to invert the "zero" states stored in a register if a "one" logic state is needed in the circuit, such as, for example, to drive the predriver.

- If particular circuit considerations and trade-offs recommend the use of dynamic registers, the logic circuitry should be designed to predominantly store "one" logic states since these states are less sensitive to noise when stored in a dynamic register as compared to a stored "zero" state.

- For the period of time during which the drivers are active (the noise is generated), special care must be taken to design the state of the clock used to synchronize the registers. As has been described, the proper state of the clock is different depending on whether the registers are static or dynamic. A proper clock state during the noise generation process significantly reduces the noise sensitivity of the static and dynamic registers for the same amount of noise present into the substrate.

- The logic elements should preferably be sized around $k_E/k_D = 4$ with a smaller or larger ratio depending on whether the noise is estimated to be primarily in phase or not.

- The logic elements should be similarly loaded, preferably by a large capacitive load. This technique can only be used in low speed applications. If low logic speeds are unacceptable, then the more similar the loads the better.

- The ground routing should be realized with thick and wide low resistivity metal layers. This routing style will produce small voltage drops on the ground lines minimizing ground biases and the effects of ground bounce.

- The grounds of the different circuit blocks, such as the ground of the drivers, the predrivers, and the logic blocks, should all be connected on-chip, with minimal parasitic resistances from one ground line to another ground line.

Accordingly, the same routing style with a low resistivity metal is recommended, thereby eliminating any V_{bias} effects and oscillatory substrate noise.

- Every transistor of a logic element should have a dedicated substrate contact in its vicinity, similar to an analog physical design style. These substrate contacts should be connected by a low resistivity metal layer. Multiple beneficial effects are achieved by this technique, such as:
  - A reduction of the amplitude of the substrate noise.
  - The same noise phase for all of the constituent transistors. As shown, since the noise simultaneously affects all of the transistors, practically no registers are affected, independent of the magnitude of noise (see Chapter 5 for more details).
  - A reduction in V_{noise} effects and the oscillatory noise waveforms.
- A compact layout is beneficial since the RC delays among the transistors of each latch are minimized.
- A low impedance substrate is recommended. This substrate creates smaller delays (or differences in phase) between one point of the substrate to another point. A non-epitaxial process is preferable due to the lower capacitive element of the substrate. A high voltage process, however, necessitates a low doping concentration in the substrate, creating a high resistance.
- If possible, it is recommended to place the noise sensitive digital circuitry as far and/or as symmetric as possible with respect to the noise source. This floorplan style maintains a similar phase for all of the transistors within the logic elements.

- It is recommended to operate the power drivers at a lower voltage power supply. If a power resistor is required to dissipate a certain power (as in the present application), it is preferable to operate the power resistor at larger currents (with larger transistors) rather than at large voltages.

- The on-off process for the power drivers should be skewed in time as much as possible. This strategy will decrease the noise amplitude within the substrate.

Chapter 7

Placement of Substrate Contacts in Epi and Non-Epi Technologies

As discussed in Chapters 4, 5, and 6, the noise behavior of digital circuitry is particularly affected by the non-uniform substrate noise distribution throughout the substrate. The noise magnitude is also shown to have a major influence. The primary objective of this chapter is to develop a sound strategy for the placement of substrate contacts and rings in order to minimize the amplitude of the noise received by the digital noise sensitive circuitry as well as obtain a uniform noise distribution throughout the substrate.

A static analysis of the noise distribution for epi and non-epi technologies is performed in Sections 7.2, 7.3, and 7.4. A shape for the power resistor of the ink-jet driver which features a highly uniform power distribution over the entire surface is discussed in Section 7.5.

7.1 Modeling

A qualitative representation of the noise distribution within the substrate for an epi and non-epi technology is discussed in Section 2.5. The primary objective

of this analysis is to determine the significance and influential factors in placing substrate contacts and rings on the noise distribution, and to develop and present rules for placing substrate contacts and rings in order to minimize and equalize the noise amplitude received by the sensitive circuitry.

A three-dimensional representation of the noise distribution is developed to achieve these objectives. The noise density, which is the third dimension in the graphical representations, is determined inside a two-dimensional section of the substrate. The following assumptions are made in the development of the model used to derive the noise distribution:

- As experimentally shown in Section 6.1.3, the noise is generated during the transitions from the linear region to the saturation region and from the saturation region to the linear region of operation of the power transistors.
- The magnitude of the generated noise depends upon the input signal transitions, the power transistor size, and other related technological aspects such as the substrate doping, substrate characteristics, and gate doping.
- For a given technology and application, all of the aforementioned variables are constant, and therefore it is assumed that the generated noise is constant. As a consequence, the noise source can be modeled as a constant current source.
- The constant current source injects noise into a resistive mesh which represents the substrate. The capacitive element of the substrate is neglected, first because it would give a fourth dimension in the representation (the time dimension), and second because once the substrate contacts and rings are placed to minimize the noise amplitude and nonuniformities, the effect of

the delays due to the capacitive element of the substrate is minimal since, as shown in Chapter 4, the amplitude and noise nonuniformities should be large in order to induce a parasitic transition at the output of a logic element.

A schematic of the model used to determine the noise distribution is shown in Fig. 7.1. For a non-epi substrate, the entire substrate is assumed to have the same resistivity. For an epi substrate, the epi layer, smaller in thickness than the bulk, has a resistivity *R1*, while the bulk has a resistivity *R2*.

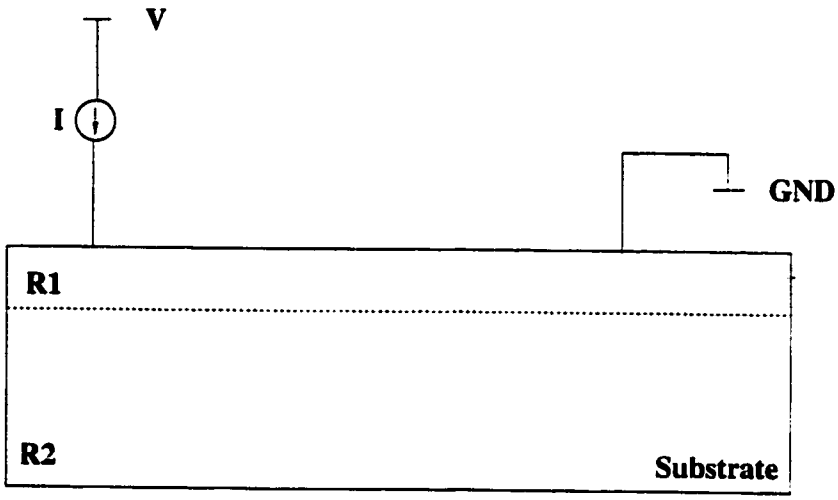


Figure 7.1: Schematic of the model used to derive the three-dimensional noise distribution within the substrate

The substrate is modeled as an R mesh, realized by connecting a large number of two-dimensional resistive primitives. A resistive primitive is shown in Fig. 7.2. The two-dimensional substrate section used to derive the noise distribution is composed of 36 by 24 resistive primitives. For an epi substrate, 36 by 6 resistive elements make up the epi layer, and the remaining elements make up the bulk. The 36 by 24 matrix of resistive primitives has been chosen since this matrix size provides sufficient precision while maintaining reasonable computational complexity.

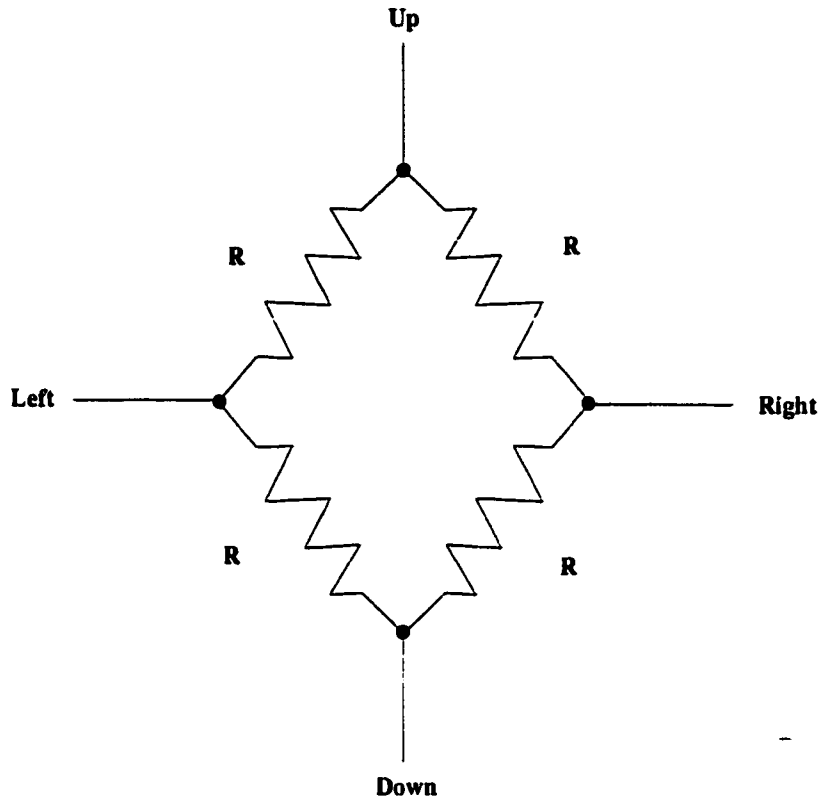


Figure 7.2: A resistive primitive used to model a section of the substrate

The procedure to determine the substrate noise distributions is as follows. Several substrate contact placement configurations are simulated using the Cadence Spectre [98] simulator. A C program has been developed to process the files generated by the simulator in order to derive the current through each resistor of each resistive primitive. An average value of the current passing through each resistive primitive is computed as the median of the currents through the four resistors of each resistive primitive. These average currents are plotted to obtain the substrate noise distribution. The flow of this procedure is shown in Fig. 7.3.

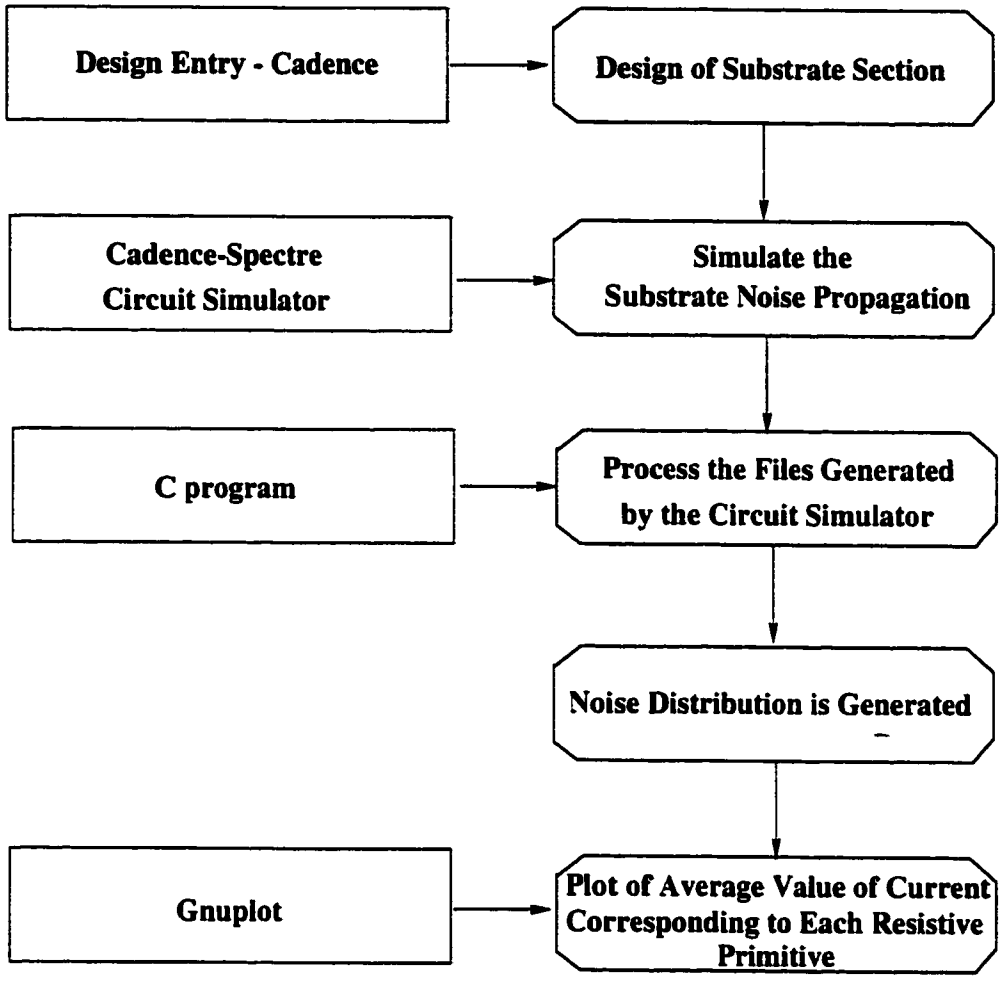
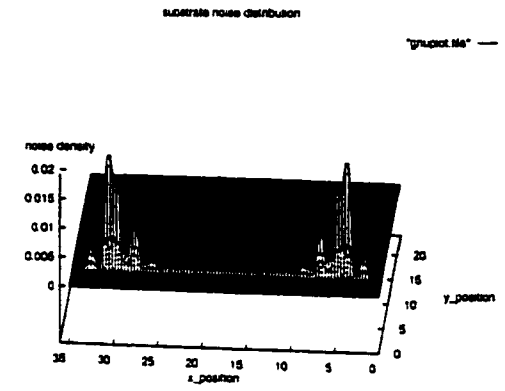


Figure 7.3: Flow diagram of the procedure used to determine the noise distribution within a substrate

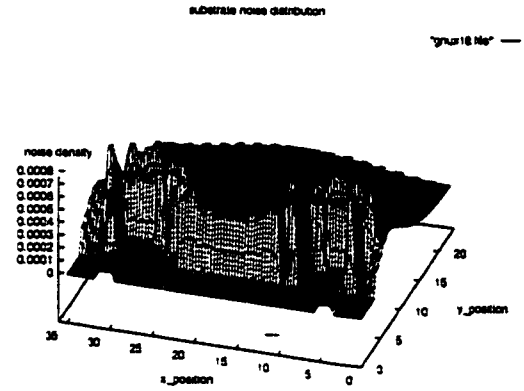
7.2 Substrate noise distribution for a non-epi technology

The highest density of substrate noise for a non-epi technology is predicted by Wooley in [69] to be at the substrate surface. In this section, this prediction is demonstrated by several three-dimensional substrate noise distributions. A thor-

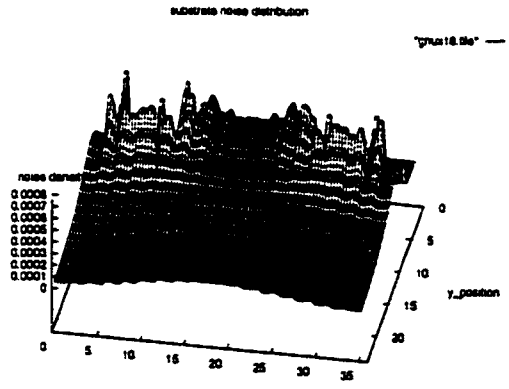
ough analysis of these distributions for a variety of substrate contact placement conditions suggests a number of rules and methodologies for placing substrate contacts and rings in order to reduce and equalize the substrate noise. The most significant practical configurations are analyzed, and conclusions are drawn for each case.



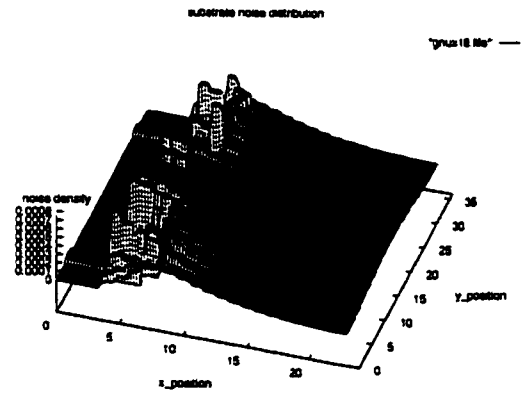
(a) Main front view



(b) Magnified front view



(c) Magnified back view



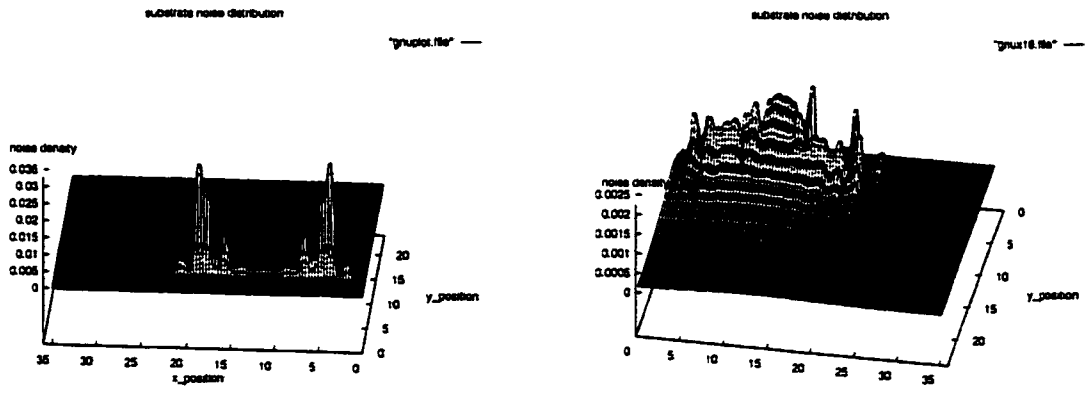
(d) Magnified lateral-back view

Figure 7.4: Substrate noise distribution for a non-epi technology for one substrate contact

7.2.1 Substrate noise distributions for one individual substrate contact

In the following discussion, an individual substrate contact is defined as a substrate contact that has a small size as compared to the distance from the noise source to the noise receptor. Three-dimensional noise distributions obtained for one individual substrate contact are shown in Fig. 7.4.

Note in Fig. 7.4a the high noise density where the noise enters the substrate (at the noise source) and exits the substrate (at the substrate contact connected to GND). Note the constant noise distribution at the substrate surface. For a detailed view of the noise distribution, the large input and output densities are eliminated in Figs. 7.4b, 7.4c, and 7.4d. Note in Figs. 7.4b, 7.4c, and 7.4d the symmetric noise distribution with the highest noise density at the surface of the substrate, gradually decreasing as the distance from the substrate surface increases.



(a) Main front view

(b) Magnified front view

Figure 7.5: Substrate noise distribution for a non-epi technology for the condition where the substrate contact is close to the noise source

Significant noise distributions for the configuration where the output node is closer to the input node are shown in Fig. 7.5. Note the higher noise density at the substrate surface as compared to Fig. 7.4, and also note that there is no noise propagation on the opposite side of the substrate contact with respect to the noise source.

Each of these noise distributions represent distributions of current and can be translated into voltage distributions. A general form of a voltage distribution is shown in Fig. 7.6.

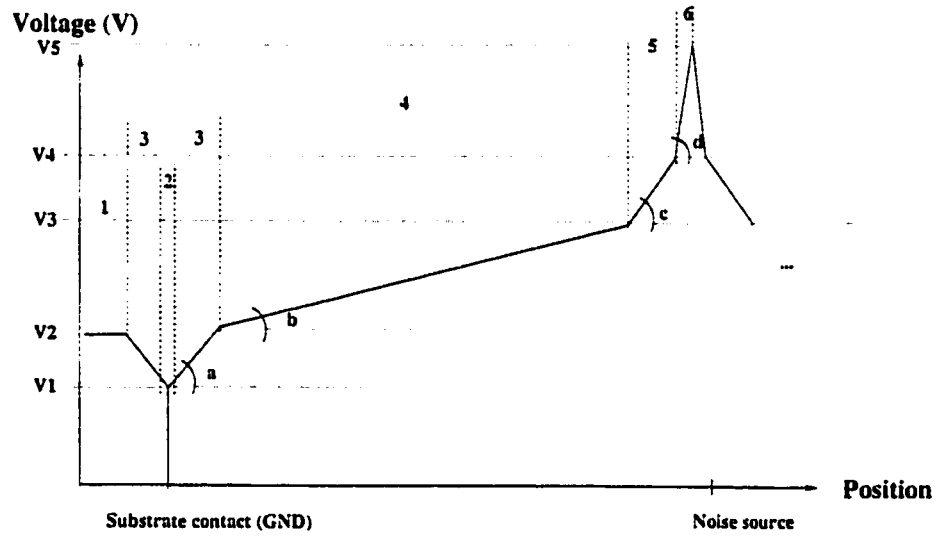


Figure 7.6: A voltage distribution at the substrate surface for one substrate contact

If the substrate contact (GND) is assumed to be at zero potential, the large spike in the substrate near the substrate contact produces a potential V_1. In the immediate vicinity of the substrate contact (region 3 in Fig. 7.6), the noise density is large, producing a voltage drop of $V_2 - V_1$. At the end of this region (region 1 in Fig. 7.6), the substrate remains biased at V_2. This constant bias has been experimentally observed, as shown in Fig. 6.1. In region 4, the noise density is smaller and constant, the voltage potential increasing approximately linear with a

slope "b." A similar region as region 3 is noted in region 5. Finally, the large noise spike near the noise source is noted in region 6. This profile is obtained when the noise source injects noise into the substrate, and can be symmetric with respect to the x axis depending upon the direction of the noise flow into the substrate.

An important conclusion regarding the placement of the noise sensitive circuitry is noted. A common technique in physical design is not to place individual substrate contacts near each constituent transistor, but rather to place a global substrate contact within each circuit block. An obvious reason for this design technique is to save area and ease the design effort. Note that if the sensitive circuitry (with no substrate contacts) is placed as in region 4 of the substrate (see Fig. 7.6), the constituent transistors are affected by a large and variable potential, which, as shown in Chapter 4, can easily induce a parasitic transition at the output of a logic stage. If the sensitive circuitry is placed as in region 6, the constituent transistors are affected by an approximately constant potential, V_2 (see Fig. 7.6). As shown in Chapter 5, a constant potential, even if large, is less likely to induce a parasitic transition than a non-uniform noise distribution. Accordingly, if a design technique is used in which a global substrate contact is placed within a circuit block, all of the constituent transistors of that block should be placed as in region 6 (see Fig. 7.6). If this is not possible, the sensitive transistors should be placed close to the substrate contact as in region 4 (the distance from the transistor to the substrate contact should be much smaller than the distance from the transistor to the noise source).

Another observation is related to the distribution of the forward biasing potential for a junction. It is common practice in the physical design process to place a substrate contact in the immediate vicinity of the source diffusion of a transistor,

as shown in Fig. 7.7a. The $P+$ substrate contact diffusion is low resistivity, and therefore, V_1 (see Fig. 7.7a) is approximately zero. In the immediate vicinity of the $P+$ diffusion, the noise density is high (as in region 1 of Fig. 7.6). Accordingly, the potential profile is quite abrupt, and the potential differences, $V_2 - V_1$ and $V_3 - V_2$, are large. If the noise is large, the potential can exceed 0.7 volts and forward bias the $N+$ junction. Note that the likelihood of forward biasing the $N+$ junction increases as the distance from the substrate contact increases. This forward biasing effect can induce a parasitic transition as well as affect the reliability of the transistors (see Chapter 5). To reduce these noise effects, a practical solution is to place the $P+$ diffusion as shown in Fig. 7.7b, where the $P+$ diffusion creates an approximately constant and close to zero potential over the entire junction area. The noise, originating from the drain, minimally affects region 1 of the junction for two reasons: 1) region 1 is not in the main trajectory of the noise, and 2) the transistor channel produces already a potential distribution from the source to the drain in both the saturated and linear regions of operation.

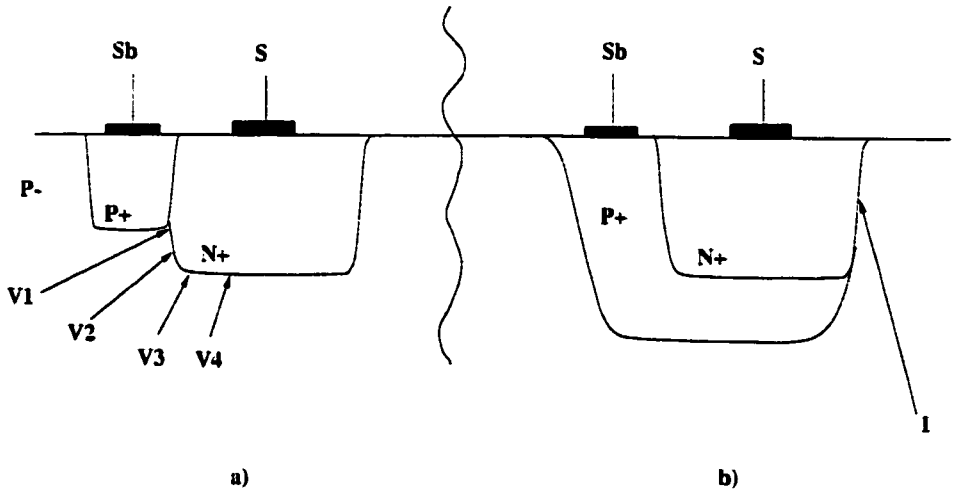
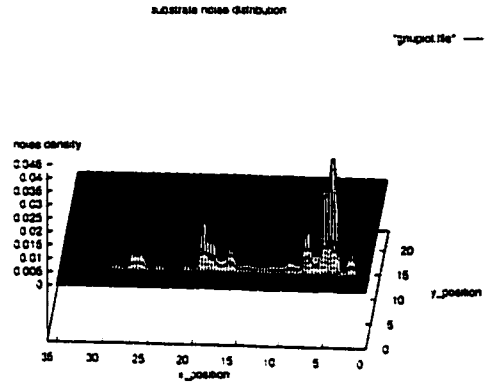
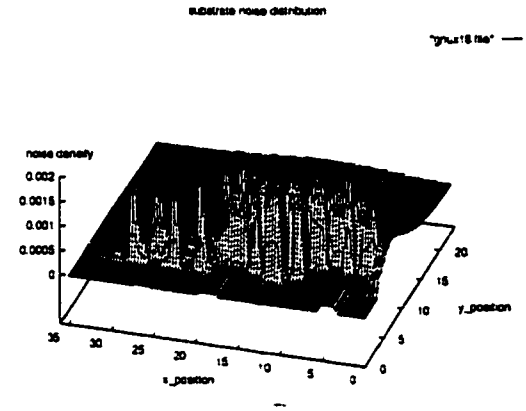


Figure 7.7: The forward biasing distribution potential of a junction: a) typical and b) recommended diffusion profiles for the substrate contact.

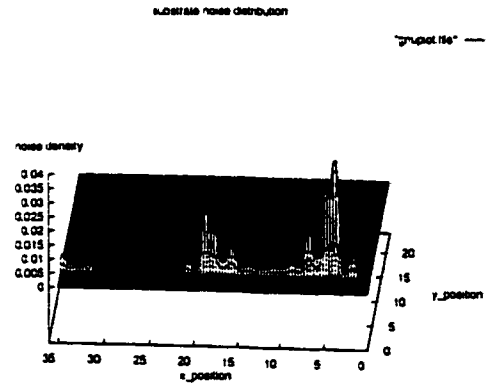
Note the importance of these effects on the power transistor. A substrate contact that is not placed near the immediate vicinity of the source diffusion of the power transistor creates a body effect which induces V_{noise} effects (see Section 6.1.4), and forward biases the source-to-substrate junction.



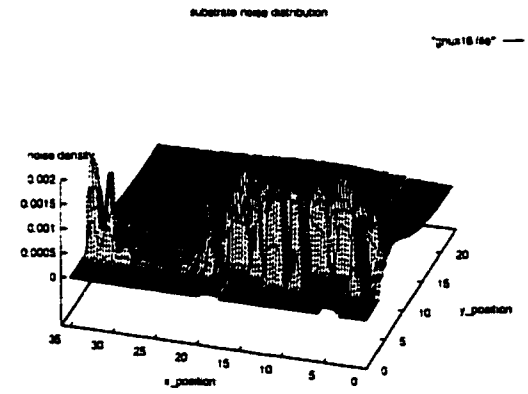
(a) Main front view



(b) Magnified front view



(c) Main front view



(d) Magnified front view

Figure 7.8: Substrate noise distribution for a non-epi technology where two substrate contacts are used. The distance between the noise source and the first substrate contact is constant, while the distance between the two substrate contacts is smaller for the a and b cases than for the c and d cases.

7.2.2 Substrate noise distributions for multiple individual substrate contacts

Several analyses have been performed to determine the effect of placing multiple substrate contacts at different distances from the noise source. In Fig. 7.8, noise distributions for two individual substrate contacts are presented. In Figs. 7.8a, 7.8b, 7.8c, and 7.8d, the distance between the noise source and the first substrate contact is constant, while the distance between the substrate contact 1 and substrate contact 2 is smaller in Figs. 7.8a and 7.8b than in Figs. 7.8c and 7.8d.

Based on these noise distributions, a similar voltage distribution as shown in Fig. 7.6 can be presented for the two individual substrate contacts case, illustrated in Fig. 7.9. Note the three noise spikes and the several regions in which the substrate is divided.

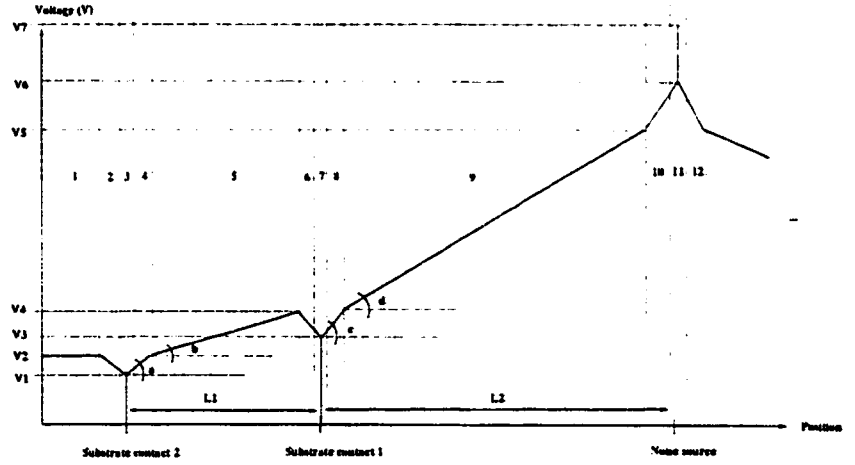


Figure 7.9: A general form of a voltage distribution at the substrate surface when two substrate contacts are used

From Figs. 7.8 and 7.9, the following conclusions can be drawn:

- The noise spike at substrate contact 1 (closer to the noise source) is larger that the noise spike at substrate contact (SC) 2.

- The noise spike at SC 2 becomes smaller while the noise spike at SC 1 becomes larger as the distance between SC 1 and SC 2 increases.
- The noise density in region 5 is much smaller than in region 9.
- The noise density in region 5 decreases as the distance between SC 1 and SC 2 increases.

Note the benefits of using multiple substrate contacts. An observation can be made for an efficient multiple substrate contact placement strategy for a non-epi technology. Two substrate contacts, for example, are efficient in reducing the noise if the distance between the two contacts (L_1, see Fig. 7.9) is comparable to or larger than the distance between the first substrate contact and the noise source (L_2), or generally, between the first substrate contact and the previous substrate contact. If L_1 is much smaller than L_2, the two substrate contacts receive practically the same noise, and the use of multiple substrate contacts is less efficient.

7.2.3 Tradeoffs among individual substrate contacts, large substrate contacts, and rings

In the following discussion, a large substrate contact is a substrate contact for which at least one dimension of the substrate contact cannot be neglected as compared to the closest distance from the substrate contact to the noise source. Based on the aforementioned noise distributions and observations for single and multiple individual substrate contacts, certain conclusions regarding the placement of individual substrate contacts versus rings can be stated. Consider first

the spatial noise distribution for two individual substrate contacts as shown in Fig. 7.10.

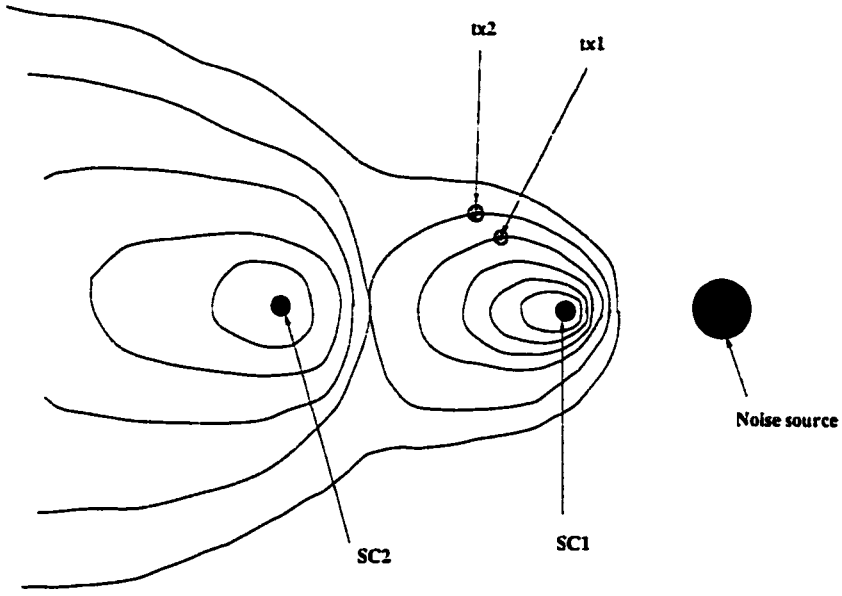


Figure 7.10: A spatial noise distribution for two individual substrate contacts. Lines of equal noise are shown.

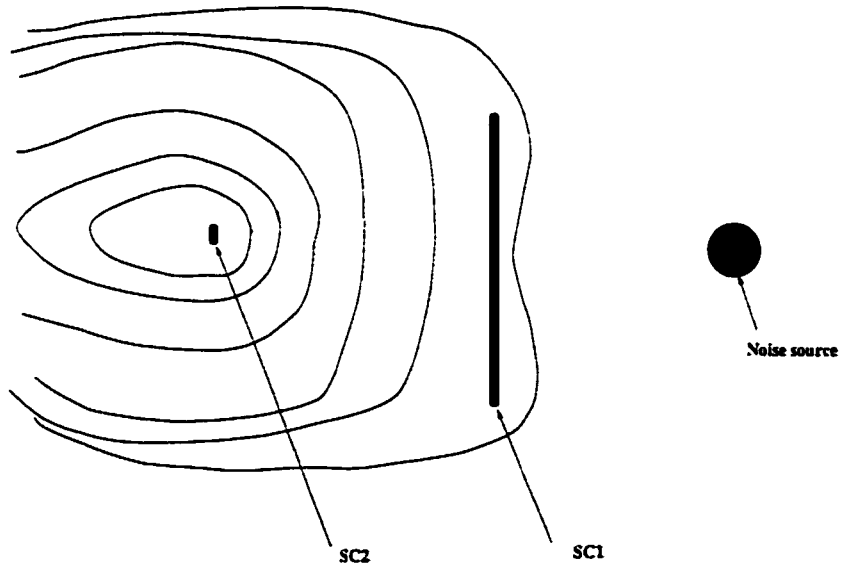


Figure 7.11: A spatial noise distribution for one large substrate contact and one individual substrate contact. Lines of equal noise are shown.

SC1 and SC2 are the two individual substrate contacts, and tx1 and tx2 are the two transistors within the circuit. Note that even if tx1 and tx2 are close, these transistors exhibit different noise lines. Accordingly, a noise nonuniformity exists between tx1 and tx2, which, as shown in Chapter 5, can induce a parasitic transition at the output of the respective logic element.

Large substrate contacts produce a noise distribution as shown in Fig. 7.11, creating a zone with a smaller noise amplitude and higher uniformity than for individual substrate contacts (see Fig. 7.10). This zone is situated behind and in the vicinity of SC1.

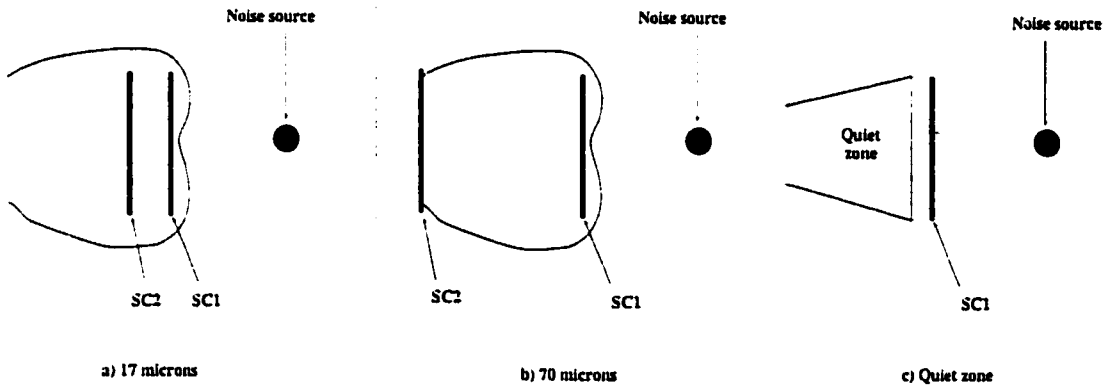


Figure 7.12: A spatial noise distribution for large substrate contacts. Lines of equal noise are depicted. The distance between SC1 and SC2 is a) 7 μm and b) 70 μm. The "quiet zone" is shown in c).

A quiet zone, shown in Fig. 7.12, has been experimentally observed as discussed in Section 6.1.5. The circuit for which measurements have been performed uses large parallel substrate contacts, as in the group4 circuits illustrated in Fig. 3.4. The noise is significantly reduced at 17 μm behind a grounded substrate contact. Practically no reduction in noise is noted at 70 μm. This high noise variation for a relatively small distance is due to the large parallel and equal length substrate

contacts that are used (see Fig. 3.4), which interact with the noise lines beyond a small distance (see Fig. 7.12). A conclusion is that the noise is reduced and uniform near and behind a large substrate contact. As the distance from the substrate contact increases, the noise remains small and uniform in an area as shown in Fig. 7.12c.

A ring surrounding the noise source, as shown in Fig. 7.13, produces a noise distribution similar to the two substrate contacts case (see Figs. 7.8 and 7.9) in any direction of the substrate (any section of the substrate such as 1, 2, 3, or 4, see Fig. 7.13). The benefit, however, is that the ring, connected to the ground, provides a lower resistivity path for the noise towards the ground than either the individual or the large substrate contacts due to the large area of the ring that surrounds the noise source.

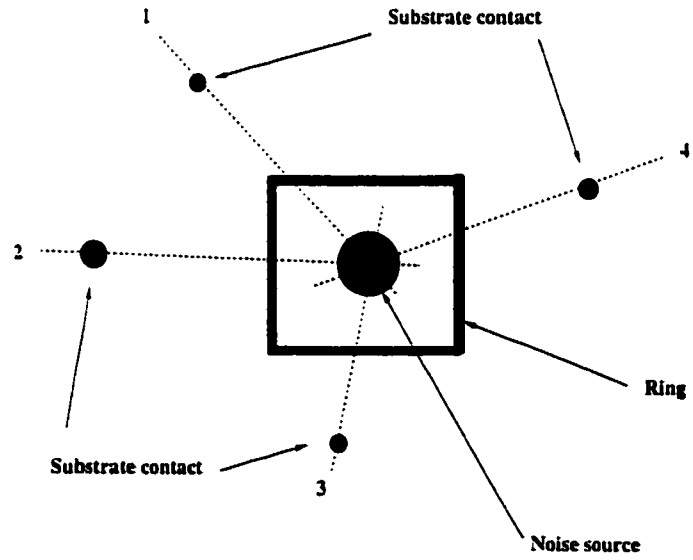


Figure 7.13: The effect of a ring on the substrate noise distribution

Since a substrate resistance is present within any section of the substrate between the noise source and the ring, a ring configuration is equivalent to con-

necting multiple similar resistors in parallel, thereby obtaining a small substrate resistance from the noise source to ground. This situation is equivalent to reducing the distance from the noise source to the substrate contact. A low resistivity noise path can also be obtained through the same mechanism of connecting multiple equivalent substrate resistors in parallel by using wide substrate contacts.

7.2.4 Significant issues for substrate contact placement

1. **Distribution of substrate resistance**

   As shown in Figs. 7.8 and 7.9, the noise distribution significantly depends upon the ratio of the distances between the noise source and the substrate contact 1, L_1, and between the substrate contact 1 and substrate contact 2, L_2 (see Fig. 7.9). These distances are proportional to the substrate resistances, R_1 and R_2. The noise at substrate contact 2, SC2, is directly proportional to the resistive ratio, R_1/R_2. Accordingly, the smaller R_1 is and/or the larger R_2 is, the smaller the noise at SC2 and the larger the noise at SC1. Alternatively, a condition for small noise at SC2 is

   $$\frac{R_1}{R_2} \ll 1. \tag{7.1}$$

   A low R_1/R_2 ratio can be obtained by minimizing R_1 by placing a ring around the noisy drain that is connected to the source terminal of the respective drain (as shown in Fig. 7.7b). A wide ring further decreases R1. The distance between the two contacts (L_2) should be as large as the physical design constraints permit, creating a large R_2. R_1 can be further decreased if a buried layer is placed below the noisy transistor.

2. **Multiple noise sources**

The R_1/R_2 ratio has a particular significance in the following case. Consider multiple independent noise sources surrounded by a common ring, as shown in Fig. 7.14a and as described in Chapter 3. If the noise source 1 (see Fig. 7.14a) is active, the noise distribution at the substrate contacts, a, b, c, and d (the large spikes), is as illustrated in Fig. 7.14b (expressed as the noise amplitude versus the position) where a, b, c, and d are the four sections of the ring (see Fig. 7.14a). This distribution is due to the different R2 resistances from SC1 to SC2 (SC2 consists of the a, b, c, and d sections of the ring). For this discussion, it is assumed that each noise source has a substrate contact near the source terminal, creating a constant R_1 for each noise source. Note that different transistors placed around the eommon ring will have a different body effect, larger and more uniform when the transistor is placed near the substrate contact a, smaller and more uniform when the transistor is placed near the substrate contact d, and variable when the transistor is placed near the substrate contacts, b or c. As the active noise source changes, different transistors are affected by a maximum body effect, depending upon the resistance R_2 from SC1 to SC2 (a, b, c, or d) and on the R_1/R_2 ratio. If no substrate contacts are placed near the noise sources, a variable noise on a, b, c, and d still occurs due to the variable resistance R_1 from the noise source to either a, b, c, or d.

Several solutions are possible to equalize the noise distribution across the ring as well as the body effect of each of the transistors, all based on creating a small resistance R_1 and R_1/R_2 ratio, such as:

- Use substrate contacts at each noise source as shown in Fig. 7.7.

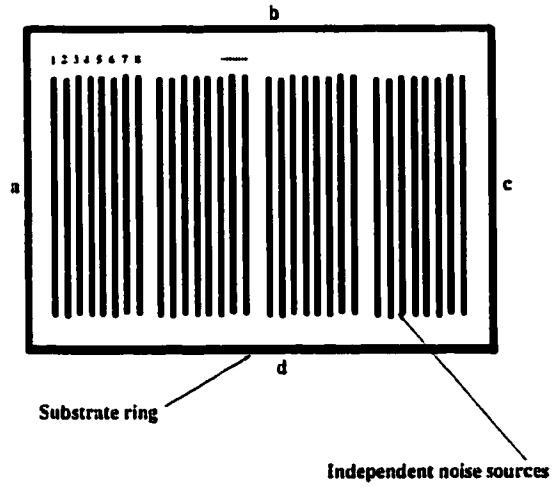
- Progressively surround groups of noise sources with rings. The smaller the groups, the better. The rings should be placed so as to create a small R_1/R_2 ratio, by making the distance from SC1 (of the noise source) to SC2 large. Multiple layers of rings are beneficial. The higher the layer, the more noise sources are surrounded. The primary drawback of multiple layers of rings is the large area that is required. A ring placed close to another ring also has minimal benefit other than the ring closest to the noise source which decreases R_1. To decrease the R_1/R_2 ratio, the rings closer to the noise source should be wider, while the rings farther from the noise source should be thinner.

- Place individual substrate contacts close to each transistor or each small group of transistors. These substrate contacts should be placed at a considerable distance from the last ring to create a small R_1/R_2 ratio. With this technique, a local noise reduction (for the area surrounding the individual substrate contact) and a high noise uniformity across the substrate is achieved.

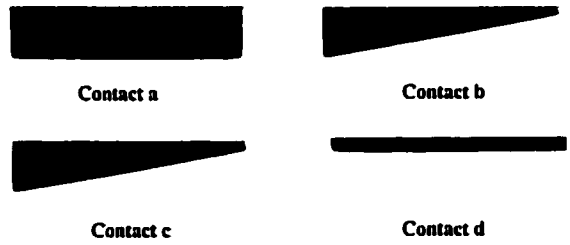
3. **Physical design aspects of a ring**

The ring is connected to ground. In order to provide a ground potential for the entire ring, Metal 1, for example, can follow the $P+$ ring diffusion surrounding the noise sources (as shown in Fig. 7.15a). However, multiple lines, such as the power and control lines, must be connected to the noise sources. These lines will require the Metal 1 connecting the ring to be interrupted, as shown in Fig. 7.15b. Where Metal 1 is interrupted, the connection between *Metal 1a* and *Metal 1b* is made through the $P+$ diffusion, inserting a resistance R, thereby producing an IR voltage drop. This IR voltage drop

can bias *Metal 1b* with respect to *Metal1a*. This bias may be important if the gap is large (high resistance) or the current I is large. This voltage drop biases the substrate below *Metal 1b* and may produce noise through any of the mechanisms described in Chapters 4 or 6, depending upon the magnitude of the IR drop. In the extreme case, if the IR drop is significant, the situation is equivalent to the substrate contact below *Metal 1b* having a negligible effect.



a) Multiple noise sources surrounded by a common ring



b) Noise distribution around the a, b, c, and d substrate contacts when the noise source 1 is active

Figure 7.14: Noise distributions: a) multiple noise sources surrounded by a common ring, b) the associated noise distribution on each of the sections of the ring

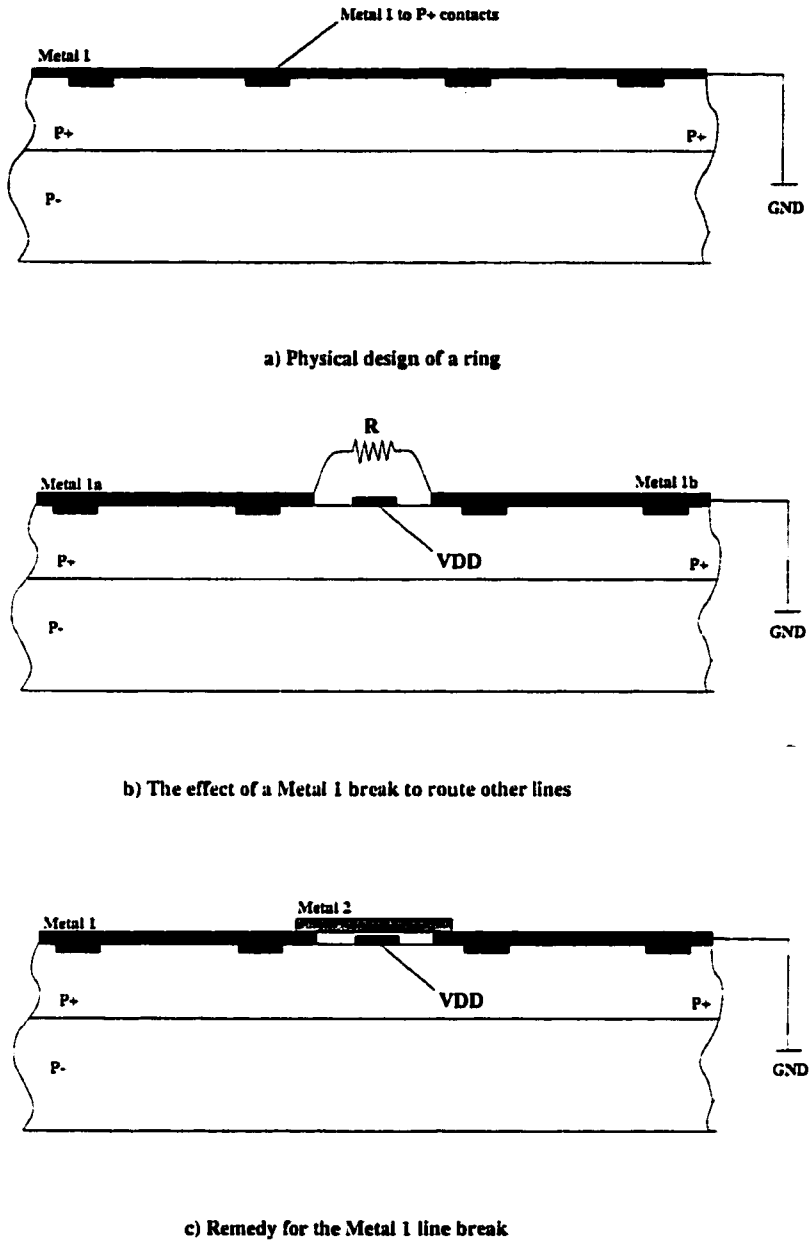


Figure 7.15: Physical design aspects of a ring; a) Typical physical design, b) The effect of a Metal 1 break induced by other lines, c) Remedy for the Metal 1 break

Solutions to minimize or eliminate this effect exist such as:

- Do not break *Metal 1* on the $P+$ substrate contact. Make the necessary connections to the noise sources in *Metal 2*.

- Minimize the current passing through the resistor by diverting the current through low resistance paths to ground through careful physical layout design.
- Create low resistivity paths between *Metal 1a* and *Metal 1b* by using, for example, *Metal 2* as shown in Fig. 7.15c.

4. **Ring surrounding the sensitive circuitry**

A ring surrounding the sensitive circuitry, as shown in Fig. 7.16, is controversial because of the following reasons. Assuming that the noise source has a substrate contact of its own, $R1$ is fixed.

- If L is small, than the a, b, c, and d sections of the ring have different R_1/R_2 ratios, and, therefore, a nonuniform distribution of noise at the ring sections is obtained. This nonuniform distribution does not benefit the sensitive circuitry, therefore, the ring placement around the sensitive circuitry is not useful.
- If L is large, then the a, b, c, and d sections of the ring receive approximately the same amount of noise since each has similar R_1/R_2 ratios. Due to the large L, these R_1/R_2 ratios are small which is beneficial. Therefore, for large L, placing a ring around the sensitive circuitry is beneficial. However, at large distances L, the effect of the ring looses significance, since placing a large substrate contact for the entire sensitive circuitry or placing individual substrate contacts for the constituent transistors has the same effect in reducing the noise. Large L distances are also not preferable due to the significant area that is expended.

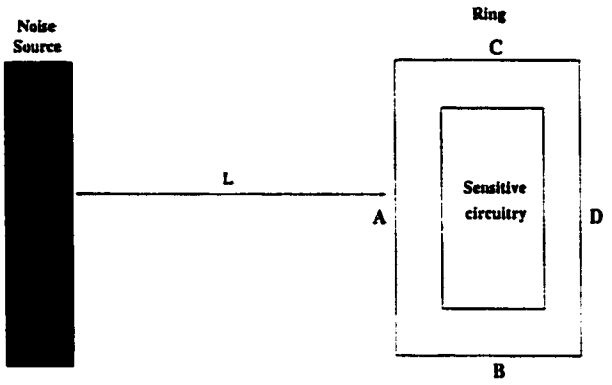


Figure 7.16: Ring surrounding sensitive circuitry

Based on these considerations, a ring surrounding the sensitive circuitry does not bring any significant benefits, and may create additional problems. It is, therefore, preferable to place a ring to surround the noise sources, maintaining small R_1/R_2 ratios. It is also preferable that each transistor of the sensitive circuitry or group of transistors has individual substrate contacts.

7.2.5 Conclusions

To summarize this analysis for a non-epi technology, the following general remarks can be listed.

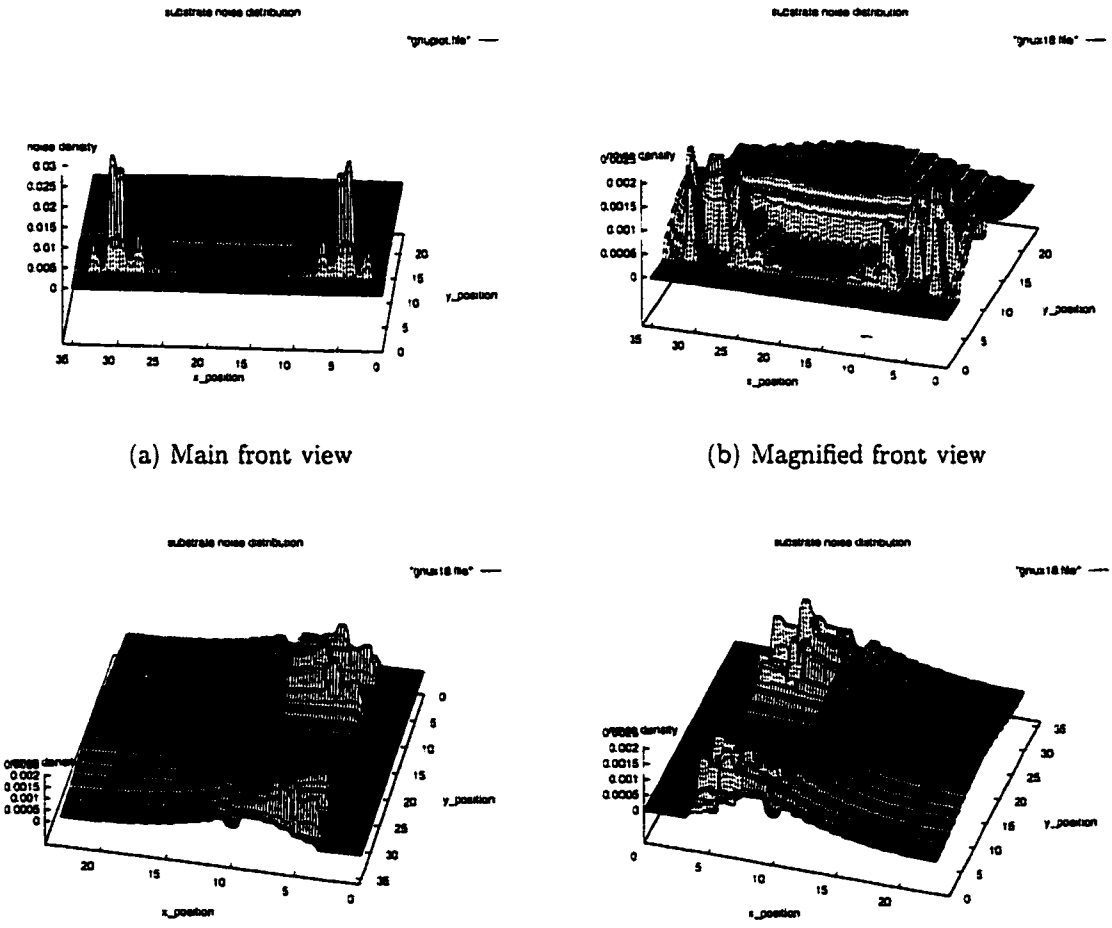
- Place a large and wide ring (a substrate contact) in the immediate vicinity of the source terminal of the noise source.
- At a considerable distance, place another thinner ring.
- If possible, place one more even thinner ring at a large distance from the previous ring.

- If multiple noise sources are present, progressively surround the noise sources with rings.
- Use special precautions when breaking the continuity of the rings.
- Place either an individual substrate contact near each constituent transistor of the sensitive circuitry or place a large substrate contact symmetric to a small group of transistors. Preferably, the sensitive circuitry should be placed at a considerable distance with respect to the noise source and the last ring surrounding the noise source.

The application of these rules will produce a low level and uniform noise distribution around the sensitive circuitry in a non-epi technology.

7.3 Substrate noise distribution for an epi technology

The highest density of substrate noise for an epi technology is predicted by Wooley in [69] to be at the interface between the epi layer and the bulk.



(a) Main front view

(b) Magnified front view

(c) Magnified lateral-front view

(d) Magnified lateral-back view

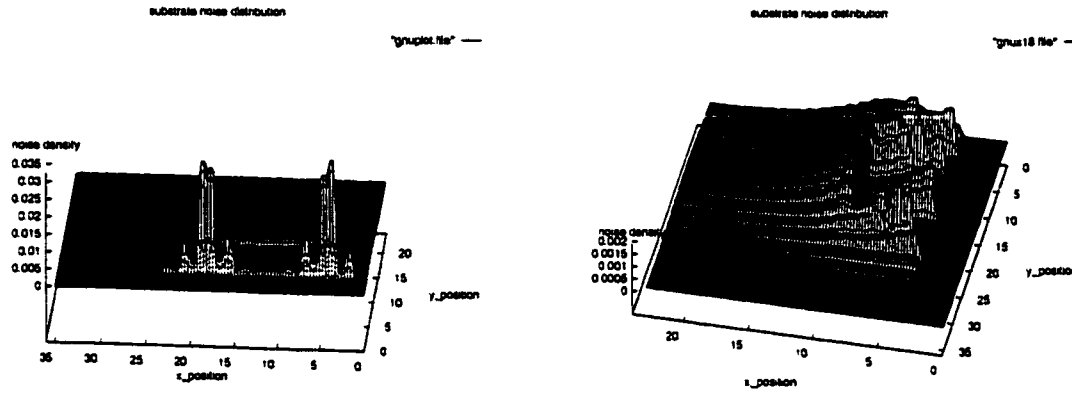
Figure 7.17: Substrate noise distribution for an epi technology for one substrate contact

This prediction is demonstrated in this section by deriving several three-dimensional substrate noise distributions. Also presented in this section are rules and methodologies for placing substrate contacts and rings in an epi technology to reduce and equalize the substrate noise. Practical substrate contact configurations are analyzed and conclusions are drawn for each case.

7.3.1 Substrate noise distributions for one individual substrate contact

Three-dimensional noise distributions for one individual substrate contact are illustrated in Fig. 7.17. Each of the noise distributions presented in this section uses a 1:10 ratio for the epi layer resistivity to the bulk layer resistivity. Note in Fig. 7.17a the high noise density where the noise enters the substrate (at the noise source) and leaves the substrate (at the substrate contact connected to GND). Note that for the same distance between the noise source and the substrate contact, as in a non-epi technology, the noise spikes that occur at the input and output are larger in an epi technology than in a non-epi technology. This behavior occurs because the noise travels predominantly through the lower resistivity path (*i.e.* through the bulk). Also note the constant noise distribution at the substrate surface, as in a non-epi technology. However, the noise density at the substrate surface is much smaller than for a non-epi technology (1:10 or less is typical), since the highest noise density is at the interface between the epi layer and the bulk. Eliminating the large input and output noise densities, note the symmetric noise distribution as shown in Figs. 7.17b, 7.17c, and 7.17d, *i.e.*, similar to the non-epi case with the highest noise density at the epi-bulk interface. Note also the gradual decrease of the noise density starting from the substrate surface and

moving into the epi layer, as well as into the bulk layer, starting from the bulk-epi interface.



(a) Main front view

(b) Magnified lateral-front view

Figure 7.18: Substrate noise distribution for an epi technology when the substrate contact is closer to the noise source

Noise distributions where the output node is closer to the input node are shown in Fig. 7.18. Note the higher noise density at the substrate surface and at the epi-bulk interface as compared to Fig. 7.17. Also note that the noise does not propagate along the opposite side of the substrate contact with respect to the noise source (at the substrate surface as well as at the epi-bulk interface).

The voltage distribution at the substrate surface is similar to the voltage distribution illustrated in Fig. 7.6. However, the noise spikes, V_1, $V_2 - V_1$, $V_4 - V_3$, and $V_5 - V_4$ (see Fig. 7.6), are larger than for a non-epi technology, while the noise nonuniformity in region 4 (expressed as the slope "b") is smaller than for a non-epi technology. This noise distribution for an epi technology, as shown above, describes an important difference as compared to a non-epi technology. This difference can be summarized by the following characteristics: 1) the noise

magnitude affecting the sensitive circuitry is larger for an epi technology than for a non-epi technology, and 2) the noise is more uniform for an epi technology than for a non-epi technology. As shown in Chapter 5, a uniform noise, even if large in magnitude, is preferable to a non-uniform noise, even if small in magnitude, in terms of the likelihood of inducing a parasitic transition.

Similar to a non-epi technology, if the sensitive circuitry (with no substrate contacts) is placed in region 4 of the substrate (see Fig. 7.6), the transistors are affected by a variable potential; however, this variable potential is much smaller than in a non-epi technology. If the sensitive circuitry is placed in region 1, the transistors are affected by an approximately constant potential V_2 (see Fig. 7.6), which however is larger than in a non-epi technology.

An important insight from this discussion is that epi technologies offer a more uniform noise, even if larger in magnitude than in non-epi technologies. This characteristic is valid in region 1 as well as in region 4 (see Fig. 7.6), benefiting the noise behavior of digital circuits.

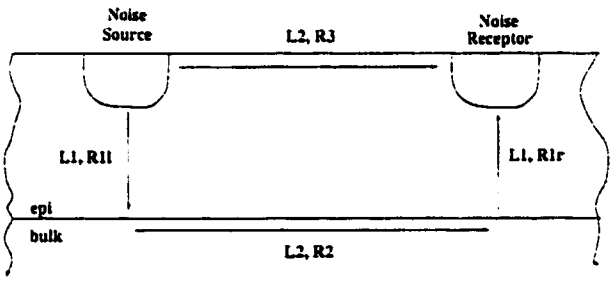


Figure 7.19: Resistance distribution between the noise source and a substrate contact for an epi technology

Fig. 7.19 is useful in determining first order equations that describe an efficient placement of the substrate contacts in an epi technology. The resistivity of the

epi layer is assumed to be k times the resistivity of the bulk,

$$\rho_{epi} = k\rho_{bulk}. \tag{7.2}$$

In Fig. 7.19 L is the distance and R is the resistance from point A to point B. As shown in Fig. 7.19, the noise path from the noise source to the noise receptor may be through the bulk at the epi-bulk interface or the epi layer along the substrate surface. The resistance from the noise source to the noise receptor through the bulk is

$$R_b \propto 2kL_1\rho_{bulk} + L_2\rho_{bulk} = \rho_{bulk}(2kL_1 + L_2), \tag{7.3}$$

assuming $R_{1l} = R_{1r}$ (see Fig. 7.19). The resistance from the noise source to the noise receptor through the epi layer is

$$R_e \propto kL_2\rho_{bulk}. \tag{7.4}$$

The noise propagates primarily through the bulk if

$$R_b \ll R_e, \tag{7.5}$$

and propagates primarily through the epi layer if

$$R_e \ll R_b, \tag{7.6}$$

depending upon L_1 which is the thickness of the epi layer and L_2 which is the distance between the noise source and the noise receptor.

As noted in the three-dimensional noise distributions shown in Figs. 7.17 and 7.18, due to the low resistivity of the bulk, the noise propagates uniformly through the bulk into the entire substrate, affecting the sensitive circuitry with a high noise amplitude signal. The noise amplitude is large but uniform, since the

low resistivity bulk introduces minimal attenuation as the distance from the noise source to the noise receptor increases. A uniform noise, as discussed previously, is beneficial for the noise behavior of the digital circuits. In addition to a uniform noise, a small noise amplitude is also desired. To reduce the noise amplitude, a possible method is to place substrate contacts to reduce the noise that reaches the bulk. This strategy is equivalent to diverting a portion of the noise from the bulk through the epi layer and can be described by satisfying (7.6). Condition (7.6) is best satisfied if the substrate contact is placed at the minimum possible distance from the noise source (which is a noisy drain). As discussed for the non-epi case, the closest substrate contact to the noisy drain can be placed with the source terminal of the noisy drain (transistor) as shown in Fig. 7.7. This substrate contact placement strategy is also effective for an epi technology. In addition to placing the substrate contact as described above, condition (7.6) can be maximized through several methods:

- Increase the substrate thickness (L_1 in Fig. 7.19). However, this technique requires adjustments in the process technology. Also, due to the thicker epitaxial layer, the high voltage devices have better performance but the performance of the low voltage devices are degraded. A tradeoff therefore exist. The thickness of the epi layer should be chosen to provide an optimal compromise between the performances of the high voltage devices and the low voltage devices that satisfy the application specific requirements.

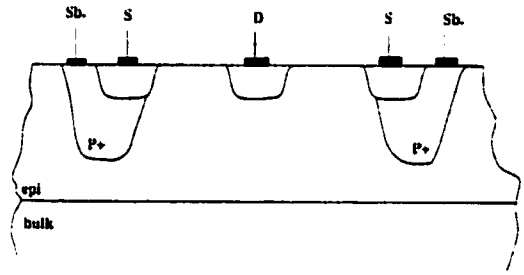
- Diffuse the substrate contact deeper into the epi layer, as shown in Fig. 7.20a.

- Create an extra buried layer below the noise source, as shown in Fig. 7.20b. This method degrades the performance of the high voltage devices due to the thinner epi layer.

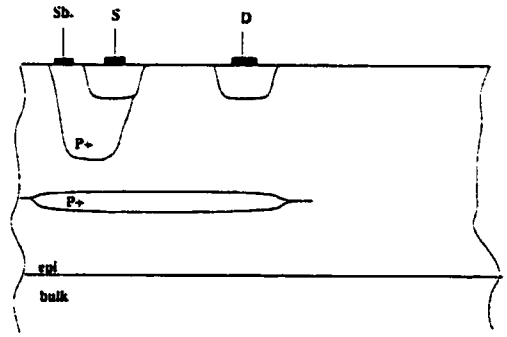
- Design the high voltage devices with minimal design overhead (such as, for example, a larger channel than is needed), that would increase the distance from the drain to the source.

- Surround the drain with the source and the substrate contact to minimize R_3 (see Fig. 7.19), as shown in Fig. 7.20a.

- Use wide substrate contacts near the drain to decrease R_3. However, a negative effect of this strategy is that R_{1r} (see Fig. 7.19) is also decreased.



a) Deeper diffusion for substrate contacts surround the drain

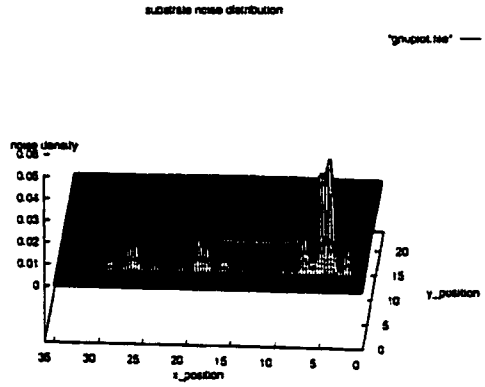


b) An additional buried layer is provided below the noise source

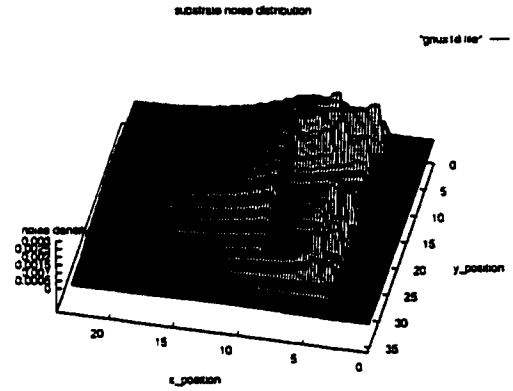
Figure 7.20: Different process adjustments to maximize condition (7.6): a) deeper diffusion for substrate contacts and b) additional buried layer.

If the substrate contact is placed far from the immediate vicinity of the source of the power transistor, the noise is injected primarily within the bulk, thereby

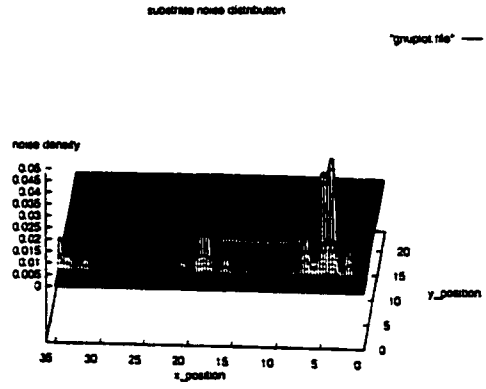
affecting the noise sensitive circuitry with a high amplitude noise signal throughout the chip. Also, a larger body effect is created for the power transistor, inducing V_{noise} effects (see Section 6.1.4), which forward biases the source junction.



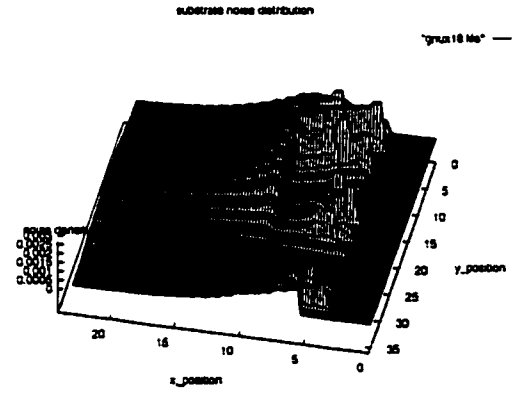
(a) Main front view



(b) Magnified lateral-front view



(c) Main front view



(d) Magnified lateral-front view

Figure 7.21: Substrate noise distribution for an epi technology when two substrate contacts are used. The distance between the noise source and the first substrate contact is constant, while the distance between the two substrate contacts is smaller for the cases shown in a and b than for the cases shown in c and d.

7.3.2 Substrate noise distributions for multiple individual substrate contacts

Several experiments have been performed to determine the effects of the placement of multiple substrate contacts at different distances from the noise source. Noise distributions with two substrate contacts are presented in Fig. 7.21. In Figs. 7.21a, 7.21b, 7.21c, and 7.21d, the distance between the noise source and the first substrate contact is constant, while the distance between the substrate contact 1 and substrate contact 2 is smaller for the configurations shown in Figs. 7.21a and 7.21b than for the configurations shown in Figs. 7.21c and 7.21d.

Based on these noise distributions, a similar voltage distribution as shown in Fig. 7.9 has been developed for the two substrate contact case in an epi technology. The differences between the non-epi and epi cases consist of larger noise spikes (such as V_1, $V_2 - V_1$, and $V_7 - V_6$, see Fig. 7.9), and smaller slopes, such as "b" and "d" (see Fig. 7.9). Note that it is possible to further reduce the noise spike near the second substrate contact by properly placing the second substrate contact, reducing the overall noise received by the sensitive circuitry. It is also possible to reduce the noise density within the bulk between SC1 and SC2 by careful placement of the substrate contacts.

Necessary conditions for an efficient placement of the second substrate contact and for placing additional substrate contacts are explained with reference to Fig. 7.22. As shown in Section 7.3.1, SC1 must be placed such that

$$R_2 \ll R_3 + 2R_1. \tag{7.7}$$

If SC2 is placed such that

$$R_4 \ll R_5 + 2R_1, \tag{7.8}$$

the situation is equivalent to placing a single wide substrate contact rather than two substrate contacts, SC1 and SC2. This choice has already been described in Section 7.3.1. It is shown that by employing a wide substrate contact, the noise is reduced by decreasing the effective resistance R_2 as compared to using only one individual substrate contact or a thin substrate contact.

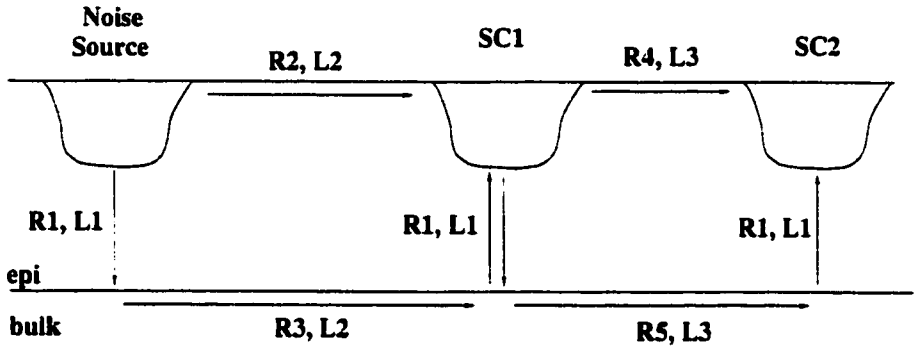


Figure 7.22: Efficient placement of multiple substrate contacts in an epi technology

If (7.8) is not satisfied, the distance L_3 is much larger than L_1. To generalize this discussion in order to derive the appropriate condition for placing any subsequent pair of substrate contacts, R_m is defined as the minimum resistance between R_2 (representing the case when the noise propagates primarily through the epi layer) and $R_3 + 2R_1$ (representing the case when the noise propagates primarily through the bulk),

$$R_m = Min\{R_2, 2R_1 + R_3\}. \tag{7.9}$$

According to Fig. 7.21, the noise at SC2 decreases as the distance between SC1 and SC2 increases. According to Fig. 7.22, this increase is equivalent to

$$R_m \ll R_5 + R_1 \tag{7.10}$$

when (7.8) is not satisfied. Condition (7.10) is equivalent to placing SC2 at a large distance from SC1. Note that in order to satisfy (7.10), L_3 (R_5) must be

considerable as compared to either L_2 (R_2), or to L_1 (R_1) and/or L_2 (R_2). Note also that in (7.10), the bulk resistance corresponding to the distance L_3, R_5, is compared to the epi layer resistance, R_2 and/or R_1. In order to obtain the same resistance through the bulk as through the epi layer, the distance through the bulk (L_3) must be ρ_{epi}/ρ_{bulk} times larger than the equivalent distance through the epi layer. To obtain a significant reduction in substrate noise, $R_5 + R_1$ must not only be comparable to R_m but should be much larger, translating to a large R_5 (L_3). A large L_3 requires a significant amount of on-chip area. Therefore, in an epi technology, multiple substrate contacts, while reducing the substrate noise, are not efficient from an area point of view. Large distances between adjacent substrate contacts are required to significantly reduce the noise. Tradeoffs are possible depending upon the particular requirements of each circuit. A second substrate contact immediately following the substrate contact near the source is efficient since R_m is small. Therefore, the distance between the substrate contact near the source terminal and the second substrate contact does not need to be large. Subsequent substrate contacts would require a significant amount of area to efficiently reduce the noise.

Note that important differences exist as compared to placing multiple substrate contacts in a non-epi technology. Due to the low resistivity of the bulk, the multiple substrate contacts in an epi technology are far less efficient than in a non-epi technology since the distance between subsequent substrate contacts must be much larger than in a non-epi technology. Alternatively, a comparable distance produces a much smaller noise reduction in an epi technology than in a non-epi technology (see Fig. 2.9a for distances greater than 50 μm).

7.3.3 Substrate contacts versus rings in an epi technology

In contrast to non-epi technologies, rings or large substrate contacts are not as beneficial in an epi technology. A ring surrounding the source terminal, as discussed in the previous section, reduces the noise by providing a smaller resistance R_2 (see Fig. 7.22). However, a ring or a large substrate contact rather than a second individual substrate contact decreases the bulk resistance R_5 (see Fig. 7.22) due to the large area of the large substrate contact or ring. Therefore, to reduce the noise with the same efficiency for a ring as for an individual substrate contact, the distance between the first substrate contact and the ring or the large substrate contact (L_3, see Fig. 7.22) must be further increased. The increased area for multiple substrate contacts as demonstrated in Section 7.3.2 is further accentuated by this approach. Summarizing, in an epi technology, since the low resistivity bulk creates a uniform substrate noise over long distances from the noise source, the technique of using individual substrate contacts for each transistor or for a small and symmetric group of transistors belonging to a sensitive circuit is preferable than using large substrate contacts or rings. This technique offers improved noise uniformity for the sensitive transistors as well as reduced noise as compared to using rings or large substrate contacts over similar distances L_3 (see Fig. 7.22).

7.3.4 Significant issues for substrate contact placement

The issues discussed for a non-epi technology are briefly reviewed for an epi technology, highlighting the major differences.

1. **Distribution of substrate resistance**

   The placement of substrate contacts depends significantly on the relationship among the R_1, R_2, and R_3 resistances (see Fig. 7.22). These resistances depend upon the doping concentrations of the epi and the bulk as well as the physical distances between the noise source and the substrate contacts and/or between two adjacent substrate contacts (see Sections 7.3.1 and 7.3.2). The appropriate ratio of these resistances, as described in Section 7.3.1 and Section 7.3.2, strongly affects the utility of the substrate contacts (individual or large) and rings.

2. **Multiple noise sources**

   For an epi technology, the placement of substrate contacts surrounding the source terminal, as shown in Fig. 7.20 is necessary to reduce the noise. Since the distance has far less importance in an epi technology due to the low resistivity path through the bulk, a ring surrounding multiple noise sources is not affected by a nonuniform noise distribution, as shown in Fig. 7.14b. Rather, the distribution is quite uniform. However, a ring surrounding multiple noise sources does not have a major effect in reducing the noise either. The only beneficial effect of such a ring is that it is equivalent to increasing the width of the rings associated with the source terminals of each noise source, thereby reducing the noise by creating a smaller equivalent resistance R_3 (as shown in Fig. 7.19).

3. **Physical design aspects of a ring**

As shown in Fig. 7.15, if the metal following the $P+$ ring diffusion is interrupted for reasons such as routing, parasitic resistances are introduced among the different sections of the ring, creating noise problems. While the phenomenon also remains valid for an epi technology, the importance is reduced in an epi technology due to reasons such as:

- The low resistivity of the bulk creates a uniform noise distribution over large distances within the substrate and across the rings.
- Any resistance (see Fig. 7.15) is short-circuited by the bulk, particularly when R is greater than $2R_1 + R_2$ (see Fig. 7.19).
- The aforementioned noise uniformity and short-circuit effect of the bulk make the gaps in the metal following the ring less important by reducing the voltage difference between the two interrupted sections of the ring.

However, a safe and effective layout design in an epi technology should use the strategies recommended for a non-epi technology to reduce or eliminate the parasitic effect of an interrupted metal.

4. **Ring surrounding the sensitive circuitry**

A ring surrounding the sensitive circuitry provides no major benefits in a non-epi technology (see Section 7.2.4). For an epi technology, a ring is also not useful. However, the reasons are different as compared to a non-epi technology, and are explained in Sections 7.3.2 and 7.3.3. Therefore, for an epi technology as for a non-epi technology, a ring surrounding the sensitive circuitry is not particularly beneficial.

7.3.5 Conclusions

To summarize this analysis of substrate contact placement in an epi technology, the following general remarks can be stated.

- A ring closely surrounding the noise source and attached to the source terminal of the noise source is highly recommended.
- A second ring following and surrounding the initial ring is recommended if the added area is acceptable.
- No additional rings or large substrate contacts are recommended.
- Individual substrate contacts are recommended for each of the sensitive transistors.

As a final remark, the low resistivity bulk of an epi technology is the principal reason for the major differences between an epi technology and a non-epi technology in terms of the substrate noise transmission process and the proper placement of substrate contacts. While the noise levels are larger in an epi technology, the noise is more uniform and significantly more independent of the distances across the substrate.

7.4 Graphical representation of noise variation as a function of substrate contact placement in epi and non-epi technologies

The goal of this section is to summarize in graphical form the most important conclusions regarding the noise level that results from different substrate contact placement conditions and substrate dopings in both epi and non-epi technologies. The conditions in which the two graphs presented here (one for epi technologies and one for non-epi technologies) are derived, are:

- Two substrate contacts, SC1 and SC2, are placed near a noise source NS.
- The noise at the second substrate contact SC2, which is the contact farthest from the noise source, is depicted in each graph.
- The abscissa of both graphs logarithmically describes the noise at SC2. Since the technology factors give such a wide spread for the actual noise levels, the noise level variation is provided in relative units.
- The ordinate for the non-epi technology logarithmically describes the ratio of the distance between the noise source and SC1, D_{NS-SC1}, and the distance between SC1 and SC2, $D_{SC1-SC2}$. For an epi technology, the ordinate logarithmically describes the ratio of the epitaxial layer thickness L_{epi} and the distance between SC1 and SC2, $D_{SC1-SC2}$.
- Variations in the noise level at SC2 for different substrate contact placement conditions are shown. The trend in the noise level variation with substrate doping level is also discussed. For each of the curves shown in the two graphs,

D_{NS-SC1} is maintained constant. Due to the many technological factors that influence the actual noise levels as well as the exact noise variations with the different substrate contacts placement conditions, the curves shown in the two graphs are intended not to be precise but to demonstrate general trends.

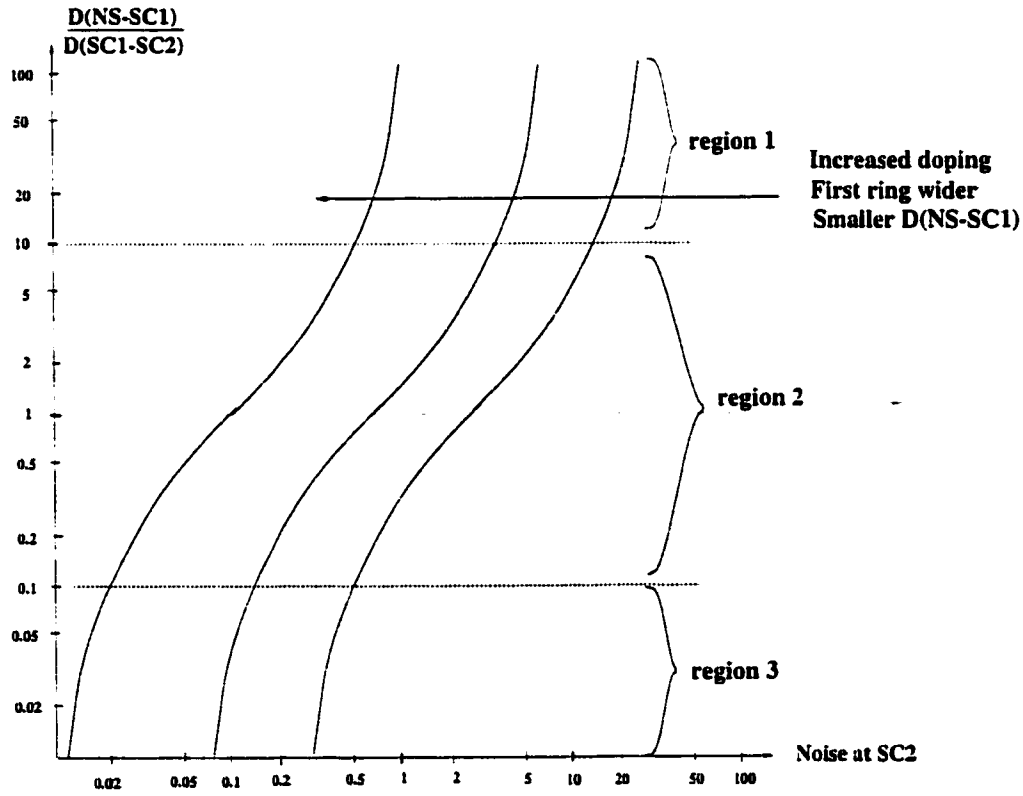


Figure 7.23: Noise variation for non-epi technologies depending on substrate contact placement

The noise variation graph for non-epi technologies is shown in Fig. 7.23. Each curve is composed of three distinct regions:

- The first region is for a large ratio of the two distances. In this region, SC2 is close to SC1, and therefore, as mentioned in Section 7.2, the second substrate contact does not significantly reduce the noise.

- SC2 becomes more efficient in reducing the noise level in region 2.

- The noise reduction saturates in region 3, where the distance between SC1 and SC2 as compared to the distance between NS and SC1 becomes large. In this range of distances, the noise is practically constant independent of distance, similarly to region 1, since SC1 collects most of the noise generated by NS, making the influence of distance between SC1 and SC2 insignificant from a noise reduction point of view.

Note that region 2 is the most efficient region for noise reduction. Particularly for equal D_{NS-SC1} and $D_{SC1-SC2}$ distances, an effective tradeoff between the utilized area and the noise reduction is achieved. Note that, as described in [69, 70], the noise decreases with distance in a non-epi technology. Note also in Fig. 7.23 that if a constant noise (current) is injected into the substrate independent of the substrate doping, the noise decreases as the substrate doping increases [70], since the noise produces a smaller voltage drop. Note, however, that the noise source may generate a different noise level depending upon the substrate doping, or the same noise level may affect a sensitive circuit differently depending upon the substrate doping. If the SC1 ring is wider and the SC2 ring is thinner while maintaining the same D_{NS-SC1} and $D_{SC1-SC2}$ distances, the noise at SC2 decreases, as discussed in Section 7.2. If D_{NS-SC1} decreases while maintaining the same distance ratio, the noise decreases since SC1 collects more current because SC1 is closer to the noise source. The noise decreases when either the substrate doping decreases and/or unequal rings are used due to a reduction in $R1$ and a decrease in the R1/R2 ratio (see Section 7.2). Note that it is more efficient in terms of both a noise reduction and an area savings points of view to place three rings at equal distances rather than two rings at a large distance. Practically, the

noise is reduced as a square when three rings are used as compared to the noise reduction obtained with two rings. Alternatively, if the noise reduction at SC2 where $D_{NS-SC1}/D_{SC1-SC2} = 1$ is $\propto k$ (see Fig. 7.23), the noise reduction at SC3 where $D_{SC1-SC2}/D_{SC2-SC3} = 1$ is $\propto k^2$. This explanation assumes that for the third ring SC1 behaves as the noise source and SC2 behaves as the first ring, and neglects the influence of NS. For large distances between NS, SC1, SC2, and SC3, this approximation is accurate. To obtain a similar k^2 noise reduction with two rings, a much larger area is required since $D_{SC1-SC2}$ must be considerable (see Fig. 7.23). Since the noise reduction saturates for large distances (see Fig. 7.23), a k^2 reduction may not be achievable with two rings.

The noise variation graph for epi technologies is shown in Fig. 7.24. Seven distinctive curves are shown, each curve depicting significant conditions for the noise level as a function of the substrate contacts placement:

- Curve No. 1 describes the condition where $\rho_{epi}/\rho_{bulk} = 10$ and $D_{NS-SC1} \gg L_{epi}$. Note that a noise reduction is observed when $D_{SC1-SC2} \geq L_{epi}$. A very weak noise reduction is noted when $D_{SC1-SC2} \leq L_{epi}$.

- Curve No. 2 describes the condition where $\rho_{epi}/\rho_{bulk} = 10$ and $D_{NS-SC1} = L_{epi}$. Note an increased noise reduction when $D_{SC1-SC2} \leq L_{epi}$ and a similar noise reduction trend as for curve No. 1 when $D_{SC1-SC2} \geq L_{epi}$.

- Curve No. 3 describes the condition where $\rho_{epi}/\rho_{bulk} = 10$ and $D_{NS-SC1} = 0.1L_{epi}$. Note the pronounced noise reduction when $D_{SC1-SC2} \leq L_{epi}$ and a weak noise reduction than exhibited by curve No. 1 and 2 when $D_{SC1-SC2} \geq L_{epi}$. The increased noise reduction for curves No. 2 and 3 is due to SC1 reducing the noise injected into the substrate as discussed in Section 7.3.

Not surprisingly, the efficiency of SC1 increases as SC1 is placed closer to the noise source, as described by (7.3).

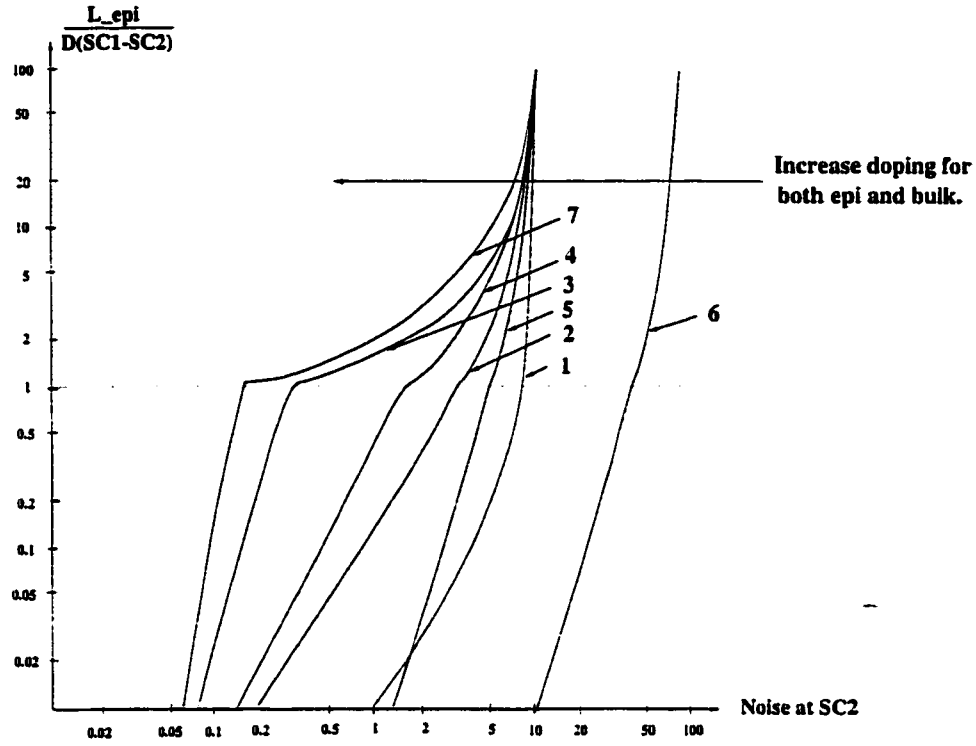


Figure 7.24: Noise variation for epi technologies depending upon the placement of the substrate contacts

- The situation where ρ_{bulk} is increased three times while maintaining ρ_{epi} constant is depicted in curve No. 4. The curve describes the condition where $\rho_{epi}/\rho_{bulk} = 3$ and $D_{NS-SC1} = L_{epi}$. Note that a higher the noise reduction is achieved as compared to curve No. 2. This behavior is expected since the noise spreads less through the bulk than for curve No. 2 due to the decreased resistivity ratio. The situation is similar to the non-epi case when $\rho_{epi}/\rho_{bulk} = 1$. The noise reduction for a non-epi technology is larger in a similar situation, since the noise spreads through the bulk in the epi technology. However, the noise decrease does not saturate for large distance

ratios in an epi technology as in a non-epi technology. Therefore, at large distances, the noise decrease may be greater than for similar distances in a non-epi technology.

- The situation where ρ_{bulk} is decreased ten times while maintaining ρ_{epi} constant is shown in curve No. 5. The curve describes the condition where $\rho_{epi}/\rho_{bulk} = 100$ and $D_{NS-SC1} = L_{epi}$. Note that, as expected, the noise spreads more easily through the low resistivity bulk. Therefore, the noise reduction is smaller than for curve No. 2 for both $D_{SC1-SC2} \leq L_{epi}$ and $D_{SC1-SC2} \geq L_{epi}$.

- For curve No. 6, ρ_{bulk} is maintained constant and ρ_{epi} is increased ten times. Accordingly, $\rho_{epi}/\rho_{bulk} = 100$ also, while $D_{NS-SC1} = L_{epi}$. The curve is similar to curve No. 6, however, a higher noise is produced. The higher noise is due to the increase in ρ_{epi}, which for the same noise (current), produces a larger voltage drop.

- The effect of a wider SC1 ring is depicted in curve No. 7. The conditions are similar to curve No. 3, while the SC1 ring is double in width (see Section 7.3). Note that, as discussed in Section 7.3, the noise is further attenuated as compared to curve No. 3 when $D_{SC1-SC2} \leq L_{epi}$. The noise decreases less than curve No. 3 when $D_{SC1-SC2} \geq L_{epi}$ due to the excellent shielding effect of the SC1 ring which collects most of the noise. This behavior makes the distance less significant when $D_{SC1-SC2} \geq L_{epi}$.

- All the curves shift to the left (less noise) as the doping of both the epi and bulk increase at the same rate, increasing both ρ_{epi} and ρ_{bulk}. The ρ_{epi}/ρ_{bulk} ratio is maintained constant.

Note that, as discussed in Section 7.3, the most effective situations for placing substrate contacts to reduce noise is to increase the epi layer thickness (L_{epi}), decrease D_{NS-SC1}, use a wider SC1 ring, and place the second SC2 ring or individual substrate contact at $L_{epi}/D_{SC1-SC2} \approx 1$ or larger. Note that, as compared to a non-epi technology where the use of three rings is effective in reducing the noise, the use of three rings has no effect on an epi technology due to the low resistivity path through the bulk (see Section 7.3 for more detail).

7.5 Deriving a uniform power distribution shape

As described in Chapter 6, the power dissipation distribution over the surface of a power resistor of a TIJ printer head is the useful output signal of this circuit application. A power level within a specific, well defined range over the entire surface of the power resistor is required for the heat to be appropriately transfered to the ink. The transferred heat insures a uniform and timely spread of the ink onto the printing surface. As described in Chapter 6, the substrate noise alters the power level, as well as the power uniformity over the resistor surface. These parasitically induced nonuniformities in the power distribution within the resistor may overheat or underheat the ink, producing a low quality printing. The poor printing may occur by printing a dot when a dot is not required due to overheating the ink, by not printing a dot when a dot is required due to overheating and early vaporization of the ink or due to underheat and non-vaporization of the ink, or by printing a low quality dot due to an insufficient heat level.

Improving the substrate noise behavior of the digital control circuitry minimizes this problem. Further improvement results by insuring that under equilibrium conditions, a highly uniform power dissipation across the entire surface of the power resistor is achieved. This high power uniformity in equilibrium conditions minimizes the risk of high power non-uniformities during transient conditions, passing uniform heat to the ink.

To investigate possible resistor shapes which will produce a highly uniform power distribution, a model of the power resistor is developed. The power resistor is modeled as a resistive mesh, similar to the substrate model (see the resistive primitive shown in Fig. 7.2). A 38 volt power supply [95] is connected to the edge of the resistor mesh. Similar to the substrate noise distribution analysis, the files

generated by the Cadence Spectre simulator are processed by a C code program which calculates the power dissipated by each resistor within each resistive primitive. The average power for each resistive primitive is determined, permitting the power distribution over the entire surface of the power resistor to be produced.

Several resistor shapes have been analyzed. Three-dimensional power distributions for three representative resistor shapes are exemplified here. One resistor shape that generates a highly non-uniform but highly suggestive power distribution is a horseshoe shape. The second resistor is shaped as a square, and finally the third shape, which produces the most uniform power distribution, is a "T" shape.

7.5.1 A horseshoe shaped resistor

A horseshoe shaped resistor is shown in Fig. 7.25. 36 by 24 resistive primitives are used to model the horseshoe shaped resistor.

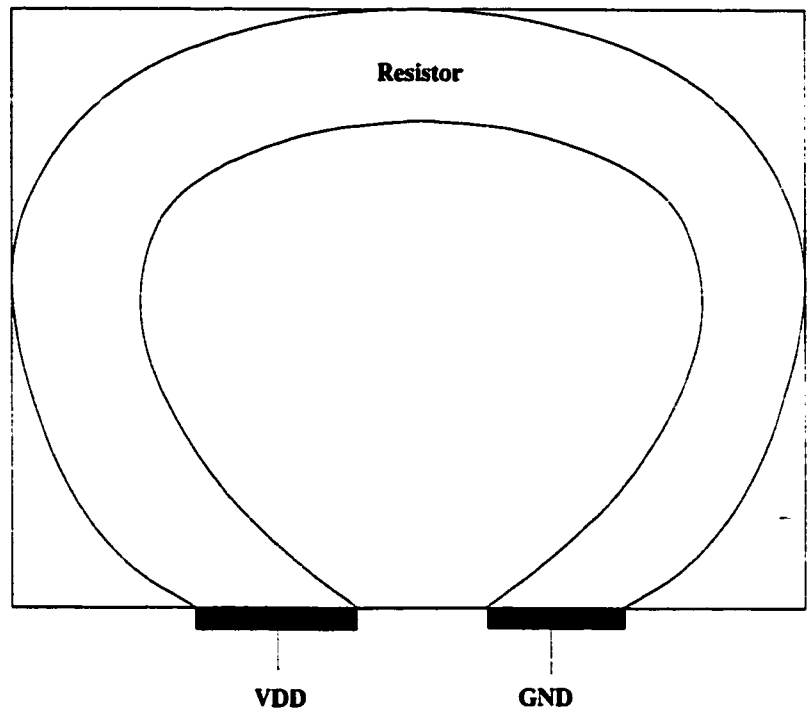
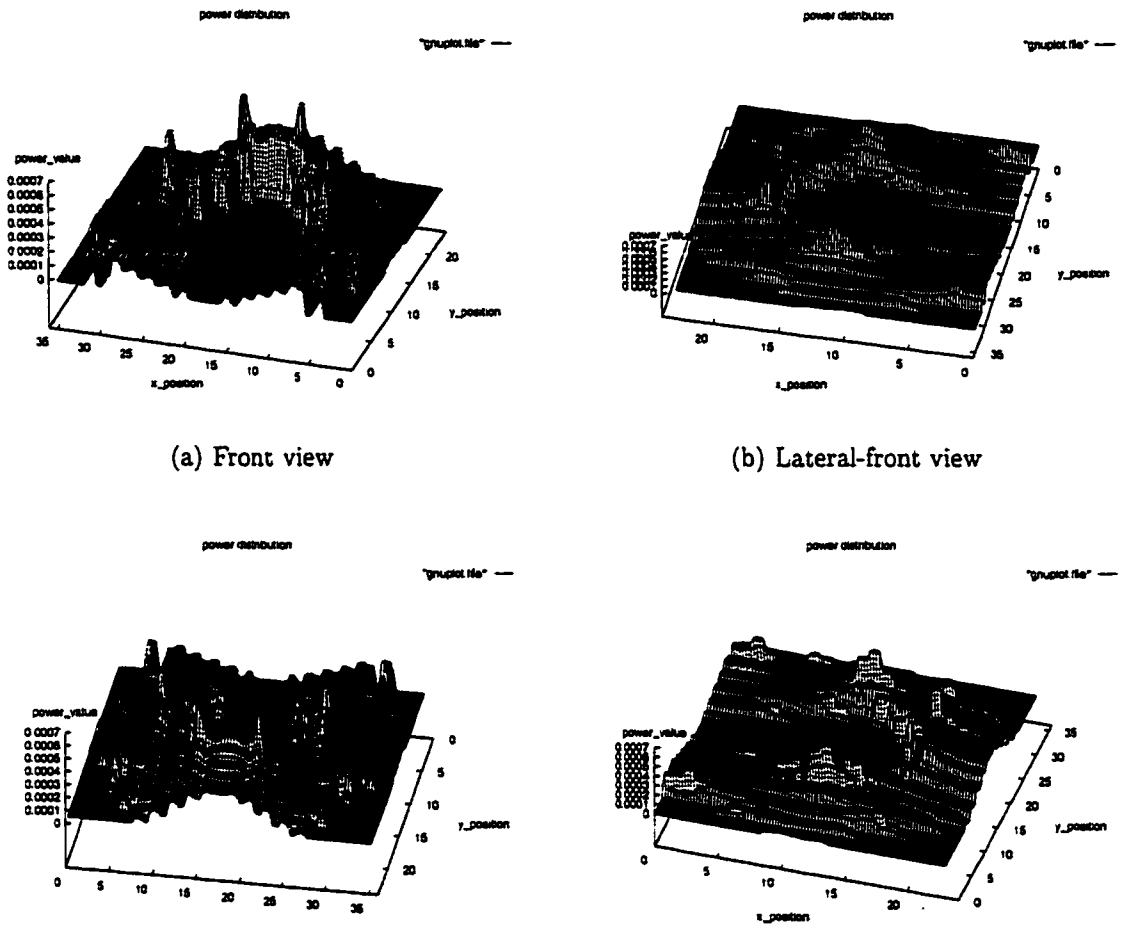


Figure 7.25: A horseshoe shaped resistor

The power distribution for this resistor shape is shown from different angles in Fig. 7.26. Note the highly nonuniform power distribution.



(a) Front view

(b) Lateral-front view

(c) Back view

(d) Lateral-back view

Figure 7.26: The power distribution for a horseshoe shaped resistor viewed from different angles

The information derived from an analysis of a horseshoe shaped resistor is that turns and corners within the resistor should be avoided in order to obtain a more highly uniform power distribution.

7.5.2 A square shaped resistor

A squared shape resistor is shown in Fig. 7.27. 36 by 24 resistive primitives are used to model the square shaped resistor. For additional accuracy, the metal resistance is included within the resistor model.

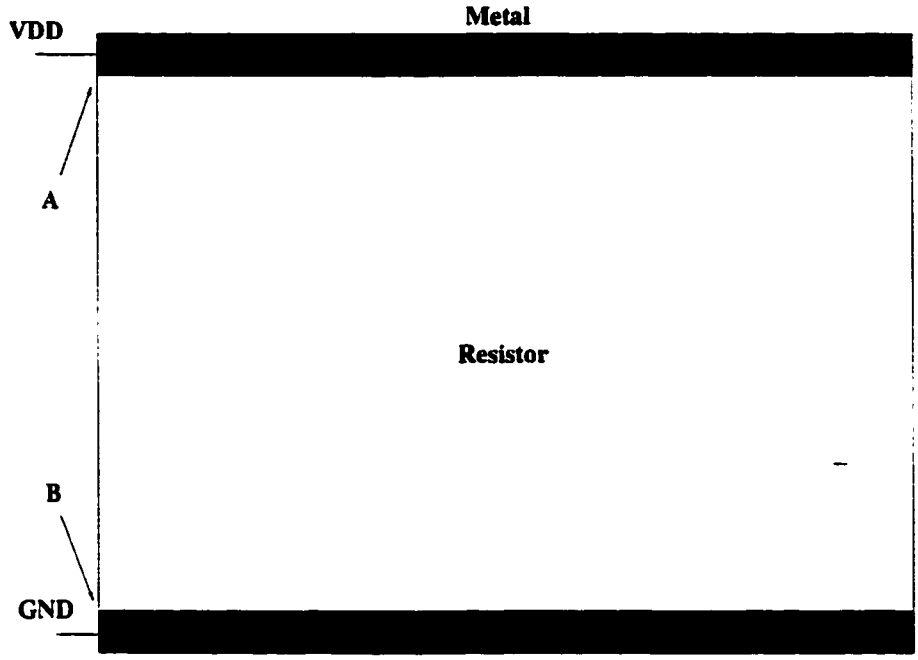
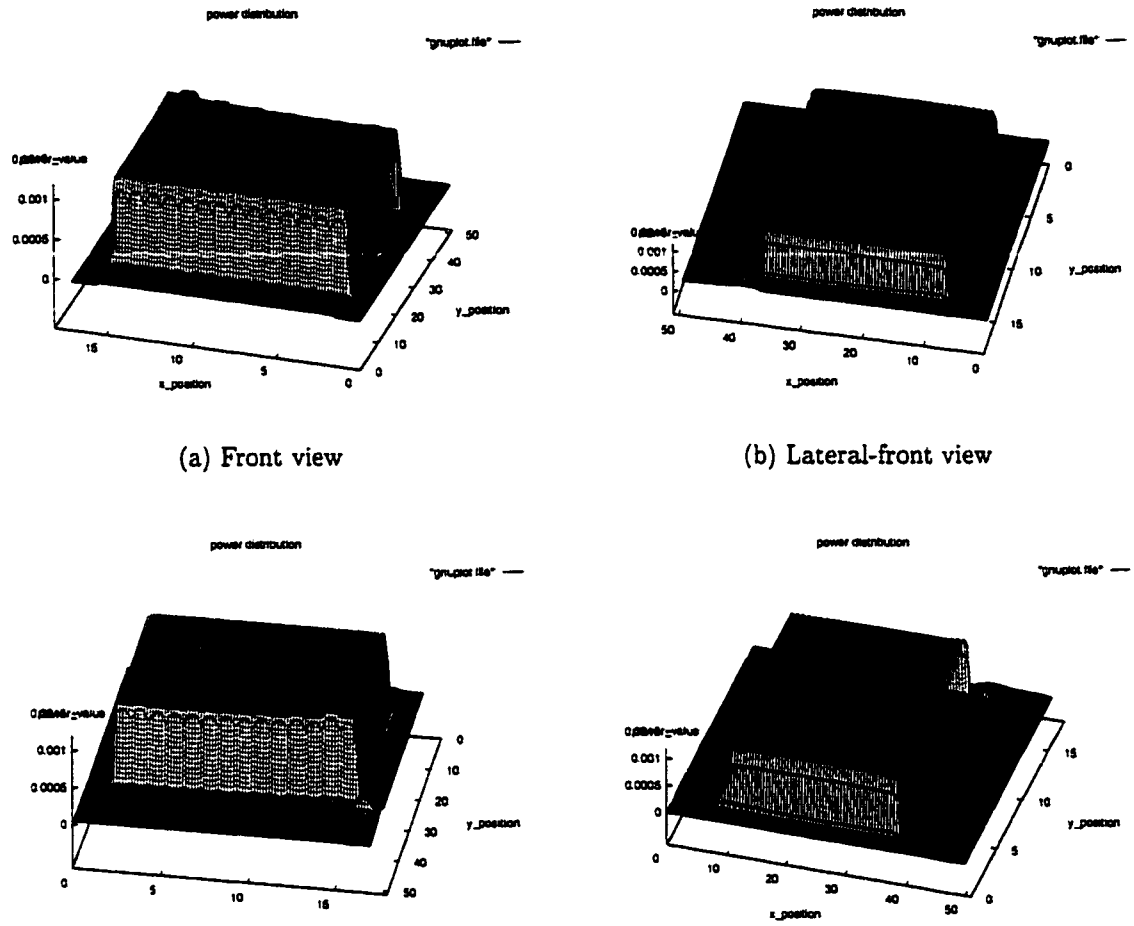


Figure 7.27: A square shaped resistor

The power distribution for a square shaped resistor is shown from different angles in Fig. 7.28. Note the nonuniformities produced at the metal-resistor interface, particularly at the A and B corners near V_{DD} and GND.



(a) Front view

(b) Lateral-front view

(c) Back view

(d) Lateral-back view

Figure 7.28: The power distribution for a square shaped resistor viewed from different angles

The information derived from an analysis of a squared shape resistor is that interfaces between the different materials should be avoided in the vicinity of the corners and turns in order to obtain a more highly uniform power distribution.

7.5.3 A "T" shaped resistor

A T shaped resistor is shown in Fig. 7.29. 36 by 24 resistive primitives are used to model the T shape. For additional accuracy, the metal resistance is included within the resistor model. There are several issues worth noting in order to obtain a highly uniform power distribution. The power supply is connected at both the left and right of the resistor. A metal buffer zone is placed near the corners and turns to avoid corner nonuniformities as noted in the square shaped resistor.

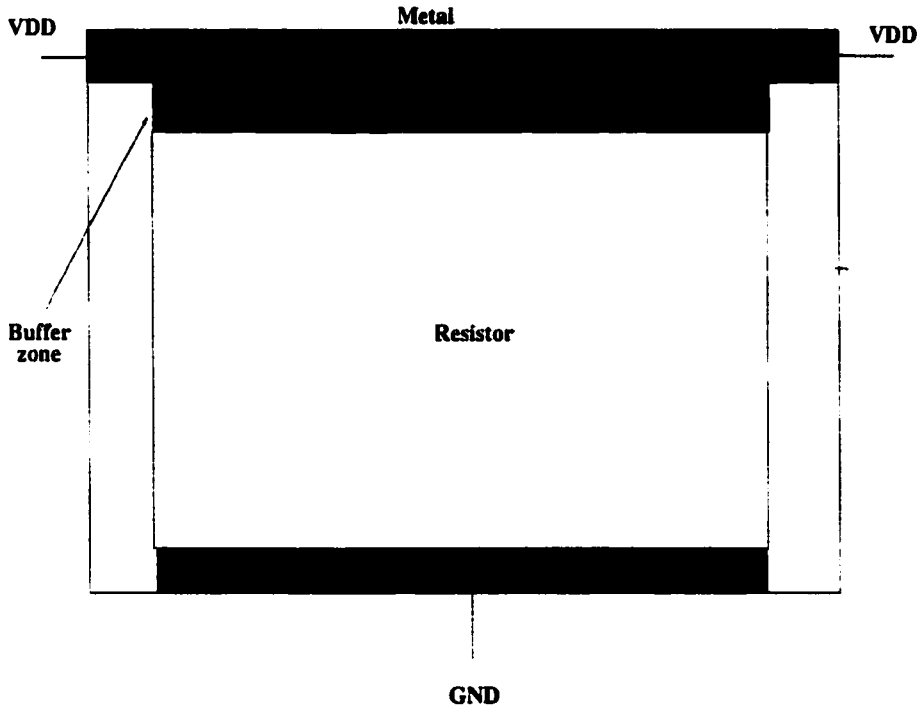
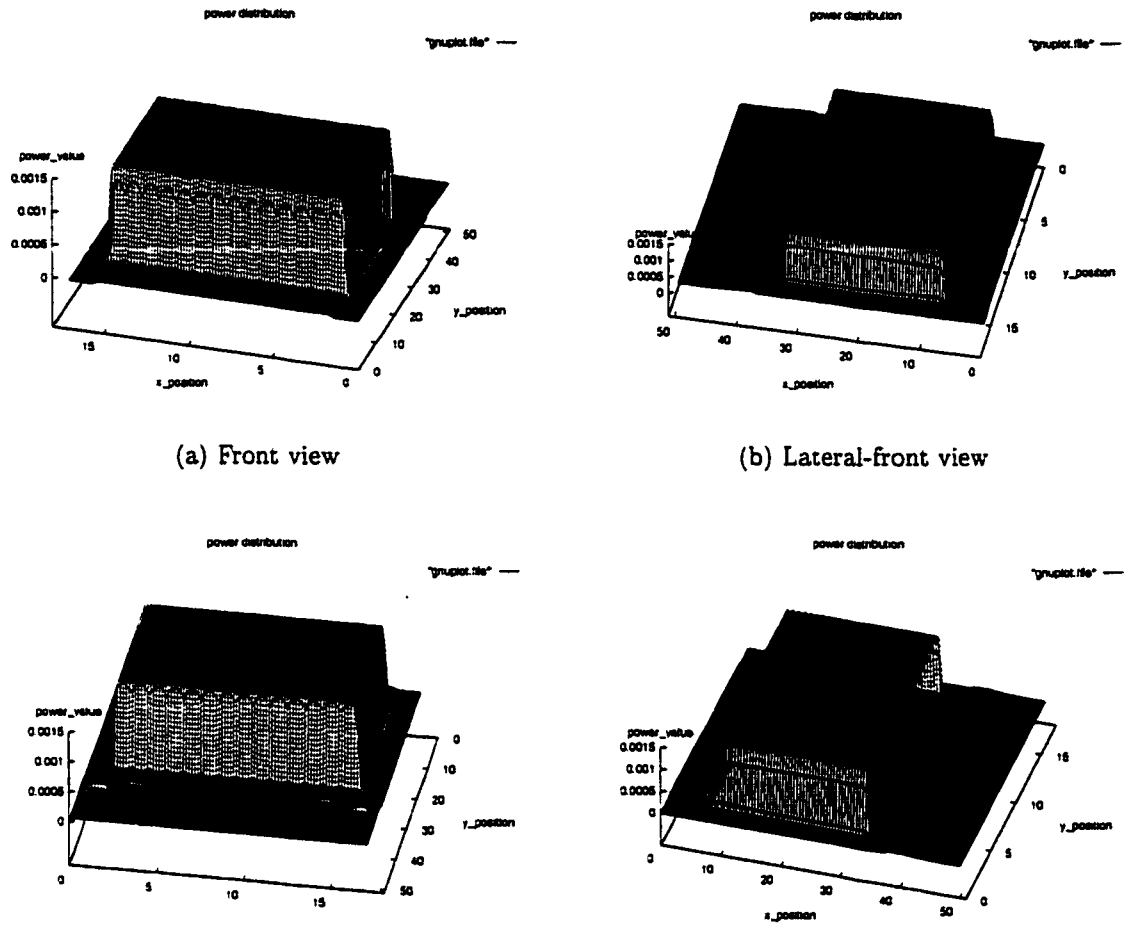


Figure 7.29: The T shaped resistor

The power distribution for a T shaped resistor is shown from different angles in Fig. 7.30. Note the uniform power distribution due to the aforementioned design precautions and conclusions drawn from the analysis of the previous two shapes.



(a) Front view

(b) Lateral-front view

(c) Back view

(d) Lateral-back view

Figure 7.30: The power distribution for a T shaped resistor viewed from different angles

The information derived from the analysis of a T shaped resistor is that with proper and careful design, a highly uniform power distribution can be successfully achieved.

Chapter 8

Substrate Coupling in CMOS Circuits

The behavior of both a CMOS inverter and a CMOS latch under the influence of substrate noise is analyzed in this chapter. Circuit simulations characterizing different noise conditions are described for a 2.5 μm CMOS technology. Focus is placed on the relationship between substrate coupling and the latch-up phenomenon.

Although the models, mechanisms, and characteristics discussed in Chapters 4, 5, and 6 describing the process in which a digital circuit may be affected by substrate noise remain valid for CMOS digital circuits, the focus of Section 8.1 is on providing a review and analysis of latch-up in CMOS technology that may be induced by substrate noise. A methodology to predict the likelihood of latch-up for any feature size technology is also described in Section 8.1. Technology, circuit, and physical design rules to minimize the likelihood of latch-up occurance are outlined. Circuit simulations characterizing a CMOS inverter and latch in a 2.5 μm technology are summarized in Section 8.2. These simulations describe the behavior of logic elements under the influence of substrate noise when none of the conditions to trigger the parasitic latch-up structure are satisfied. Design

recommendations for repeater insertion in a noisy environment are also provided in Section 8.2.

8.1 Latch-up in CMOS circuits [99]

Latch-up is a parasitic circuit effect specific to a PNPN structure such as in CMOS technology. Due to the effect of latch-up on circuit reliability (see Section 8.1.1), latch-up is a well investigated phenomenon. A variety of innovative process and circuit techniques have been developed to minimize (or eliminate) the occurance of latch-up [25–29, 63, 64, 90, 100–105]. A parasitic positive feedback circuit structure formed within the substrate, responsible for the latch-up phenomenon, can be triggered by substrate noise, therefore latch-up can be induced by substrate noise. Mixed-signal smart-power applications are particularly susceptible to substrate noise induced latch-up due to the high level of substrate noise present in these applications.

The most important aspects of latch-up, with particular emphasis on substrate noise induced latch-up, are reviewed in Section 8.1.1. Mathematical conditions describing the occurance of latch-up are discussed in 8.1.2. A strategy for estimating the likelihood of latch-up for different technologies is presented in Section 8.1.3. The primary techniques used to minimize latch-up are outlined in Section 8.1.4.

8.1.1 The latch-up phenomenon

The latch-up phenomenon is explained here with reference to Fig. 8.1. A circuit schematic of a CMOS inverter is shown in Fig. 8.1a. Latch-up can appear between any pair of NMOS and PMOS transistors connected between V_{DD} and GND,

independent of the gate connections. A cross-section of a pair of MOS transistors is shown in Fig. 8.1b. The schematic depicts a parasitic circuit connected between the power and ground rails composed of an NPN bipolar transistor, a PNP bipolar transistor, and two resistors.

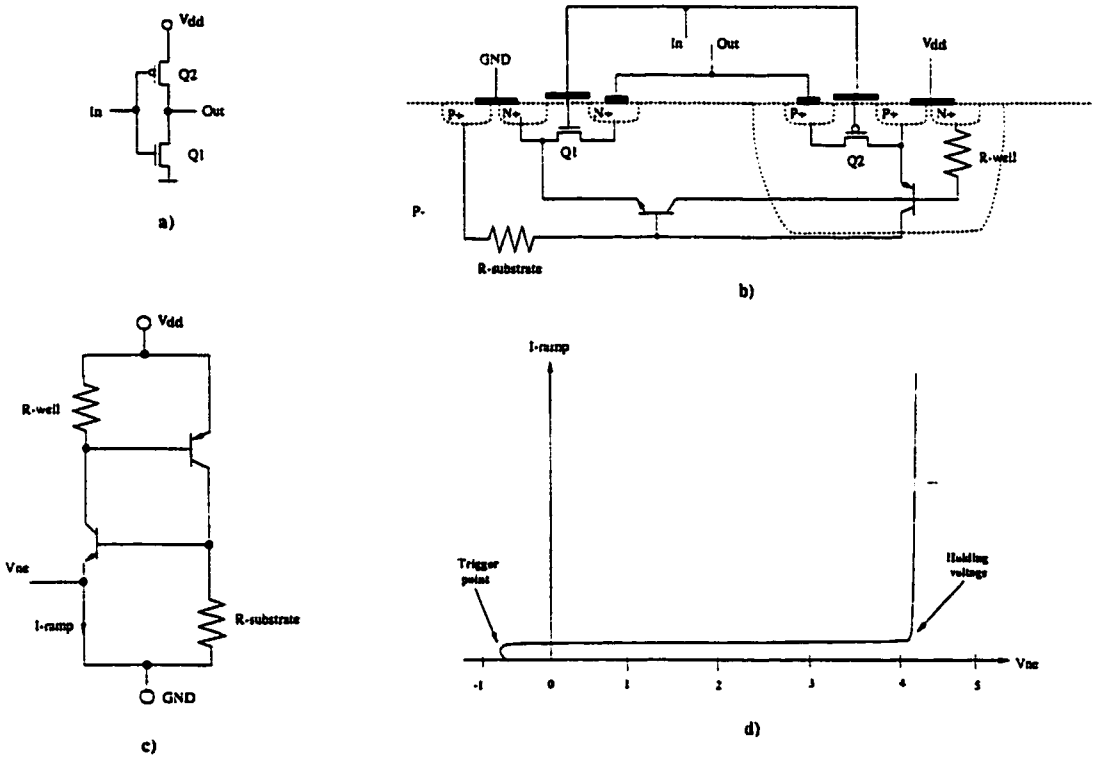


Figure 8.1: The latch-up phenomenon: a) A CMOS inverter, b) Process cross-section of an N-well CMOS inverter, c) An SCR parasitic circuit schematic of an N-well CMOS structure, and d) The $I - V$ characteristic of the parasitic circuit.

The parasitic circuit, equivalent to a parasitic silicon controlled rectifier (SCR) thyristor structure, is depicted in Fig. 8.1c. Conduction of one of the devices may give rise to a positive feedback path, ending in a stable state. Latch-up is a phenomenon common in CMOS processes since two parasitic bipolar transistors (and therefore an SCR structure) exist between the substrate, the well, and the sources of the NMOS and PMOS transistors. Consider the parasitic circuit shown in Fig. 8.1c. If a minimum voltage of 0.7 volts biases $R_{substrate}$ either directly

due to the substrate noise or as a consequence of the substrate noise such as ground bounce, the NPN transistor will turn on. The collector current of the NPN transistor biases the resistor R_{well}. When V_{BE} across the PNP transistor reaches a minimum of 0.7 volts, the PNP transistor turns on. A PNP collector current is generated, biasing the resistor $R_{substrate}$. The voltage V_{BE} across the NPN transistor increases, reaching the trigger point ($V_{BE-NPN} = 0.7$ volts). As shown in Fig. 8.1d, at this point the emitter voltage V_{ne} "snaps back" and reaches a stable state characterized by a holding voltage of approximately 4 volts (originating from the Zener voltage across the $N+$ to $P+$ junction at the emitter of the NPN transistor, see Fig. 8.1b). This stable state persists as long as the voltage across the two transistors is greater than the holding voltage. At this point, the noise source that triggered the parasitic latch-up behavior may disappear. Since the NPN emitter is also the source of the NMOS transistor, the voltage across the NMOS-PMOS structure (an inverter in this case) is only 1 volt (if $V_{DD} = 5$ volts). If the circuit is not destroyed by effects such as electromigration due to the large currents (see Fig. 8.1d), the circuit will stop operating. To disable the positive feedback latch-up loop, the voltage across the parasitic structure must be reduced below the holding voltage, which can be accomplished by turning off the power supply.

Note that even if the substrate noise amplitude is sufficiently large to trigger latch-up, the substrate noise must also be of sufficient duration in order for the positive loop to stabilize and lock. Therefore, if V_{nl} is the substrate noise amplitude and T_{nl} is the duration of the noise pulse, a relationship between V_{nl} and T_{nl} exists in order for the latch-up to lock. Qualitatively, a large V_{nl} requires a small T_{nl}, while a small V_{nl} requires a large T_{nl} (see Fig. 8.2).

The parasitic structure is actually more complex than the structure shown in Fig. 8.1c. A schematic of a more complicated parasitic circuit is depicted in Fig. 8.3, where two additional bipolar transistors corresponding to the drains of the NMOS and PMOS transistors are shown. The process cross-section is shown in Fig. 8.3a, while a schematic of the resulting parasitic circuit is depicted in Fig. 8.3b. Note the two additional transistors, Q3 and Q4. The emitters of Q3 and Q4 are connected to the output terminal of the inverter, *Out*.

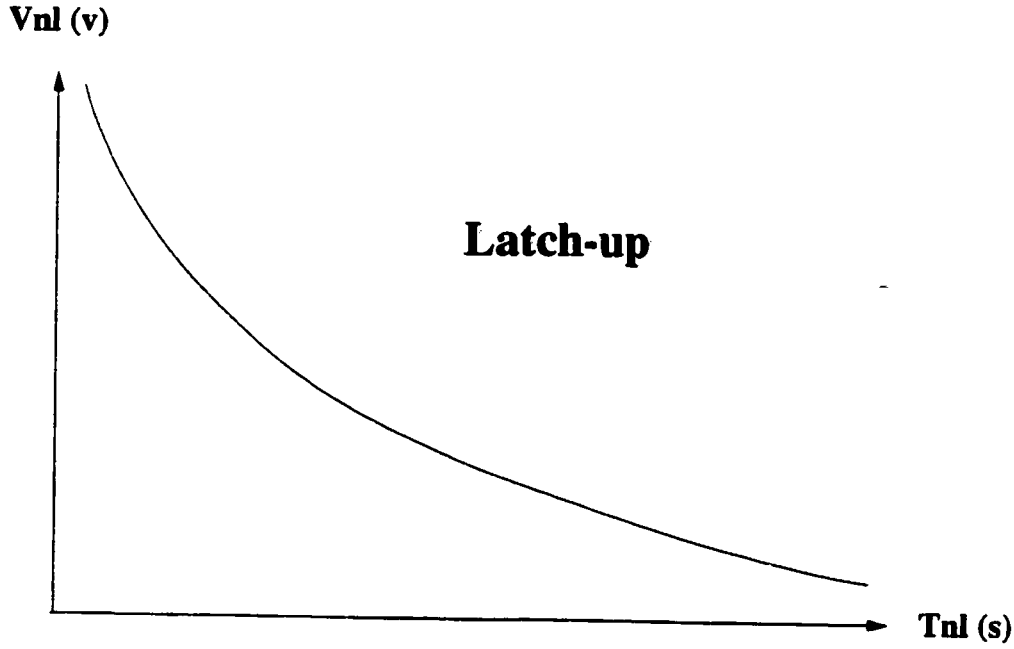


Figure 8.2: Latch-up occurance depending on the $V_{nl} - T_{nl}$ relationship

In relation to the substrate noise, Q3 and Q4 may induce latch-up due to a parasitic transition at the output of a logic element. This situation may be created by the following two situations:

- The substrate bias and the output parasitic transition are such that V_{BE} across Q4 reaches a minimum 0.7 volts. Q4 is turned on and a current is generated at the collector of the Q4 transistor, biasing R_{well}. The loop

closes in a way similar to that shown in Fig. 8.1. This situation may occur, for example, for an undershoot of the output (0.7 volts below the ground potential when the substrate is at the ground potential), or for any situation where the output of the circuit is at a potential lower than 0.7 volts with respect to the substrate. Examples of such situations are: 1) the circuit drives a small capacitive load producing fast output transitions and therefore undershoots and ringing, and 2) multiple noise spikes within the substrate are present such that the output, driving a large capacitive load, does not have sufficient time to resolve to a steady state in between the noise spikes.

- The well bias and the output parasitic transition are such that V_{BE} across Q3 reaches a minimum of -0.7 volts. Q3 is turned on and a current is generated in the collector of the Q3 transistor that biases $R_{substrate}$. The loop is closed in a way similar to that illustrated in Fig. 8.1. This situation may occur, for example, for an overshoot at the output (0.7 volts above the V_{DD} potential when the well is at a potential of V_{DD}), or for any situation where the output is at a higher potential than the well. Examples of such situations are: 1) the output drives a large capacitive load, producing slow output transitions and therefore the noise signal in the well oscillates quickly with respect to the output node, and 2) multiple noise spikes within the substrate are present such that the output (that drives a small capacitive load) does not have sufficient time to resolve to a steady state in between the noise spikes.

For example, multiple noise spikes (high noise nonuniformity within the substrate) occur when multiple noise sources are present (such as in the application described in Chapter 3). Note the importance of the amplitude, duration, and speed of the output parasitic transitions induced by the substrate noise at the

output of a logic element (see Chapter 5), and the relationship among these characteristics and the substrate and well bias with respect to triggering latch-up and closing the parasitic loop. Note that a solution for avoiding latch-up induced by the parasitic output transitions is using low-swing logic families.

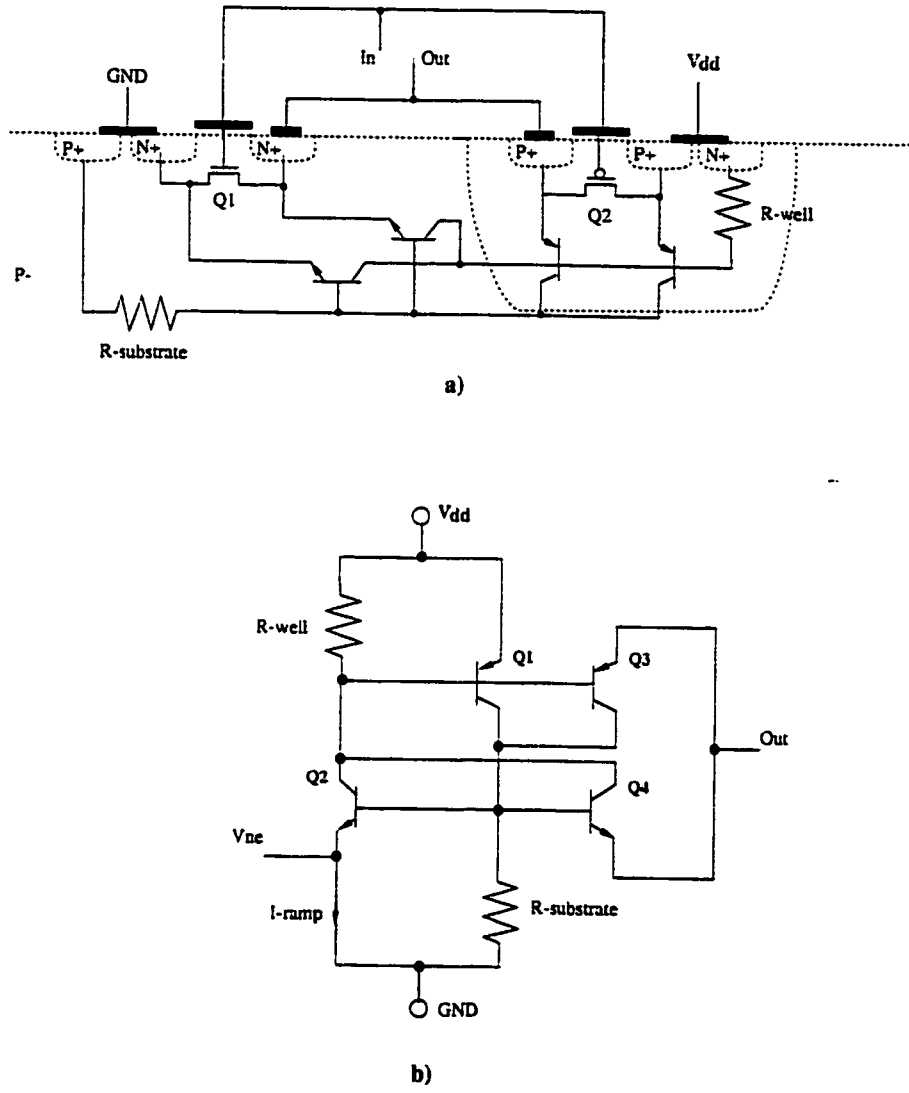


Figure 8.3: Further insight into the latch-up phenomenon: a) Process cross-section of a CMOS inverter and b) A schematic of the SCR parasitic circuit.

8.1.2 Mathematical conditions for the occurance of latch-up

As described in Section 8.1.1, for latch-up to occur, the parasitic PNPN circuit must be triggered and the holding state must be maintained. One of the situations where latch-up is triggered is when one of the two NPN transistors are turned on and a sufficient current $I_{npn-trigger}$ in the collector is generated to bias R_{well} and turn on the PNP transistor (see Figs. 8.1c and 8.3b). The mathematical form for this condition is [102]

$$I_{npn-trigger} = \frac{V_{pnp-on}}{\alpha_{npn} R_{well}}, \tag{8.1}$$

where V_{pnp-on} of approximately 0.7 volts is the turn-on voltage of the PNP transistor, α_{npn} is the common base gain of the NPN transistor, and R_{well} is the well resistance. Note that to minimize the probability of triggering latch-up, a large $I_{npn-trigger}$ is desired, which is equivalent to the existence of a high amplitude substrate noise. Multiple solutions exist to reduce the amplitude of the substrate noise such as the proper placement of the substrate contacts (see Chapter 7). Accordingly, if a large $I_{npn-trigger}$ is required to trigger latch-up, it may not be possible to reach the required noise amplitude to generate the necessary $I_{npn-trigger}$. Note from (8.1) that $I_{npn-trigger}$ can be increased by reducing α_{npn} and R_{well}. A small α_{npn} is equivalent to a small β_{npn} according to the general equation,

$$\beta = \frac{\alpha}{1-\alpha}. \tag{8.2}$$

An analysis of the circuit depicted in Fig. 8.1c produces the following inequality for latch-up to occur,

$$\beta_{npn}\beta_{pnp} \geq 1 + \frac{(\beta_{npn}+1)(I_{Rsubstrate} + I_{Rwell}\beta_{pnp})}{I_{DD} - I_{Rsubstrate}}, \tag{8.3}$$

where

$$I_{Rsubstrate} = \frac{V_{BE-npn}}{R_{well}}, \tag{8.4}$$

$$I_{Rwell} = \frac{V_{BE-pnp}}{R_{substrate}}, \tag{8.5}$$

and I_{DD} is the total supply current. Again, note that by reducing R_{well}, $R_{substrate}$, and the gain of the parasitic transistors, β_{npn} and β_{pnp}, the probability for satisfying (8.3) is greatly reduced.

A common criterion for latch-up is that the sum of the common base current gain of the NPN and PNP transistors must equal or exceed unity [64, 100, 103],

$$\alpha_{npn} + \alpha_{pnp} \geq 1. \tag{8.6}$$

This expression is equivalent to (8.3).

As demonstrated above, the characteristics of the bipolar transistors and the values of the R_{well} and $R_{substrate}$ are decisive in determining whether latch-up is triggered. A low β of the bipolar transistors as well as low values of the two resistors are desirable to prevent the likelihood of latch-up. Due to the higher mobility of the electrons as compared to the mobility of holes, an NPN transistor is characterized by a larger β than a PNP transistor for the same geometrical configuration. In the parasitic structures illustrated in Figs. 8.1b and 8.3a, note that the NPN transistors are lateral transistors while the PNP transistors are vertical transistors. As compared to a vertical transistor, the base width of a lateral transistor is significantly more difficult to control and therefore larger. As a consequence, β for a lateral transistor is typically smaller than β for a vertical transistor. Note also that the base width of the NPN transistors is the distance

between the drain of the NMOS transistor and the N-well (see Fig. 8.3a), while the base width of the PNP transistors is the distance between the depth of any of the $P+$ diffusions and the N-well edge. Accordingly, the base width of the PNP transistor is much smaller than the base width of the NPN transistor. Note also that while the PNP base width is technologically dependent, the NPN base can be adjusted by simple physical design techniques. For 1.2 μm minimum design rules, typical values for β_{npn}, β_{pnp}, R_{well}, and $R_{substrate}$ are, depending on the substrate doping and other technological factors, 2 to 5, 10 to 100, 10 to 20 kΩ, and 2 to 5 kΩ, respectively. A large spread of these parasitic elements is noted and is highly dependent on the physical design implementation.

8.1.3 Analysis of substrate noise induced latch-up for different technologies

Since different technologies are characterized by different values of β and R, the conditions to trigger latch-up differ from one technology to another technology. For substrate coupling induced latch-up, as shown in Section 8.1.1, the triggering conditions are determined by the noise amplitude V_{nl} and noise duration T_{nl}. The sensitivity to latch-up of different technologies has been described in the literature [104–106] based on both device and circuit simulation. With circuit simulation, the parasitic structure shown in Fig. 8.1c is used, and worst case model parameters for the bipolar transistors and resistors are employed. Published results for several technologies are listed in Table 8.1, where the foot-

notes[6,7,8,9,10,11,12,13,14,15] describe the different simulation conditions, simulators, and assumptions used to produce these results.

Table 8.1: Worst case conditions for substrate noise induced latch-up in different technologies

Technology	Noise amplitude V_{nl} (V)	Noise duration T_{nl} (ns)
0.5 μm P-well[6,7]	2	12.5
1.2 μm N-well[8,9]	2	4.5
	1.5	6
	1	9
	0.75	19
1.5 μm[10,11] twin-tub[12,13]	2.5	0.7
2 μm N-well[14,15]	0.76	2.8

Note the variety of technologies, ranging from a feature size of 0.5 μm to 2 μm for N-well, P-well, or twin-well CMOS process technologies. For the 1.2 μm technology, note that, as expected (see Section 8.1.1), T_{nl} increases as V_{nl} decreases. Note the 2 μm and 1.2 μm N-well technologies for a V_{nl} of 0.75 volts; as the technology feature size decreases (at a ratio of $\approx$ 1.67:1), T_{nl} increases at a ratio of $\approx$ 6.8:1. Using this ratio, the latch-up triggering conditions for any technology can be obtained. However, the extrapolated results greatly depend on the accuracy of the results listed in Table 8.1, specifically on the accuracy of the 2 μm and 1.2 μm technologies. These extrapolated results are useful as a first order estimate for analyzing the substrate level characteristics that may induce latch-up in different technologies. Some extrapolated results are listed in Table 8.2.

[6] Custom simulation tool [106]
[7] 3 volt power supply
[8] SPICE circuit simulations of the structure shown in Fig. 8.1c
[9] 5 volt power supply
[10] Not specified in [104]
[11] Author's estimation from the drawings provided in [104] based on typical layout rules
[12] 5 volt power supply
[13] Medici [74] simulations
[14] 5 volt power supply
[15] Custom simulation tool [105]

Table 8.2: Theoretical extrapolation of the latch-up triggering conditions based on the experimental results listed in Table 8.1

Technology	Noise amplitude V_{nl} (V)	Noise duration T_{nl} (ns)
2.5 μm N-well	2.0	0.13
	1.5	0.18
	1.0	0.26
	0.75	0.56
2 μm N-well	2.0	0.66
	1.5	0.88
	1.0	1.3
	0.75	2.8
1.2 μm N-well	2.0	4.5
	1.5	6
	1.0	9
	0.75	19
0.5 μm N-well	2.0	43.9
	1.5	58.5
	1.0	87.8
	0.75	185
0.18 μm N-well	2.0	122
	1.5	162
	1.0	244
	0.75	513

The trends quantified in Table 8.2, namely that T_{nl} increases as the technology feature size decreases, can be attributed to certain device issues such as the increased internal electric fields in scaled technologies. As the technology is scaled, the distance between adjacent junctions decreases and the density of the junctions increases. The electrons injected into the substrate by a noisy drain are attracted by the high density of the space-charge regions, the recombination rate of the charge carriers increasing as the technology feature size decreases. Accordingly, in scaled technologies, a larger time is necessary for the charge carriers to concentrate and efficiently bias and turn-on the parasitic bipolar transistors, triggering latch-up. The increased sensitivity to substrate noise induced latch-up

in the P-well and twin-well technologies as compared to an N-well technology (see Tables 8.1 and 8.2) can be attributed to the lower mobility of holes as compared to electrons. Accordingly, less carriers are attracted by the space-charge regions as compared to an N-well technology, making the recombination rate lower. As a consequence, as compared to an N-well technology, more carriers are available to efficiently bias and turn-on the parasitic bipolar transistors; therefore, the noise duration T_{nl} necessary to trigger latch-up is smaller.

Furthermore, as a technology is scaled, the base thickness of both the NPN and PNP transistors decreases, increasing β. However, at the same time, both R_{well} and $R_{substrate}$ decrease since the doping concentrations increase and the distances responsible for the two resistance values decrease (see Fig. 8.3a). To a first order approximation, the two effects cancel since the larger collector current generated by the two transistors (due to a larger gain) produce a similar voltage drop across the smaller resistors. The voltage drop, however, increases substantially if the density of the substrate contacts is low, since the distances responsible for the parasitic resistors have increased (see Fig. 8.1b).

Concluding, a scaled technology with poorly placed substrate contacts (see Chapter 7) may be more sensitive to substrate noise induced latch-up because of the increased β of the parasitic transistors and the increased parasitic resistances due to the poor placement of the substrate contacts. At the same time, a scaled technology featuring an enhanced substrate contact placement is less prone to substrate noise induced latch-up. The sensitivity of a scaled technology to substrate noise induced latch-up improves as illustrated by the trends listed in Tables 8.1 and 8.2. As the feature size of a technology decreases, a substrate noise pulse of similar amplitude must have a larger duration to efficiently induce latch-up.

Experimental results characterizing the sensitivity to noise induced latch-up of epi and non-epi technologies are described by Troutman in [27]. Aspects such as the sensitivity to: 1) the R_{well} and $R_{substrate}$, 2) a negative bias of the substrate, 3) a backside substrate contact, and 4) the position and layout of the source terminals of the transistors with respect to the substrate contacts have been experimentally investigated.

A conclusion consistent with VLSI deep submicrometer technologies can be developed from [27] to improve the sensitivity to substrate noise induced latch-up. Specifically, an epi technology should be used with a backside substrate contact. The source terminal of the PMOS transistor should be partially surrounded by a well substrate contact. These recommendations are in addition to the aforementioned conclusions regarding the sensitivity to substrate noise induced latch-up in scaled technologies.

8.1.4 Measures to prevent triggering latch-up

The analysis described in Sections 8.1.1, 8.1.2, and 8.1.3 suggests several solutions to minimize the sensitivity to substrate noise induced latch-up. These solutions can be divided into technological, physical, and circuit design related approaches. Briefly, most of these solutions either reduce the parasitic β or R (see Fig. 8.1c) or both. A summary of these solutions are presented next.

- **Technological solutions**
  - Scaled technologies are beneficial (see Section 8.1.3).
  - Epitaxial technologies are beneficial (see Section 8.1.3). Thin epitaxial layers further decrease the sensitivity of a circuit to latch-up.

- Use a retrograde well technique [107] to reduce R_{well} while preserving the performance of the transistors.
- Older technological techniques to reduce the β of the parasitic transistors utilize gold doping or neutron irradiation [108, 109]. Another technique utilizes Schottky source/drains on the PMOS transistors to degrade the emitter injection efficiency [110, 111]. A highly doped bulk with a thin epitaxial layer has also been shown to be efficient in shunting the lateral parasitic bipolar transistors [103, 112].

- **Physical design solutions**
  - From Fig. 8.1b, note that either $R_{substrate}$ or R_{well} is composed of two paths; 1) from the base terminal of the bipolar transistor to the substrate (well) contact, and 2) from the substrate (well) contact to the emitter terminal. The second element, which may be particularly large, can be minimized by shorting the resistor with a low resistivity metal connection between the substrate contact and the emitter terminal routed through the shortest physically allowable path.
  - Connect substrate (well) contacts to the power supply lines with metal (*i.e.*, do not use diffusion or polysilicon).
  - The previous two techniques also prevent both of the two diodes (source-to-substrate, see Fig. 8.1b) from becoming forward-biased.
  - Place substrate contacts as close as possible to the source terminals of the MOS transistors. Ideally, place one substrate contact near each transistor connected to any of the power supply lines.

- Maintain a symmetric and conservative layout. For every row, the PMOS transistors should be placed in the upper side and the NMOS transistors should be placed in the lower side. Avoid physical design styles in which the NMOS and PMOS devices are interwined in a checkerboard style.
- Use $N+$ and $P+$ guard rings connected to the V_{DD} and GND power supply lines, respectively, surrounding the PMOS and NMOS transistors to reduce the gain (β) of the parasitic bipolar transistors.
- Source diffusion regions of the NMOS transistors should be placed so that these regions lie along equipotential lines generated by the current flow. Alternatively, the source terminals should be perpendicular to the primary direction of the current flow. This technique reduces the possibility of latch-up due to an effect called *field aiding* [101].
- Always use highly doped and wide $N+$ and $P+$ substrate contacts placed as close as possible to the source terminals of the MOS transistors to reduce the parasitic resistances.
- Correctly placing the substrate contacts in a scaled technology (see Section 8.1.3) greatly improves the immunity of the circuit to latch-up induced by substrate noise.
- Use a backside substrate contact for epi technologies (see Section 8.1.3).
- Preferably, the source terminal of the PMOS transistor should partially surround the substrate contact [27].

- **Circuit design solutions**

  - Avoid fast transition signals driving the primary noise generation circuitry. These fast transition signals may generate large substrate noise, producing a large V_{nl} (see Sections 8.1.2 and 8.1.3, as well as Fig. 2.15).
  - In case of multiple noise sources, avoid excessive skewing of the signals that turn on these noise sources. While the skewing is beneficial since the skew reduces the amplitude of the maximum instantaneous noise (the V_{nl}), excessive skewing increases the duration of the noise pulse, T_{nl} (see Section 8.1.3). Therefore, a tradeoff exists between the number of noise sources that should be turned on at any one time and the maximum skew. This tradeoff depends upon the relationship between V_{nl} and T_{nl} for a target technology (see Section 8.1.3). Accordingly, if a circuit analysis of the noise generation process and the V_{nl}–T_{nl} relationships demonstrate a critical impact on the latch-up immunity of the circuit, a strategy for driving the circuits that generate noise (the noise sources) may be delicate, requiring a careful design effort in order to avoid latch-up.
  - Particularly for non-epi technologies, bias the backside substrate contact with a negative voltage (see Section 8.1.3).

8.2 The noise behavior of CMOS logic primitives

It is assumed in this section that the necessary precautions have been taken to ensure that latch-up is eliminated. Under this assumption, circuit simulations using the Cadence-Spectre simulator for a 2.5 μm CMOS technology are presented here to describe the conditions in which a parasitic transition is induced by substrate noise at the output of a CMOS inverter and latch. A similar analysis has been performed for an NMOS inverter and latch in Chapter 5. The analysis considers the worst case situation in which a substrate noise of a given amplitude forces the substrate to float synchronously, in phase, and with the same amplitude as the substrate noise. The sensitive circuits do not float with the substrate noise. These conditions are equivalent to the situation where the substrate noise variations are not induced into the power supply lines, a practical situation when the substrate contacts are at a sufficient distance from the sensitive circuitry and/or when no low resistivity path exists between the substrate contacts and the ground of the logic sensitive circuitry. As the distance between the sensitive circuitry and the substrate contacts decreases and/or a low resistivity path is created between the substrate contacts and the ground of the logic sensitive circuitry, the substrate noise variations are increasingly induced into the power supply lines. As a consequence, the sensitive circuits float increasingly synchronously with the substrate with the same magnitude and direction as the substrate noise. This synchronous variation minimizes the deleterious effects of substrate noise, particularly when the digital circuit elements are physically close on-chip. If the on-chip distance between operationally connected digital circuit elements is large, such as is the

case for a buffer driving a circuit through a long interconnect line, the substrate noise may affect the circuit (which will float synchronous with the noise) and may not affect the buffer. If the output of the buffer is at logic high and the circuit floats with a positive substrate noise, the logic high level at the buffer output may be seen as a logic low signal by the circuit. Therefore, a parasitic transition at the output of the circuit may be induced. This behavior directly affects the repeater insertion methodology. As noise becomes an increasingly important issue, large digital buffers driving long interconnect lines are not recommended. The use of a large number of distributed repeaters is preferable, even if the speed of the circuit is degraded. The number of repeaters depends upon the characteristics of the substrate noise (such as the amplitude and any non-uniformity), and should be chosen such that the overall effect of the estimated noise amplitude and non-uniformities as well as the presence of other noise mechanisms is below a threshold such that the likelihood of inducing a parasitic transition is minimized. Another related aspect is if the ground line floats synchronously with the substrate noise but the V_{DD} line does not. In this case, the operation of the circuit is affected by a power supply variation induced by the substrate noise. To minimize this parasitic power supply variation, an efficient capacitive filter should be used to control the voltage fluctuations within the power supply lines.

Note the importance of analyzing the noise behavior of the principal logic elements under worst case conditions. The noise immunity can be enhanced as compared to the results obtained in these worst case conditions through methods such as 1) properly placing the substrate contacts, 2) using a low resistivity interconnect path between the substrate contacts and the ground lines of the sensitive circuitry, 3) using a compact layout, and 4) decoupling the power supply.

In this section, an analysis of a CMOS inverter and latch is performed. The worst case conditions of this analyses are summarized as follows:

- No low resistivity path exists between the substrate contacts for the epi layer (N-well) and GND (V_{DD}).
- The substrate contacts for the epi layer and N-well do not reduce the substrate noise at the sensitive circuits.
- The epi layer and the N-well are biased at zero and five volts, respectively, under equilibrium conditions.
- The substrate noise variations are added to the equilibrium bias values of the epi layer and N-well.

Design recommendations for repeater insertion in a noisy environment are also provided.

8.2.1 Noise analysis of a CMOS inverter

A CMOS inverter as well as the noise analysis set-up are shown in Fig. 8.4. Similar to the NMOS inverter analysis, V1 and V2 are the noise signals for Q1 and Q2, respectively. V1 simulates the noise into the epi layer and V2 simulates the noise into the N-well. Substrate voltage transients vary from +5 to -5 volts. The size of Q1 is $4\,\mu m/4\,\mu m$, and the size of Q2 is $8\,\mu m/3\,\mu m$. Results of the static analysis are presented in Table 8.3 and are discussed below.

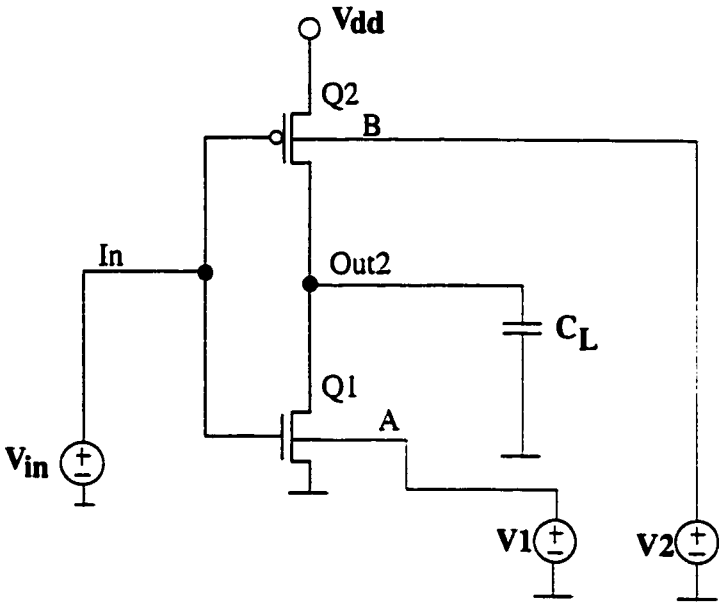


Figure 8.4: Circuit used to investigate the noise behavior of a CMOS inverter

Situations 1 to 11 correspond to the case where the noise is in the epi layer and affects the NMOS transistors but is not present in the N-well, and therefore does not affect the PMOS transistors. This situation may occur for certain substrate contact placements, during transient noise conditions, or because of a less optimal physical design (the circuit placement should be along equipotential noise lines).

Table 8.3: Inverter output response as a function of substrate bias

No.	In	V1 (V)	V2 (V)	V_{out} (V)	V_{TNN} (V)	V_{TPN} (V)
1.	High (Low)	5	5	4.58 (5)	0.71(0.7)	-0.93 (-0.93)
2.	High (Low)	4	5	3.46 (5)	0.71 (0.7)	-0.9 (-0.94)
3.	High (Low)	3	5	2.44 (5)	0.71 (0.7)	-0.88 (-0.94)
4.	High (Low)	2	5	1.44 (5)	0.72 (0.71)	-0.86 (-0.94)
5.	High (Low)	1	5	0.44 (5)	0.73 (0.71)	-0.84 (-0.94)
6.	High (Low)	0	5	0 (5)	1 (1)	-0.83 (-0.94)
7.	High (Low)	-1	5	0 (5)	1.5 (1.5)	-0.83 (-0.94)
8.	High (Low)	-2	5	0 (5)	1.89 (1.88)	-0.83 (-0.94)
9.	High (Low)	-3	5	0 (5)	2.2 (2.19)	-0.83 (-0.94)
10.	High (Low)	-4	5	0 (5)	2.47 (2.46)	-0.83 (-0.94)
11.	High (Low)	-5	5	0 (5)	2.71 (2.7)	-0.83 (-0.94)
12.	High (Low)	5	10	4.59 (5)	0.71 (0.7)	-2 (-2)
13.	High (Low)	4	9	3.46 (5)	0.71 (0.7)	-1.9 (-1.9)
14.	High (Low)	3	8	2.44 (5)	0.71 (0.7)	-1.63 (-1.68)
15.	High (Low)	2	7	1.44 (5)	0.71 (0.71)	-1.41 (-1.49)
16.	High (Low)	1	6	0.44 (5)	0.73 (0.71)	-1.16 (-1.28)
17.	High (Low)	-1	4	0 (4.68)	1.52 (1.51)	-0.62 (-0.72)
18.	High (Low)	-2	3	0 (3.69)	1.89 (1.88)	-0.63 (-0.71)
19.	High (Low)	-3	2	0 (2.68)	2.19 (2.11)	-0.65 (-0.71)
20.	High (Low)	-4	1	0 (1.67)	2.47 (2.46)	-0.67 (-0.7)
21.	High (Low)	-5	0	0 (0.6)	2.71 (2.71)	-0.69 (-0.7)

The reverse situation, when the noise is present in the N-well and is not present in the epi layer, occurs under similar conditions and is described by cases 1 to 10 listed in Table 8.4. A positive (negative) noise spike is induced in the N-well for situations 1 to 5 (6 to 10). However, this reverse situation occurs with a lower probability since: 1) an N-well is a local diffusion of limited area, and each well hosts a small group of PMOS transistors, 2) typically, the power devices that generate large amounts of noise are NMOS devices, and 3) if a complementary pair of power devices is used, the power PMOS transistor is realized in an individual N-well which is not shared with other sensitive transistors.

Table 8.4: Inverter output response as a function of substrate bias

No.	In	V1 (V)	V2 (V)	V_{out} (V)	V_{TNN} (V)	V_{TPN} (V)
1.	High (Low)	0	10	0 (5)	1.02 (1.01)	-1.89 (-2)
2.	High (Low)	0	9	0 (5)	1.02 (1.01)	-1.74 (-1.85)
3.	High (Low)	0	8	0 (5)	1.02 (1.01)	-1.57 (-1.68)
4.	High (Low)	0	7	0 (5)	1.02 (1.01)	-1.38 (-1.49)
5.	High (Low)	0	6	0 (5)	1.02 (1.01)	-1.15 (-1.26)
6.	High (Low)	0	4	0 (4.68)	1.02 (1.01)	-0.72 (-0.94)
7.	High (Low)	0	3	0 (3.68)	1.02 (1.01)	-0.63 (-0.71)
8.	High (Low)	0	2	0 (2.68)	1.02 (1.01)	-0.65 (-0.71)
9.	High (Low)	0	1	0 (1.67)	1.02 (1.01)	-0.67 (-0.7)
10.	High (Low)	0	0	0 (0.6)	1.02 (1.02)	-0.69 (-0.7)
11.	High (Low)	3	6	2.44 (5)	0.71 (0.7)	-1.2 (-1.26)
12.	High (Low)	5	7	4.58 (5)	0.71 (0.7)	-1.48 (-1.49)
13.	High (Low)	-3	4	0 (4.68)	2.2 (2.19)	-0.62 (-0.72)
14.	High (Low)	-5	3	0 (3.69)	2.71 (2.7)	-0.63 (-0.71)
15.	High (Low)	2	7	1.44 (5)	0.71 (0.71)	-1.41 (-1.49)
16.	High (Low)	3	10	2.44 (5)	0.71 (0.7)	-1.95 (-2)
17.	High (Low)	1	8	0.44 (5)	0.73 (0.71)	-1.58 (-1.68)
18.	High (Low)	-2	8	0 (5)	1.89 (1.88)	-1.57 (-1.68)
19.	High (Low)	-5	8	0 (5)	2.71 (2.7)	-1.57 (-1.68)

Situations 11 to 19 listed in Table 8.4 describe intermediate transient noise configurations. Situations 11 to 14 (15 to 19) describe a fast rising (falling) noise transient into the epi layer that is induced (with a delay) into the N-well.

Note from the data listed in these two tables the situations for which a significant parasitic transition is induced when the input is either a logic high or logic low. When the input is logic high, significant parasitic transitions are induced for situations 1, 2, 3, 4, 12, 13, 14, and 15 listed in Table 8.3 and situations 11, 12, 15, and 16 listed in Table 8.4. When the input is logic low, significant parasitic transitions are induced for the situations 18, 19, 20, and 21 listed in Table 8.3, and situations 7, 8, 9, 10, and 14 listed in Table 8.4.

When the input is logic high, a parasitic output transition is produced when a positive noise transient is present in the epi layer independent of the noise in the N-well, which can be either zero or positive. When the input is logic low, a parasitic output transition is produced when a negative noise transient is present in the N-well, independent of the noise in the epi layer, which can be either zero or negative.

Note that, as compared to the NMOS logic elements, output parasitic transitions occur equally for both positive and negative noise spikes and for both input high and input low signals. Note, however, that a parasitic transition can be induced by a positive noise spike only when the input is logic high, and can be induced by a negative noise spike only when the input is logic low. The phenomenon responsible for this behavior is the forward biasing of the epi-source junction of the NMOS transistor for positive noise transients and the N-well-source junction of the PMOS transistor for negative noise transients. To exemplify this phenomenon, situation No. 1 listed in Table 8.3 is discussed below. The other situations are similar.

- Note that for this situation, the output is 4.6 V. The epi layer (biased at 5 volts), strongly forward biases the substrate-to-source junction, generating a current of $\approx$ 22.5 mA from the substrate to the source. The substrate-to-drain junction may be similarly forward biased. However, the current that is generated if the substrate-to-drain junction is forward biased can only discharge the capacitive output load. Therefore, since a continuous current path cannot be created, the substrate-to-drain junction cannot be forward biased. The equilibrium drain (the output) potential is such that due to the resulting bias of the substrate-to-drain junction, the current generated by this junction compensates for the leakage current of the output capacitance.

The noise immunity of the CMOS logic circuits appears to be worst than the noise immunity of the NMOS logic circuits since a parasitic output transition can be induced equally for both positive and negative noise transients and for both input high and low signals. However, note that a significant parasitic transition is induced if the aforementioned junctions are forward biased with more than 2 volts. For the epi-source junction of an NMOS transistor (as depicted in Fig. 8.5), this forward-bias voltage may be generated due to the following parasitic elements: 1) RC_m and L_m caused by the currents flowing through the ground line, 2) RC_{sb1} and L_{sb1} caused by the currents flowing through the epi layer between the P+ substrate contact and the source diffusion, and/or 3) RC_{sb2} and L_{sb2} caused by the currents flowing through the epi layer between the source diffusion edge closest to the drain (to the transistor channel) and the source diffusion edge closest to the substrate contact. All of these parasitic elements are minimized if the substrate contacts are placed as close as possible to the source diffusion, minimizing the forward bias voltages of the epi-source junction.

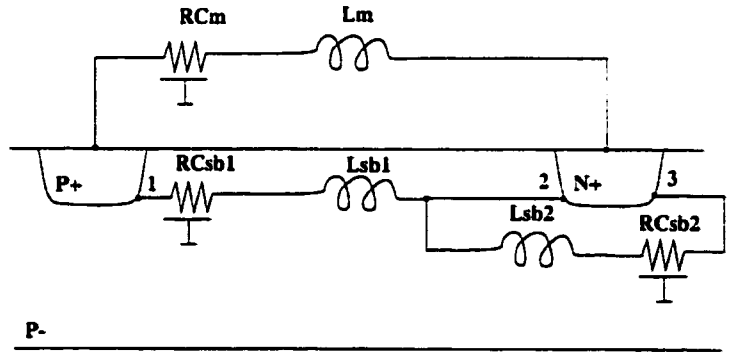


Figure 8.5: The parasitic elements that forward bias the epi-source junction

An effect similar to latch-up can be induced by the parasitic elements of the epi layer corresponding to $Sb1$ and $Sb2$, and is described next. Consider, for example, that the substrate noise is $\approx$ 0.7 volts such that the epi-source junction is

marginally biased and a small current is injected into the epi layer. This current further forward biases the epi-source junction through the $Sb1$ and $Sb2$ parasitic elements, creating a positive feedback loop between the substrate and the source diffusion by further increasing the forward bias of the epi-source junction. Therefore, the current injected into the epi layer by the forward biased junction increases, creating a larger forward bias. Note that the initial substrate noise of ≈ 0.7 volts may surpass the 2 volt threshold due to this positive feedback loop through an avalanche effect. The condition for this avalanche effect being triggered is that the initial substrate noise spike needs to be of sufficient duration to permit the positive feedback loop to increase the forward bias voltage to the 2 volt threshold. Note, however, that the avalanche effect may still be triggered even if the initial substrate noise spike is not of sufficient duration. That is, if the forward bias voltage reaches, for example, a minimum of 1.4 volts when the initial 0.7 volt noise spike disappears. The junction bias will remain at ≈ 0.7 volts, thereby maintaining the positive feedback loop and increasing the forward bias voltage to 2 volts in the absence of noise.

Note the importance of the parasitic elements of $Sb1$ in triggering this effect. In the following discussion, 1, 2, and 3, depicted in Fig. 8.5, denote the contact locations. If the potential of the P+ substrate contact is at a zero reference potential, 1 represents the lowest potential of the three contacts, increasing in potential at 2 due to $Sb1$, and subsequently increasing in potential at 3 due to $Sb2$. Therefore, reducing the parasitic elements of $Sb1$ minimizes the deleterious effects of the positive feedback loop between the substrate and the source diffusion. The parasitic elements of $Sb2$ cannot be minimized for a target technology because the minimum diffusion width (as noted between contacts 2 and 3) is technologically

imposed. Therefore, the most vulnerable contact of the epi-source junction that can be forward biased is contact 3. The parasitic elements of $Sb2$ may, however, be minimized by placing a substrate contact such that the contact partially surrounds the source. Such a substrate contact placement has been experimentally observed by Troutman to improve latch-up immunity (see Section 8.1); therefore, these theoretical explanations support the experimental observations.

If the distance between 1 and 2 (the substrate contact and the source diffusion, see Fig. 8.5) is comparable to or larger than twice the epi thickness, the current injected by the epi-source junction propagates between the source and the substrate contact through the low resistivity bulk. This situation is equivalent to the worst case conditions defined at the beginning of this section.

To minimize the effects generated by forward biasing the epi-source junction, thereby improving the noise immunity of CMOS digital circuits, the following rules are recommended:

- In a noisy environment, each transistor should have a substrate contact in the immediate vicinity of the source diffusion. This strategy requires the expenditure of significant area. Depending upon the estimated magnitude of the noise, several transistors may share a common substrate contact, thereby saving area and easing the physical design process.

- Note that routing the ground line such that the source terminal is at a reference zero potential makes the $Sb1$ parasitic elements bias the P+ substrate contact (with respect to the source diffusion) rather than biasing the source diffusion with respect to the substrate contact (see Fig. 8.5). This situation is preferable since biasing a P+ to P- (substrate contact to epi layer) junction does not create a positive feedback loop.

- Whenever the substrate contact cannot be placed in the immediate vicinity of the source diffusion, the ground line should be routed such that the source is at zero potential, namely, the current flow reaches the source diffusion first, followed by the substrate contact.

A dynamic characterization of the noise behavior of a CMOS inverter under the worst case conditions permits the following conclusions to be drawn:

- A significant parasitic transition can be dynamically induced when the input is at logic high for the situations 1, 2, 3, 4, 12, 13, 14, and 15 listed in Table 8.3, and the situations 11, 12, 15, and 16 listed in Table 8.4. A significant parasitic transition can be dynamically induced when the input is at logic low for the situations 18, 19, 20, and 21 listed in Table 8.3, and the situations 7, 8, 9, 10, and 14 listed in Table 8.4.

- A significant parasitic transition can be dynamically induced when the input is at a logic high (low) when a positive (negative) noise spike is present in the epi layer (N-well). The parasitic transition is not influenced by the noise present in the N-well (epi layer). The positive (negative) noise spike affects the NMOS (PMOS) transistor.

- The parasitic transition at the output of an inverter sharply follows the transition of the substrate noise spike that generates the output parasitic transition. This sharp output parasitic transition is independent of the capacitive load and the size of the transistors in the inverter. For a positive (negative) noise spike, the rising (falling) transition of the noise spike produces an output parasitic transition. This sharp transition at the output

can be explained by the transient forward bias conditions of the transistor junctions which occur during the signal transition of the substrate noise.

- When the noise disappears, it is desirable that the output voltage transitions quickly return to the initial state. This way, if the positive noise spike is just a glitch, the output is also only a glitch, minimizing the impact on the logic circuitry (although some power will be dissipated). While the low-to-high parasitic transition is independent of the transistor size or capacitive load, large transistor sizes and small capacitive loads are desirable in order to return the parasitic output transition to the initial state as quickly as possible following the disappearance of the noise signal.

- Note that long duration noise transients are more damaging than short duration noise transients since the output parasitic transitions occur over a longer period of time.

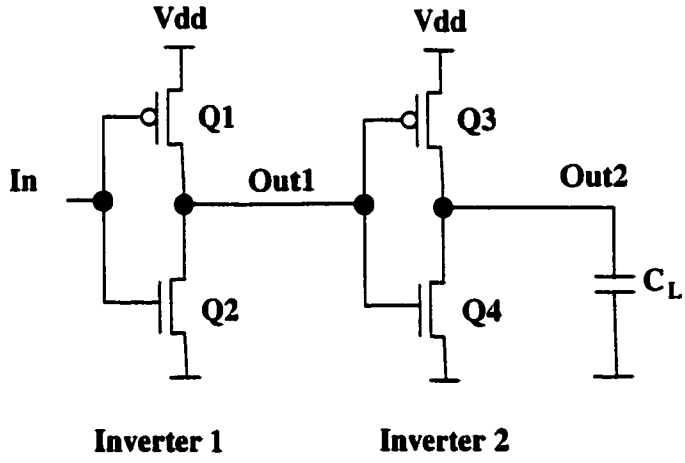


Figure 8.6: Two interconnected CMOS inverters

- Per the simulation results, a second inverter as shown in Fig. 8.6 is affected by a parasitic transition at the output of a first inverter only if this output

reaches a minimum amplitude of 3 volts (for a low-to-high output parasitic transition and a 5 volt system). This behavior is consistent with CMOS noise margins. Therefore, practically any substrate noise level below $\approx$ 3 volts amplitude is insignificant. This noise level is quite large to not induce latch-up.

- The noise behavior of the CMOS logic elements is better than the NMOS counterpart circuits. For CMOS circuits, it has been demonstrated that a noise signal can be transmitted for both input high and input low states, and for both positive and negative logic spikes. This situation is worst than for the NMOS logic elements in which a parasitic transition is shown to be induced primarily when the input is high and the substrate noise spike is positive. However, to induce a parasitic transition, the substrate noise amplitude must be significantly larger for CMOS circuits than for the NMOS circuits.

The primary conclusion of this theoretical analysis of the noise immunity of a CMOS inverter is that in order to induce a significant parasitic transition that can affect the following logic element, a large noise signal is required. If this large noise signal exists within the substrate, such as in the case of a smart-power application, it is more likely that this noise signal will induce latch-up before a parasitic transition is induced. Careful physical design, as discussed in this chapter and Chapter 7, minimizes the likelihood of both noise-induced latch-up and parasitic transitions. To minimize the effects of parasitic transitions, large transistor sizes and small capacitive loads are recommended. Careful physical design can eliminate any noise induced problems in CMOS logic circuits. Also, CMOS logic circuits are more robust to noise induced problems than NMOS circuits.

8.2.2 Noise analysis of a CMOS latch

A circuit schematic of the latch analyzed in this section is shown in Fig. 8.7. Circuit simulations using Cadence Spectre have been performed to evaluate the noise behavior of this latch. The simulation set-up is shown in Fig 8.8. Note that, similar to an NMOS latch, independent noise sources to simulate a variety of noise configurations have been provided for each of the four transistors. As with the NMOS latch, an open loop latch is analyzed. Since a transmission gate is used in the feedback loop, the output voltage is transmitted over the feedback connection without any voltage drop. The voltage across each of the four noise sources varies between +5 and -5 volts.

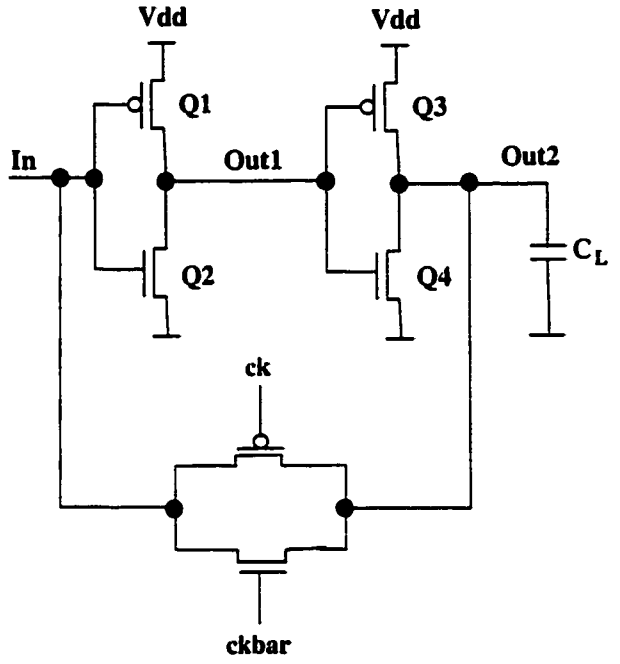


Figure 8.7: A CMOS latch

As shown for a CMOS inverter, only a positive noise pulse can induce a parasitic transition when the input is logic high, and only a negative noise pulse can induce a parasitic transition when the input is logic low. As also shown, a sig-

nificant parasitic transition is induced if the noise spike (positive or negative) is greater than 3 volts. In Table 8.5, all of the possible states of the two inverters when affected by noise are listed. The states of the two inverters with zero noise are listed in the first three columns, while the corresponding states of the two inverters in the presence of noise are listed in the final three columns.

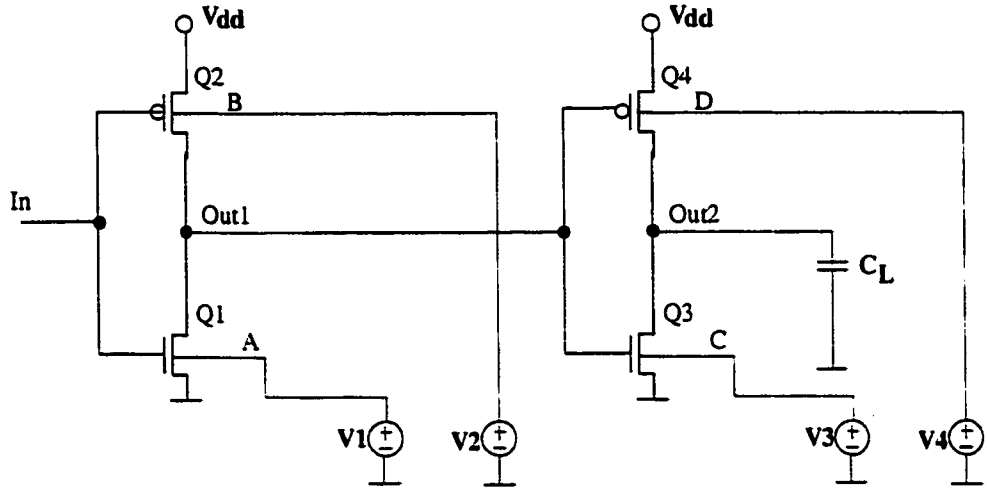


Figure 8.8: The simulation set-up

Table 8.5: Noise analysis of a latch

No.	In	Out1	Out2	In (noise)	Out1 (noise)	Out2 (noise)
1.	High	Low	High	High	High	High
2.	High	Low	High	High	High	Low
3.	High	Low	High	High	Low	High
4.	Low	High	Low	Low	High	Low
5.	Low	High	Low	Low	High	High
6.	High	Low	High	High	Low	High
7.	High	Low	High	High	Low	Low
8.	Low	High	Low	Low	High	Low
9.	Low	High	Low	Low	Low	Low
10.	Low	High	Low	Low	Low	High

Situations 1 to 5 refer to a positive noise spike while situations 6 to 10 refer to a negative noise spike. A positive noise spike greater than 3 volts affects both

inverters in situation 1, only inverter 2 in situation 2, and none of the two inverters in situations 3 and 4. The noise for inverter 1 in situation 5 is unimportant since the input is low and the substrate noise is positive. Inverter 2 in situation 5 is affected by noise. A negative noise spike greater than 3 volts affects both inverters in situation 9, only inverter 1 in situation 10, and none of the two inverters in situations 6 and 8. The noise for inverter 1 in situation 7 is unimportant since the input is high and the substrate noise is negative. Inverter 2 in situation 7 is affected by noise. Note that similar to the NMOS latch, a parasitic transition may not be latched if the noise is uniform (or "in phase"), and may be latched if the noise is nonuniform (in Table 8.5, see situation 1 as compared to situation 2, situation 4 as compared to situation 5, situation 6 as compared to situation 7, and situation 9 as compared to situation 10).

8.2.3 Repeater insertion for improved substrate noise immunity

An important observation must be noted which is equally valid for NMOS logic circuits. The noise spikes within the substrate may be either of small duration, or propagate more quickly than the delay of a logic element. For these conditions, by the time the parasitic transition induced by the noise into inverter 1 propagates to the output of inverter 1 (see Fig.8.6), the noise disappears. Depending upon the capacitive load and transistor size of the two inverters, the parasitic transition may be stored dynamically on a capacitor, transmitted to the output of inverter 2, and latched within the register. To minimize the likelihood of these situations, small capacitive loads at each output node, large transistor sizes, and a compact layout (as defined by the following analysis) are recommended.

With reference to Figs. 8.9 and 8.10, a noise spike of amplitude V_{nl} and duration T_{nl} affects inverter 1. t_D is the time required for the noise signal within the substrate to propagate across a distance D between the two inverters. As the signal propagates across the distance D, the noise spike may be attenuated and distorted; therefore, the noise affecting inverter 2 will have an amplitude V_{nl1} and a duration T_{nl1}. As shown, inverter 1 sharply responds to noise after a negligible delay t_{i1}. The noise induced parasitic signal at the output of inverter 1 has a duration of T_{pt1} with a fall time dependent on the transistor size. t_{RC} is the time required for the parasitic output transition to propagate across the interconnect between the two inverters. The noise induced parasitic signal may arrive at the input of inverter 2 distorted due to the interconnect impedance.

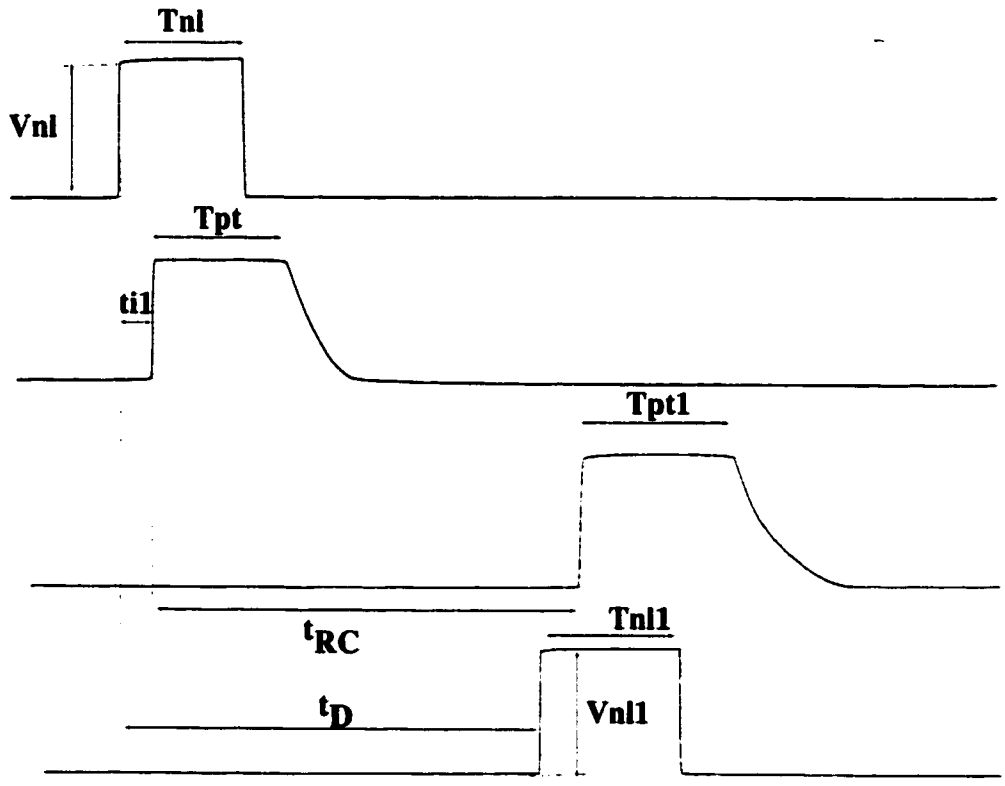


Figure 8.9: Substrate noise waveforms affecting two on-chip inverters

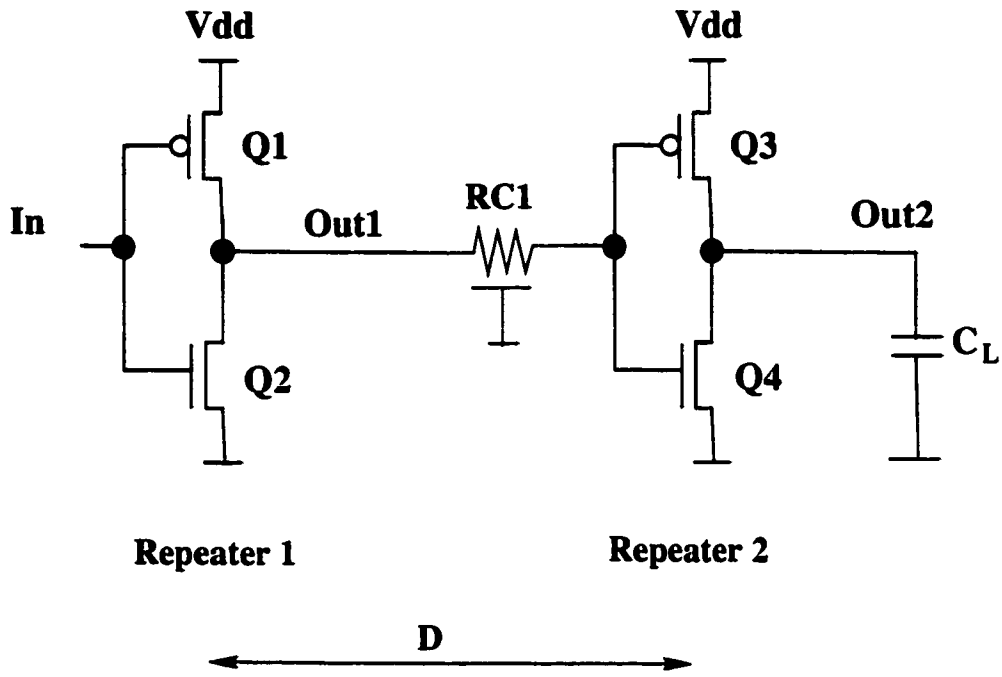


Figure 8.10: Two interconnected CMOS inverters. D is the on-chip physical distance between the two inverters

The necessary conditions so that the noise does not affect the correct circuit operation are:

$$t_D \leq t_{il} + t_{RC}, \tag{8.7}$$

$$T_{pt} \approx T_{nl}, \tag{8.8}$$

$$T_{ptl} \approx T_{nll}, \tag{8.9}$$

$$t_D + T_{nll} \leq t_{il} + t_{RC} + T_{ptl}, \tag{8.10}$$

$$t_{i1} + t_{RC} + T_{pt1} - t_D - T_{nt1} \approx 0, \tag{8.11}$$

and

$$V_{nl} \geq 3V \qquad \& \qquad V_{nl1} \geq 3V, \tag{8.12}$$

or

$$V_{nl} \leq 3V \qquad \& \qquad V_{nl1} \leq 3V. \tag{8.13}$$

These conditions are satisfied if both t_{RC} and t_D are negligible, the transistor sizes are large and the capacitive loads are small, and substrate contacts are placed to achieve high noise uniformity. Note that in order to satisfy these conditions, a maximum distance among the logic elements (inverters or repeaters) exists. The number of repeaters that should be inserted along a noisy *RC* line is much larger than if only delay is being minimized.

Concluding, similar to an NMOS latch, a CMOS latch is highly sensitive to noise nonuniformities across the substrate. Several rules have been suggested to improve the tolerance of a latch to noise. Circuit rules for transistor sizing and capacitive loading at each of the output nodes have been presented. Also, from a circuit point of view, when inserting repeaters to drive a noisy *RC* line, rules different from those used to optimize the speed and/or power [113–117] must be used. From a physical design point of view, the location for inserting repeaters and routing the interconnect lines has also been discussed. Naturally, a compact physical design style is preferable.

Chapter 9

CMOS Experimental Data

Thirty test circuits have been designed and fabricated in a 2.5 μm N-well CMOS technology. The issues chosen for investigating the CMOS circuits are similar to the issues chosen for investigating the NMOS circuits. In addition, the influence of substrate noise on latch-up, as well as the relationship between the substrate noise characteristics, latch-up, and the process of inducing a parasitic transition, have been investigated. A subset of CMOS test circuits has been fabricated to evaluate these additional effects. In this subset of test circuits, the power drivers are not isolated so that the noise generated into the substrate is larger. As for the NMOS circuits, several test chips have been fabricated to experimentally determine the principal characteristics of the noise generation process within the substrate. The experimental results derived from the measurement of the test circuits are presented in this chapter. In presenting the data, the emphasis is placed on illustrating the effects of each of the analyzed issues, on comparing the results with the expected behavior as described in Chapters 4 and 8, and on discussing possible noise mitigation techniques.

A circuit and physical design overview of the CMOS test circuits is described in Section 9.1. The experimental data is presented and discussed in Section 9.2. Fi-

nally, several conclusions regarding the substrate noise behavior of digital circuits are summarized in Section 9.3.

9.1 CMOS circuit and physical design overview

An overview of the circuit and physical design of the CMOS test circuits is presented in this section. Characteristics and tradeoffs of the circuit design process are described in Section 9.1.1. Physical design considerations are described in Section 9.1.2.

9.1.1 Characteristics of the CMOS circuit design process

The mixed-signal smart-power application that has been analyzed for the NMOS circuits and used in the Thermal Ink-Jet (TIJ) printers is also used in the CMOS analysis. A similar circuit architecture as for the NMOS circuits has been implemented for the CMOS circuits in which 5 volt digital logic independently selects one of the 48 analog power drivers. One to possibly all 48 power drivers can be selected at any one time. Each of the 48 high voltage power drivers are driven by a 13 volt predriver circuit which is placed between the 5 volt logic and the gate of the power drivers. These 13 volt predriver circuits provide the required voltage swing on the gate of the power drivers for an efficient turn-on/off process of the power drivers. As described for the NMOS circuits, for noise immunity considerations, no registers are used in the logic blocks that select the power drivers. The noise generated by the power drivers is monitored, similar to the NMOS circuits, by a chain of master-slave registers placed in the upper side of the integrated circuit. A different category of test circuits monitors the

noise generated by the power drivers by observing the actual waveforms propagating within the substrate. One of the objectives of the research presented in this section is to accurately compare the noise behavior of the NMOS circuits with the noise behavior of the CMOS circuits. To achieve this objective, the circuit implementation of the CMOS blocks and the physical design of the test circuits have been designed to be as similar as possible to the circuit implementation and physical design of the NMOS circuits.

Some of the circuit details are shown in Fig. 9.1. Note the similarity of the NMOS and CMOS circuits; the power driver, the inverters, and the static latches. Therefore, certain circuit variables from the comparative analysis are eliminated.

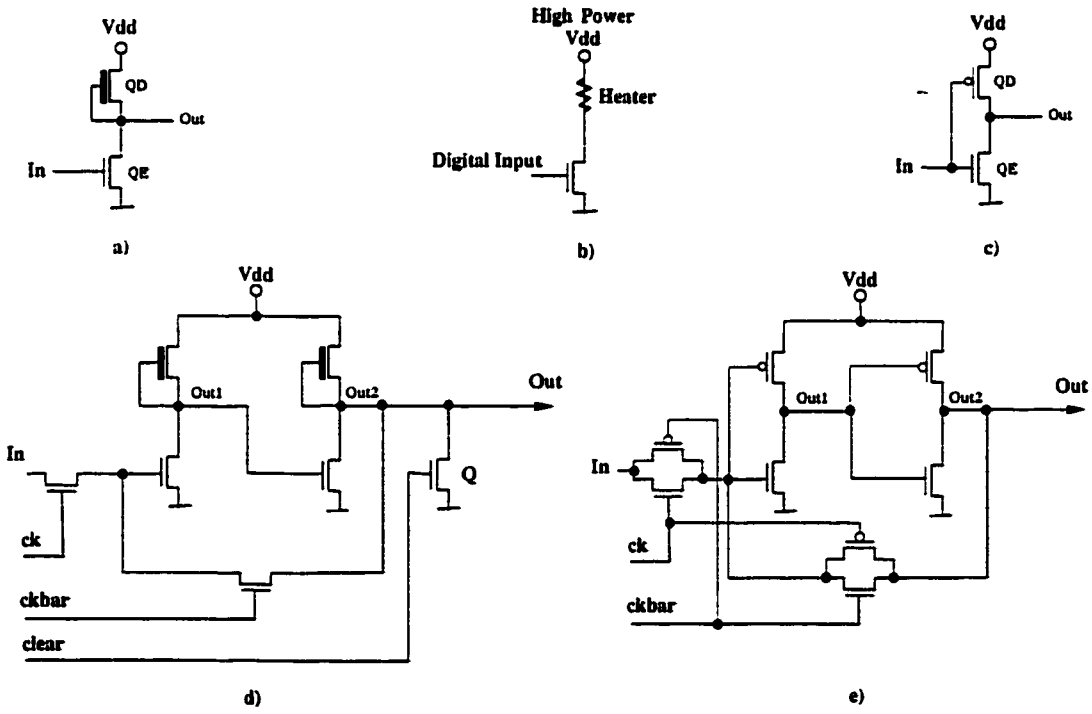


Figure 9.1: NMOS and CMOS test circuits: a) an NMOS inverter, b) NMOS and CMOS power driver, c) a CMOS inverter, d) an NMOS static slave latch, and e) a CMOS static latch.

The predriver is a voltage interface circuit converting a 5 volt digital input signal to a 13 volt digital output signal. This voltage interface circuit has been implemented using an asymmetrically sized NAND gate as shown in Fig. 9.2. The P1 and P2 PMOS transistors are sized to minimize the power dissipation when the *In* 1 and *In* 2 inputs are high, since all of the transistors, N1, N2, P1, and P2, are *on* in this situation. However, the size of the P1 and P2 transistors can not be too small since these transistors provide the low-to-high transition of the predriver output signal that drives the gate of the power driver. Therefore, a tradeoff between the power dissipation and the rise time of the low-to-high output transition of the predriver exists.

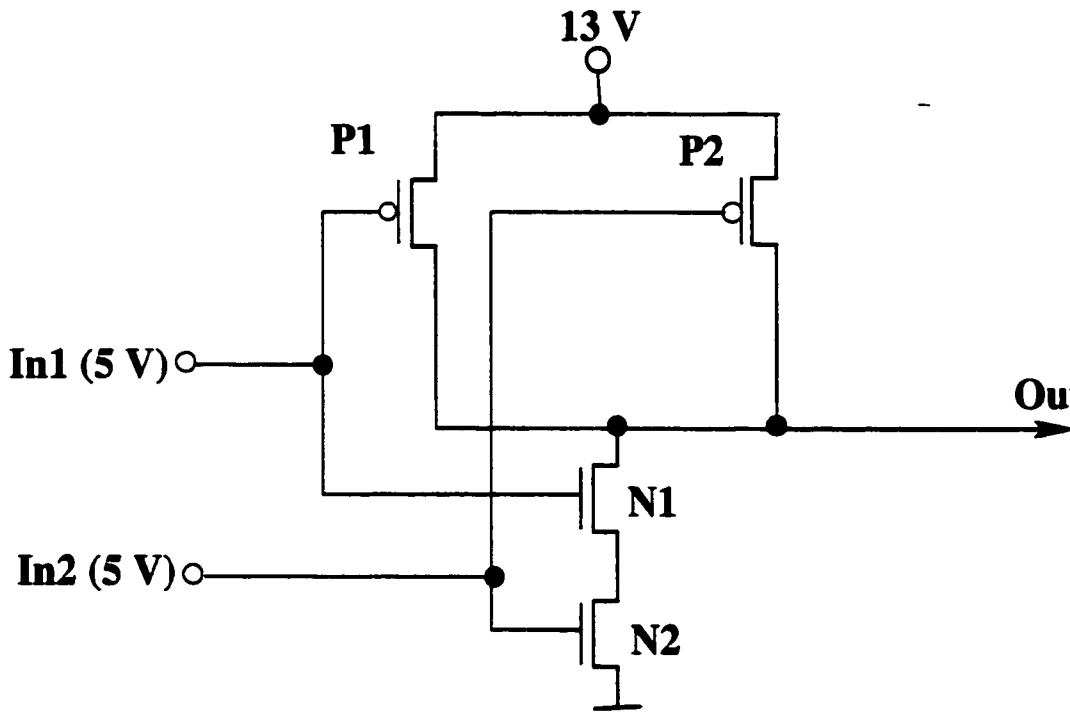


Figure 9.2: A CMOS NAND gate implementing a 5-to-13 volt voltage interface circuit

As an alternative to this interface circuit, the voltage interface circuit [118] shown in Fig. 9.3 has been used in some of the test circuits. The power dissipa-

tion, transition times, and speed are optimized, permitting the interface circuit to provide a high drive capability [118]. The low-to-high and high-to-low transitions for this voltage interface circuit are sharp (for the required load conditions) and approximately equal. However, these advantages have a drawback, a significant increase in the on-chip area required by the voltage interface circuit as compared to the NAND gate based interface circuit.

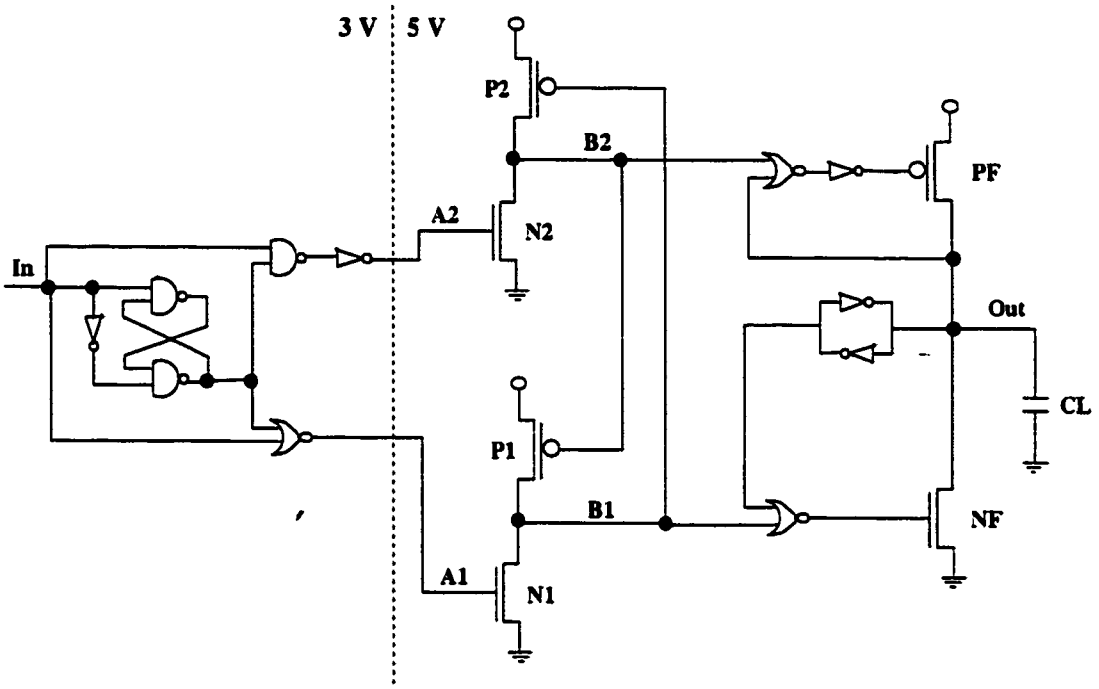


Figure 9.3: Schematic of an alternative CMOS voltage interface circuit

9.1.2 Physical design considerations

To accurately compare the theoretical and experimental results obtained for the NMOS circuits, the CMOS circuits have a similar floorplan as the NMOS circuits. The floorplan for the test circuits that use registers to monitor the influence of substrate noise is shown in Fig. 9.4. The differences between the

NMOS and CMOS circuits consist of: 1) the NMOS circuits feature 64 power drivers grouped in eight groups of eight power drivers each while the CMOS circuits feature 48 power drivers grouped in six groups of eight power drivers each, and 2) the NMOS circuits feature 32 master-slave sensitive registers placed in the upper side of the chip (see Fig. 9.4) while the CMOS circuits feature 20 master-slave registers, placed similar to the NMOS test circuits.

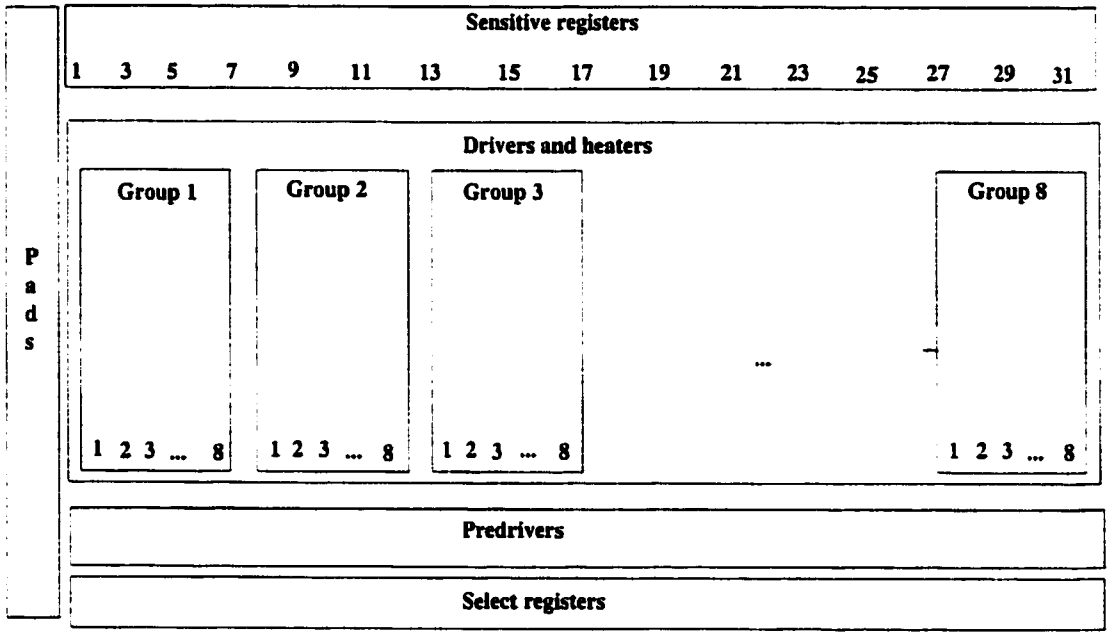


Figure 9.4: Floorplan of the NMOS and CMOS test circuits

A microphotograph of a CMOS test circuit that uses registers to monitor the substrate noise is shown in Fig. 9.5. As compared to the NMOS circuits, substrate contacts have been provided for each of the following: 1) each power driver has substrate contacts, similar to the NMOS power drivers, 2) certain test circuits have a ring surrounding the power drivers, 3) a substrate contact is provided for approximately every two gates, and 4) each N-well has a substrate contact. Note that the placement of the substrate contacts does not follow the complete

methodology described in Chapter 7; however, more substrate contacts than in the NMOS circuits are used. The test circuit shown in Fig. 9.5 uses the NAND gate based circuit as the predriver.

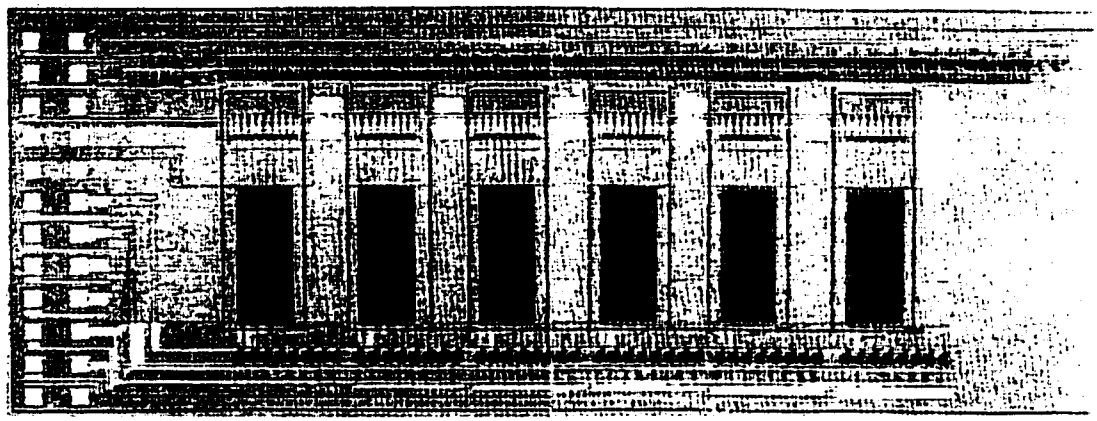


Figure 9.5: Microphotograph of CMOS test circuit

A microphotograph of a CMOS test circuit with substrate contacts to monitor the substrate noise is shown in Fig 9.6. The substrate contacts are placed according to the same ideas as described in Section 3.3.1 for the NMOS circuits in group 4. The test circuit shown in Fig 9.6 uses a voltage interface circuit optimized for power dissipation and area [118]. However, due to area constraints, only three independent interface circuits are used. The output of the first interface circuit simultaneously drives the power drivers 1, 2, and 3, the output of the second interface circuit drives the power drivers 4, 5, and 6, and the output of the third interface circuit drives the power drivers 7 and 8. The load of each voltage interface circuit is large as compared to the load of a NAND gate (when the NAND gate circuit is used as an interface circuit), but due to the considerable output drive current of the voltage interface circuit [118], the size of the load is less significant. A microphotograph of a test circuit designed specifically to test the voltage interface circuits is shown in Fig. 9.7.

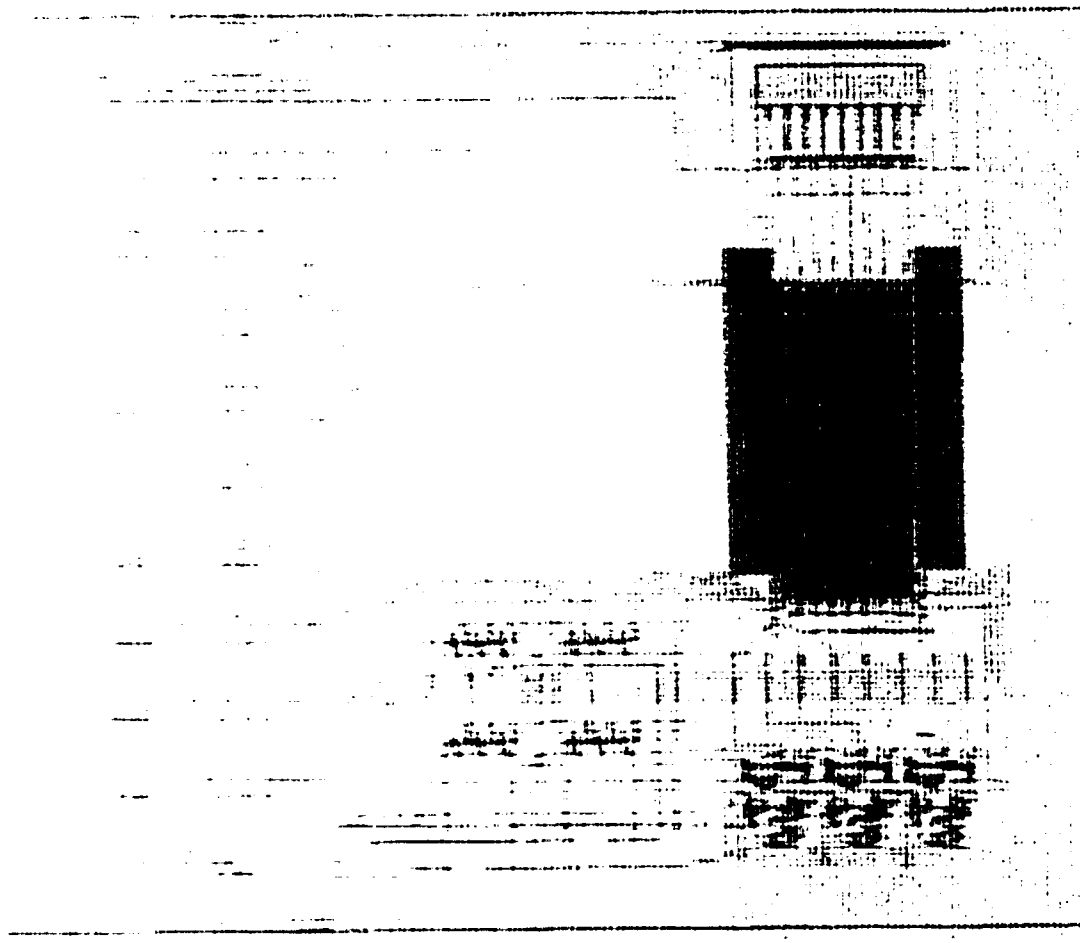


Figure 9.6: Microphotograph of a CMOS test circuit used to probe the substrate noise waveforms

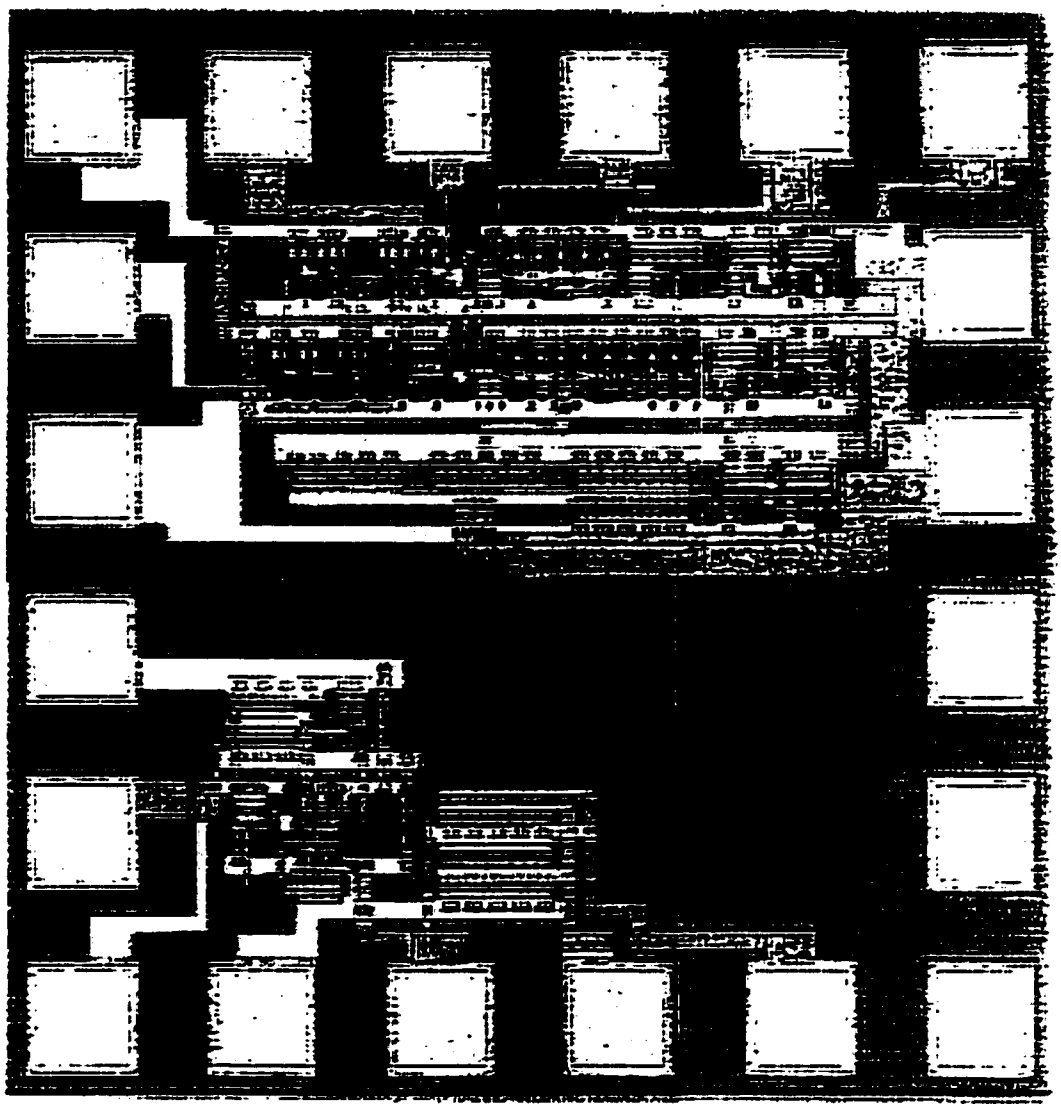


Figure 9.7: Microphotograph of a CMOS test circuit used to test the voltage interface circuits

9.2 Experimental data

The experimental data characterizing the noise behavior of the CMOS digital circuits are both similar and different to the noise behavior of the NMOS digital circuits. In this section, these similarities and differences between the two logic families are presented, discussed, and explained.

9.2.1 Latch-up and metastability

As discussed in Chapter 8, a smaller substrate noise amplitude is required to induce latch-up than to induce a parasitic transition at the output of a CMOS logic element. The test circuits which feature non-isolated power drivers generate a larger level of substrate noise than the test circuits which feature isolated power drivers, permitting the theoretical assumptions to be verified. The experimental data show that indeed, as expected, the test circuits which feature non-isolated power drivers are prone to substrate noise induced latch-up and metastability. When latch-up occurs, irreversible damage to the circuit is prevented by limiting the current generated by the logic power supply voltage. No latch-up or metastability has been noted for the test circuits featuring isolated power drivers.

Several of the issues that influence the noise sensitivity of the NMOS digital circuits (see Chapter 6) have been experimentally shown to also influence the noise sensitivity of the CMOS digital circuits. The sensitivity to latch-up and metastability of the test circuits which feature non-isolated power drivers has been experimentally shown to depend on:

- The pulse width on the gate of the power drivers (the time during which the power drivers are *on*)

- The power supply of the power drivers
- The turn on/off characteristics of the power drivers
- The number of power drivers that are active at any one time
- The skew of the turn on/off times of the power drivers

The latch-up behavior of the circuits featuring non-isolated power drivers as a function of the supply voltage of the power drivers when all six groups of power drivers are active for a 2 μs pulse is listed in Table 9.1. Latch-up is shown to not occur when only one group is active for a 2 μs pulse at 38 volts, or when eight groups are active at 38 volts and the turn-on/turn-off time of each of the groups is distributed (or skewed) in time over a 2 μs period.

Table 9.1: Latch-up behavior of CMOS test circuits with non-isolated power drivers as a function of the power supply voltage

Power supply (V)	38	34	30	26	22	20	18
Latch-up	Yes	Yes	Yes	Yes	Yes	Yes	No

Metastability is observed when the duration and/or amplitude of the substrate noise pulse is not sufficient to maintain but is sufficient to trigger the latch-up process [64, 102–106]. The metastable state (the output oscillation) is maintained by a positive feedback loop among the predriver, power driver, and the substrate and/or ground lines [119], as shown in Fig. 6.5 for the NMOS circuits. This positive feedback loop is responsible for developing an oscillatory substrate noise waveform [119] as shown in Fig. 6.3.

Test data also show that the noise generated as the power drivers turn-off is more likely to induce noise glitching than the noise generated as the power drivers turn-on. This behavior can be explained by noting that in order for the

two events to be similar from a noise point of view, the turn-on edge must be sufficiently sharp, and the power supply of the predrivers must be sufficiently high in order to produce a large voltage swing on the gate of the power drivers. Test data show that it is sufficient to skew the turn-off time of the active power drivers to reduce the influence of the substrate noise.

As previously described, these test circuits feature asymmetrically sized NAND gates as predrivers, and as a consequence, the turn-on edge of the power drivers is much slower that the turn-off edge (see Section 9.1). As also discussed, the amount of noise that is generated depends on the signal transition times. Therefore, the observed effect has a solid theoretical explanation. Driving the power drivers with the voltage interface circuit equalizes the noise effects of the turn-on and turn-off edges, which is actually an undesirable effect. Therefore, it is preferable to operate the NAND gates as an interface circuit, and to skew the turn-off edge of the power drivers to minimize the influence of this edge on the generated noise. The drawback of using NAND gates, however, is increased DC power dissipation, as discussed in Section 9.1. As an alternative to the increased power dissipation, a voltage interface circuit with reduced output drive can be used, thereby reducing the power dissipation and producing slower and equal transition times for the turn-on and turn-off signals at the power drivers. However, this solution requires increased area.

Another noteworthy aspect of this analysis is related to the effect of skewing the turn-off signals of the power drivers on the latch-up immunity. As discussed in Chapter 8, by skewing these pulses, T_{nl} increases, and therefore, a smaller V_{nl} amplitude (see Chapter 8) may induce latch-up. While this effect may occur, this effect did not occur in the specific experiments, not even for the non-isolated

power drivers (with large noise, or V_{nl}) and for eight skewed drivers (increased T_{nl}). Therefore, the $V_{nl} - T_{nl}$ relationship to induce latch-up is not satisfied.

9.2.2 Effects of process technology adjustments

Experimental data show that, in general, for the isolated power drivers, the sensitive registers are not affected, independent of the combination of the experimental test conditions such as the power supply of the power drivers, the pulse width, the number of drivers that are active at any one time, the skewing of the power drivers, and other test conditions. However, a difference is observed depending on the HV-well (high-voltage well) and the threshold voltage (V_T) doping concentrations. For increased doping levels, the registers in the vicinity of the active power drivers can be randomly affected from one pulse to another pulse. This phenomenon can be explained by noting the differences between the noise transmission process in a non-epitaxial technology as compared to an epitaxial technology [69, 120–122], which is primarily due to the low resistivity path through the bulk in an epi technology [120] (see Chapter 7). Three-dimensional noise distributions are shown in Chapter 7 for a non-epi and epi technology, respectively [120]. For high dopings in the HV-well and V_T regions, local non-epitaxial areas are created by making the doping level within the epitaxial layer closer to the doping level within the bulk. Another aspect that contributes to this behavior is the decreased threshold voltage of the transistors as the V_T doping levels increase. Test data show that the placement of the substrate contacts with respect to the sensitive registers and power drivers [120] can also affect the integrity of the stored data.

Certain conclusions can be drawn from these tests regarding the noise immunity of scaled and low voltage technologies. The transistors in scaled technologies are affected by small-channel effects such as mobility degradation and velocity saturation, due to the increase in the internal electric fields. A solution is to decrease the power supply and the threshold voltage (V_T) of the transistors. While the decrease in the power supply and threshold voltage can not be made at the same rate as the technology scaling factor, the electric fields are sufficiently decreased to improve the reliability of the transistors to acceptable levels. However, by decreasing the power supply and threshold voltage of the transistors, the speed of the circuits decreases. Also, the leakage and subthreshold currents of the MOS transistors increases substantially, creating significant levels of stand-by power dissipation which is unacceptable in million transistor systems. These leakage and subthreshold currents further increase due to substrate noise through effects such as the body effect. This situation is similar to the experimentally observed behavior caused by the increased V_T doping levels. Due to the large feature size (2.5 μm) and small number of transistors, the power dissipation caused by these parasitic currents (observed primarily for small amounts of substrate noise) is not significant in the target application [95]. As experimentally shown, only a large amount of noise is significant in this application, and the noted effect is a parasitic transition at the output of a logic element. However, in a scaled technology operating at a low power supply and featuring million transistors with small threshold voltages, a small amount of substrate noise can be significant. Even if the substrate noise levels are not sufficiently large to induce a parasitic transition, these noise levels do increase the currents caused by leakage and subthreshold conduction, thereby increasing the stand-by power dissipation of the system to unacceptable levels.

Reducing substrate noise in million transistor digital application is an important research problem in future microelectronic systems.

9.2.3 Data dependency

The experimental data demonstrates that the noise sensitivity of digital circuits increases as the HV-well and V_T dopings increase. To clarify this dependency, test circuits featuring isolated power drivers have been designed, manufactured, and evaluated. These circuits have been shown to have improved latch-up immunity due to the smaller substrate noise that is generated. For these circuits, the data stored in the registers is affected under certain conditions. While the stored data is affected in a predominantly random manner (see Section 9.2.2), weak dependencies on certain test conditions are noted. Although these dependencies are weak, they are noted here for several reasons. First, there is a certain similarity with the conditions in which the NMOS digital circuits are affected (see Chapter 6). This similarity demonstrates that the basic mechanisms in which the substrate noise affects any MOS circuit are, at their origin, similar (see Chapter 4). Second, while today these dependencies are for non-practical conditions (*e.g.*, very high dopings), these conditions will become more common as technologies become further scaled (see Section 9.2.2).

Experimental data demonstrate that the registers are affected primarily when the stored data is at logic high. This behavior can be explained by two aspects: 1) the transmission path of a parasitic *"high"* logic level inside a CMOS latch (see Fig. 9.1) for $D_{in} = 1$ (from one inverter directly to another inverter) and for $D_{in} = 0$ (through a transmission gate), and 2) the noise, generated as the power drivers turn-off (which has been shown to generate a larger amount of noise than

when the power drivers turn-on), affects primarily the *"high"* logic data signal stored in a register.

In addition, a dependence on the pulse duration, skew, and supply voltage of the power drivers, as well as on the number of power drivers that are active at any one time has also been noted. All of these dependencies have also been shown to be significant in NMOS circuits (see Chapter 6).

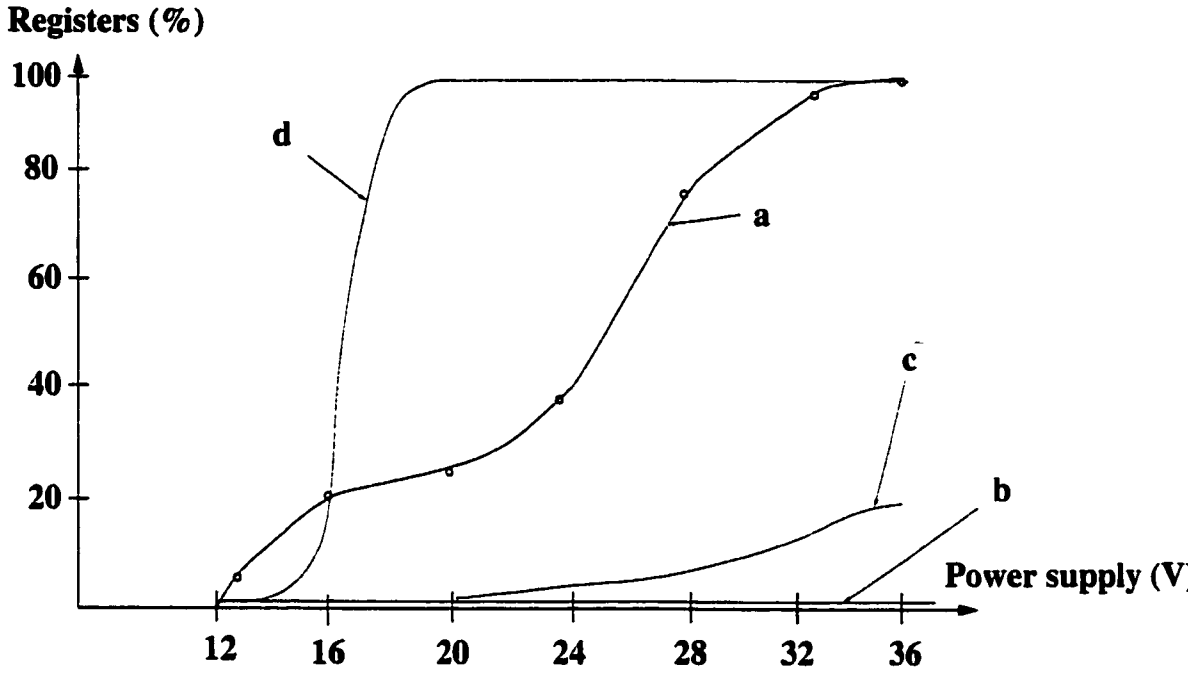


Figure 9.8: Experimental data characterizing the affected registers as a function of the supply voltage of the power drivers: a) NMOS circuits, b) isolated CMOS power drivers, c) isolated CMOS power drivers featuring high dopings, and d) non-isolated CMOS power drivers (latch-up and metastability)

A dependence on the distance between the power drivers and the sensitive registers has not been experimentally observed. This dependence is weak for NMOS circuits (see Chapter 6). An even weaker dependency is expected for CMOS circuits due to the propagation characteristics of the substrate noise in epi

technologies (see Chapter 7). This weaker dependence has been experimentally confirmed.

Among all of the dependencies between the substrate noise and the noise immunity of the CMOS digital registers mentioned here, the experimental data show that the most significant dependence is between the affected registers and the supply voltage of the power drivers. This dependence is shown in Fig. 9.8 for test circuits featuring both isolated and non-isolated power drivers. For comparison, a similar dependence for NMOS circuits is also shown in Fig. 9.8, where the affected registers are averaged over the four clocking regimes as described in [123] and in Chapter 6. The four curves shown in Fig. 9.8 are normalized with respect to the number of affected registers. Note that for curve d, once latch-up is induced, all of the registers are considered to be affected.

9.3 Conclusions

The theoretical and simulation-based results presented in Chapter 8 are confirmed by experimental data in this chapter. As shown in the simulation results, in order to induce a parasitic transition in a CMOS logic element, a substrate noise larger than 3 volts is required. This level of substrate noise is experimentally shown to be practically unachievable even in smart-power applications characterized by high levels of substrate noise. Experimentally, substrate noise induced latch-up is much more likely than substrate noise induced parasitic transitions. That behavior occurs because, as theoretically expected, a smaller amount of noise is required to induce latch-up and metastability than the noise level necessary to induce a parasitic transition. It is also shown that the CMOS logic circuits are much more tolerant to substrate noise than NMOS logic circuits. The NMOS

logic circuits are affected by substrate noise due to a multitude of factors as is described in Chapter 6. These factors are shown in this chapter to be much less important for CMOS logic circuits, only occuring under extreme conditions. The importance of substrate noise in high complexity, highly scaled technologies, featuring low power supplies and threshold voltages, have been experimentally demonstrated in this chapter.

Chapter 10

Conclusions

From the point of view of a circuit designer, any parasitic phenomenon that affects the correct operation of a circuit and therefore alters the performance of the circuit (as compared to the design specifications) represents a highly undesirable situation. Some parasitic phenomena are highly predictable, others are completely unpredictable. In many situations, the standard solution to these parasitic phenomena is to design a circuit with a sufficiently high margin of safety such that the circuit operates correctly under any reasonable conditions. However, the drawback of this design style is that the circuit is often designed to operate far from the maximum possible performance, whether it be dissipated power, area, speed, dynamic range, or analog processing accuracy. In the worst case, the allocated safety margin may be surpassed, destining the circuit to failure. To ensure that these highly undesirable situations are not encountered, parasitic phenomena must be well understood, and not just as a single problem, but in terms of the interactions and effects on the overall system.

Substrate coupling noise (SCN) belongs to this category of highly undesirable phenomena. This research effort focuses on understanding SCN as a global phenomenon, emphasizing a circuit and physical design perspective. Another focus

of this research effort has been the interactions of SCN with technology, circuit design, and physical layout. A final objective of this research effort has been the development of design techniques to minimize SCN.

A fair question that could be expected in a conclusions chapter of a dissertation treating SCN is *"how much noise is too much."* As always, especially in engineering, and as demonstrated throughout this research dissertation, the answer is *"it depends."* And to be more precise, it depends on whether the application is analog, digital, or mixed-signal, on specific circuit details, as well as the target performance of the application. It also depends on the nature of the noise aggressor. For example, a switching circuit and/or high voltage circuit generates more noise than a circuit operating in the analog domain and/or a low voltage circuit. The significance of the noise also depends on the characteristics of the noise victim. For example, a high precision analog processing circuit tolerates less noise than a digital circuit. All of these criteria are related to the performance characteristics of the application. For example, a digital application is likely to be more tolerant to noise than the analog portion of a mixed-signal application. Practically, the noise that can be tolerated by a digital application may be smaller than the noise tolerated by a mixed-signal application if the digital circuit is designed to achieve a high level of performance while the analog processing portion of the mixed-signal application is designed with a large safety margin. Finally, as has been shown in this dissertation, all of these issues depend upon both the technology and the circuit implementation. For example, a CMOS technology is shown to be significantly more tolerant to SCN than an NMOS technology and static circuits are more tolerant to SCN than dynamic circuits.

Another conclusion of this dissertation is that it is possible to enhance the tolerance of a system to SCN by employing circuit and physical design techniques, thereby not requiring expensive technological enhancements. Certain technological enhancements may have a significant impact on the sensitivity of circuits to SCN. Therefore, an important issue is the sensitivity of the implementing technology to SCN. The focus of this dissertation is on developing circuit and physical design techniques that improve the noise behavior of a given technology.

Another conclusion of this dissertation is that despite the relative behavior of circuits to SCN depending upon whether the circuit is analog or digital, static or dynamic, or NMOS or CMOS, common characteristics still exist. The source of these common characteristics is the low level circuit fundamentals and phenomena which are strongly dependent on the behavior of the technology specific transistors.

Interactions and implications of SCN at levels such as technology, device, circuit, and system have been described throughout this dissertation. It is demonstrated here that it is possible to design a system which features high SCN immunity; however, the complexity of the problem remains considerable. The focus of the design effort is to:

- Assess the application at the system level and decide, depending upon the target performance, what range of SCN is tolerable (such as the noise amplitude and uniformity) for the sensitive circuits.

- Assess the available technology, model parameters, and circuit issues related to SCN such as the body effect, latch-up, short-channel effects, and subthreshold conduction.

- Design the system at the circuit and physical levels to satisfy the target performance specifications. The design process consists of employing aggressor circuit structures that generate the lowest amount of noise and victim circuit structures that tolerate the greatest amount of noise. The objective is to reduce the deleterious effects of SCN by producing optimal SCN characteristics such as low amplitude and high uniformity noise. All of these issues must tradeoff system performance requirements such as the total system power dissipation and area, since there may be circuits that are highly tolerant to SCN (either generate small amounts of noise or tolerate large amounts of noise) but dissipate large amounts of power or occupy a significant amount of area.

In terms of the future of SCN, as the circuit and technological complexity of microelectronic systems increases, the importance of SCN will also increase. Therefore, high performance systems will operate at increasingly higher levels of substrate coupling noise. Presently SCN is particularly significant in mixed-signal circuits, attention, however, will soon shift to multi-million transistor DSM low-voltage digital applications. This trend of SCN affecting digital systems will occur as the stand-by power dissipation generated by the parasitic currents caused by leakage and subthreshold conduction in the presence of even smaller levels of SCN will increase to unacceptable levels in multi-million transistor applications.

In summary, SCN will become increasingly important as circuit performance increases as long as a common substrate is shared. Research in SCN will therefore be required in new areas such as multi-million transistor DSM digital applications. In order to efficiently cope with the increasing importance of SCN and, in general, with on-chip noise, novel circuit approaches must be employed, such

as differential digital circuit structures [124]. These noise issues will also need to be integrated into computer-aided design (CAD) tools in order to efficiently deal with the complex problems caused by substrate coupling noise.

Chapter 11

Future Work

As the circuit and technological complexity of microelectronic systems increases and as long as there is a common substrate, the importance of substrate coupling noise (SCN) will increase whether the circuit be digital, analog, or mixed-signal. SCN, however, is not significant in silicon-on-insulator (SOI) circuits. While researchers are presently evaluating a variety of different issues in SOI, there still remains significant technology maturation before SOI begins to dominate over bulk technologies due to reasons such as yield, process control, and related cost issues. As a consequence, solutions must be developed to successfully and reliably manage the effects of SCN. Focus on non-technological solutions is preferable, specifically, on circuit and physical design solutions that address mainstream technologies such as DSM CMOS digital technologies.

DSM CMOS is the primary technology targeted for implementing systems-on-a-chip (SOC) applications. SOCs are typically composed of a variety of analog, digital, high power, low voltage, and/or high voltage circuit blocks. Complex interactions among these diverse circuit blocks occur in the SOCs, either through the common substrate or through parasitic coupling among the interconnect. Therefore, SCN in SOCs is a particularly challenging problem. There are two primary

approaches that may be employed to address this highly challenging problem of increasing SCN in future microelectronic systems: design tool development and novel circuit approaches. While presently, research on SCN has focused on analog signal processing circuit blocks, attention is expected to shift towards the issue of SCN affecting digital signal processing circuit blocks.

The implications of substrate coupling noise on future multi-million transistor DSM digital systems are discussed in Section 11.1. The challenge of developing effective design tools that consider SCN are outlined in Section 11.2. Novel circuit structures represent a potentially useful strategy for managing SCN. This approach is highlighted in Section 11.3. Finally, this chapter concludes with Section 11.4.

11.1 The implications of substrate coupling noise on DSM digital circuits

The research presented in this dissertation has focused primarily on the behavior of digital circuits under substrate noise. Therefore, this dissertation can be seen as an initial point for attacking a problem that will be of increasing importance in the near future: substrate coupling noise in digital applications. In present digital microelectronic systems, substrate coupling noise is not yet a highly critical problem requiring dedicated solutions. Current research in SCN is focused on mixed-signal applications where the noise generated in the substrate by high speed digital circuits can affect the sensitive analog circuitry. The effect of high power circuits on the digital control circuitry is the focus of this dissertation.

Two new applications for research in SCN can be foreseen: mixed-signal systems-on-a-chip (SOC) and multi-million transistor DSM digital systems. While SOCs will benefit from the current research in SCN, a different analysis will be necessary for digital systems. As suggested in this dissertation, the analysis of next generation digital systems must be at an analog level in order to solve the many complex low level problems that will arise. Digital circuits and systems must be treated as analog entities; for example, further optimization can be achieved if a signal transition is considered as continuous rather then as two discrete voltages [116–118, 124, 125].

Substrate noise in a digital system is generated primarily by the high switching activity and large buffers driving the interconnect (these buffers can be seen as power drivers as in the smart-power application analyzed here). As shown in Chapter 9, research in substrate coupling noise in digital systems will be driven by the need to reduce stand-by power dissipation caused by increasing leakage and subthreshold conduction currents. SCN will also degrade the performance of the logic elements. Therefore, design tools and novel circuit approaches are two important solutions that need to be developed to manage these new challenges.

11.2 Design tool development

Similar to any new field or research area, a limited amount of research has dealt with the complex design problems caused by SCN, particularly since the appropriate design approach may vary from circuit to circuit. A solution to cope with this limited expertise consists of developing design tools that can address SCN-related problems. The development of design tools for SCN should satisfy the following objectives:

- Substrate modeling. The complexity of the substrate model depends upon the target application. While for certain applications modeling the substrate as a resistive mesh is sufficient, for other higher frequency applications an *RC* or *RLC* model may be necessary.

- Interconnect modeling. As mentioned throughout this dissertation, the interconnect system is highly related to the substrate. Therefore, the effects of the interconnect must be included in a comprehensive SCN analysis tool.

- Modeling the noise sources and noise receptors. As described in this dissertation, a noise source injects a parasitic current into the substrate. This parasitic current affects the operation of the sensitive transistors. Therefore, a model for the noise source and noise receptors should provide:

  - A technology dependent device analysis capability which produces the magnitude and distribution of the parasitic current generated within the substrate. This current must account for the specific circuit conditions in which the device operates, such as the operating point of the device. The value of the current must also account for the specific device and circuit behavior, such as short-channel effects, the body effect, and parasitic interconnect effects (such as generated by the ground routing, substrate contact placement, and interconnect noise).

  - The parasitic current should be injected into the substrate at the location of the device.

  - This current is distributed within the substrate. Therefore, part of the parasitic current reaches each transistor within the noise sensitive circuits. For each transistor, this current must be determined and

modeled in terms of the position of the on-chip transistor with respect to the local substrate. Modeling elements describing the influence of this parasitic current on the transistor operation must be considered within the device model, and back annotated into a circuit simulation file. The current affecting a transistor is dependent on the placement of the substrate contacts. Therefore, a substrate contact placement methodology must also be considered during this phase.

- The noise generation, transmission, and reception process to properly model and capture the noise process within a circuit simulator is completed. The circuit simulator will use this information to simulate the circuit operation in the presence of noise.

- A tool to generate the optimal transistor placement for minimum substrate noise interactions may be appropriate. This transistor placement information will be used when routing the interconnect. The interconnect routing should be designed to minimize the influence of interconnect noise and/or ground bounce.

11.3 Novel circuit approaches

By using appropriate expertise and design tools, SCN can be minimized although not eliminated. Additional strategies can be used, such as exploiting novel circuits which generate less noise or tolerate larger noise. Multiple solutions to achieve this objective have been suggested within this dissertation. For digital circuits, low-swing and differential circuits [124] are useful approaches for generating less noise while tolerating greater noise. For analog circuits, differential,

high slew-rate, redundant circuit structures may be effective for tolerating large amounts of noise. For high-voltage circuits, solutions involving serial devices for synchronously switching the high voltages have demonstrated promising results (each device switches only a portion of the high voltage, thereby generating less noise). Optimizing existing circuit structures, such as the load, transistor size, circuit family, clocking and data conditioning signals and circuitry, can also be employed.

11.4 Conclusions

In engineering and science, one's imagination and ideas are the only limitations towards finding a solution to a problem. Engineers and scientists always seem to find solutions to problems that originally appeared to be a fundamental limit. Ingredients for success are always good ideas, inspiration, enthusiasm, desire, and the willingness to make a sustained effort. If a team is also available, there is no frontier...

Bibliography

[1] G. K. Teal, "Single Crystals of Germanium and Silicon – Basic to the Transistor and Integrated Circuit," *IEEE Transactions on Electron Devices*, Vol. ED-23, No. 7, pp. 621–639, July 1976.

[2] W. F. Brinkman, D. E. Haggan, and W. W. Troutman, "A History of the Invention of the Transistor and Where it Will Lead Us," *IEEE Journal of Solid-State Circuits*, Vol. 32, No. 12, pp. 1858–1865, December 1997.

[3] J. Bardeen and W. H. Brattain, "The Transistor, a Semiconductor Triode," *Physical Review*, Vol. 74, pp. 230–231, July 1948.

[4] J. Bardeen and W. H. Brattain, "Physical Principles Involved in Transistor Action," *Physical Review*, Vol. 75, pp. 1208–1225, April 1949.

[5] W. Shockley, "The Theory of p-n Junctions in Semiconductors and p-n Junction Transistors," *Bell System Technical Journal*, Vol. 28, pp. 435–489, July 1949.

[6] M. Atalla, E. Tannenbaum, and E. J. Scheinber, "Stabilization of Silicon Surfaces by Thermally Grown Oxides," *Bell System Technical Journal*, Vol. 36, No. 3, pp. 749–783, May 1959.

[7] B. Deal and A. Grove, "General Relationship for the Thermal Oxidation of Silicon," *Journal of Applied Physics*, Vol. 36, No. 12, pp. 3770–3778, December 1965.

[8] J. A. Hoerni, "Planar Silicon Transistors and Diodes," *IRE Transactions on Electron Devices*, Vol. ED-8, No. 2, p. 178, March 1961.

[9] D. Kahng, "A Historical Perspective on the Development of MOS Transistors and Related Devices," *IEEE Transactions on Electron Devices*, Vol. ED-23, No. 7, pp. 655–657, July 1976.

[10] R. E. Kerwin, D. L. Klein, and J. C. Sarace, "Method for Making MIS Structures," *U. S. Patent 3,475,234*, filed March 27, 1967, issued October 28 1969.

[11] F. Faggin and M. Shima, "The History of the 4004," *IEEE Micro*, Vol. 16, No. 6, pp. 10–20, December 1996.

[12] M. B. Rudin and R. Jenkins, "System/Circuit Device Considerations in the Design and Development of a D/A and A/D Integrated Circuits Family," *Proceedings of the IEEE International Solid-State Circuits Conference*, pp. 11–12, February 1967.

[13] J. J. Pastoriza and A. A. Molinari, "High Performance Monolithic D/A Converter Circuit," *Proceedings of the IEEE International Solid-State Circuits Conference*, pp. 122–123, February 1970.

[14] D. J. Doley, "A Complete Monolithic 6-bit D/A Converter," *Proceedings of the IEEE International Solid-State Circuits Conference*, pp. 50–51, February 1971.

[15] D. R. Breuer, "High-Speed A/D Converter Monolithic Techniques," *Proceedings of the IEEE International Solid-State Circuits Conference*, pp. 146–147, February 1972.

[16] A. Marshall, "Intelligent Power Integrated Circuit-History and Overview," *Texas Instruments Technical Journal*, Vol. 11, No. 2, pp. 2–9, March/April 1994.

[17] H. Bierman, "Smart Power ICs Move from Promise to Production," *Electronics*, Vol. 31, pp. 40–45, August 5 1985.

[18] J. Korec, "Silicon-on-Insulator Technology for High-Temperature Smart-Power Applications," *Materials Science and Engineering B-Solid-State Materials for Advanced Technology*, Vol. B29, No. 1-3, pp. 1–6, January 1995.

[19] R. Frank and B. Dunn, "Future Cars to Employ More Smart Power ICs," *Power Conversion and Intelligent Motion*, Vol. 15, No. 2, pp. 22–27, February 1989.

[20] A. Marshall and K. Buss, "Automotive Semiconductor Switch Technologies," *IEEE Workshop on Electronics and Applications in Transportation*, pp. 68–72, October 1990.

[21] M. Glogolja and J. Tihanyi, "Smart-SIPMOS-an Intelligent Power Switch," *IEEE Industry Applications Society Annual Meeting*, Vol. 1, pp. 423–433, August 1986.

[22] B. Murari, "Reliability of Smart Power Devices," *Microelectronics and Reliability*, Vol. 37, No. 10-11, pp. 1735–1742, October/November 1997.

[23] S. Krishna and I. S. Gaeta, "An Analog Technology Integrates Bipolar, CMOS, and High-Voltage DMOS Transistors," *IEEE Transactions on Electron Devices*, Vol. ED-31, No. 1, pp. 89–95, January 1984.

[24] T. Sakurai and A. R. Newton, "Alpha-Power Law MOSFET Model and its Applications to CMOS Inverter Delay and Other Formulas," *IEEE Journal of Solid-State Circuits*, Vol. SC-25, No. 2, pp. 584–594, April 1990.

[25] R. R. Troutman, "Latchup in CMOS Technologies," *IEEE Circuits and Devices Magazine*, Vol. 3, No. 3, pp. 15–21, May 1987.

[26] R. R. Troutman, "Recent Developments in CMOS Latchup," *Proceedings of the IEEE International Electron Devices Meeting*, pp. 296–299, December 1984.

[27] R. R. Troutman and H. P. Zappe, "Layout and Bias Considerations for Preventing Transiently Triggered Latchup in CMOS," *IEEE Transactions on Electron Devices*, Vol. ED-31, No. 3, pp. 315–321, March 1984.

[28] R. R. Troutman and M. J. Hargrove, "Transmision Line Model for Latchup in CMOS Circuits," *Proceedings of the IEEE Symposium on VLSI Technology*, pp. 56–59, September 1983.

[29] R. R. Troutman and H. P. Zappe, "Power-up Triggering Conditions for Latch-up in Bulk CMOS," *Proceedings of the IEEE Symposium on VLSI Technology*, pp. 52–53, September 1982.

[30] Burr-Brown Corporation, "Burr-Brown IC Data Book," *Digital to Analog Converters*, Tucson, AZ, 1989-1998.

[31] Merriam-Webster Inc., "Merriam-Webster's Collegiate Dictionary," *Tenth Edition*, Springfield, MA, 1997-1998.

[32] S. M. Sze, *Physics of Semiconductor Devices*. John Wiley & Sons, Inc., 1969.

[33] A. V. Oppenheim and A. S. Willsky, *Signals and Systems*. Prentice-Hall, Inc., 1997.

[34] M. E. Thomas and I. A. Saadat, "VLSI Interconnect Options For On-Chip High Performance Applications," *Proceedings of the Wescon Conference*, pp. 318–322, November 1991.

[35] J. C. Blankenhorn, "MCM Interconnect Considerations," *Proceedings of the National Electronic Packaging and Production Conference (NEPCON)*, pp. 141–152, June 1994.

[36] R. C. Frye, P. R. Smith, and Y. L. Low, "Inductive Crosstalk Between Integrated Passive Components in RF-Wireless Modules," *Proceedings of the IEEE International Conference on Multichip Modules and High Density Packaging*, pp. 496–500, April 1998.

[37] A. Deutsch, H. Smith, G. A. Katopis, W. D. Becker, P. W. Coteus, and P. J. Reslte, "The Importance of Inductance and Inductive Coupling for On-chip Wiring," *Proceedings of the IEEE Electrical Performance of Electronic Packaging Conference*, pp. 53–56, October 1997.

[38] T. Sakurai, "Closed-Form Expressions for Interconnection Delay, Coupling, and Crosstalk in VLSI's," *IEEE Transactions on Electron Devices*, Vol. 40, No. 1, pp. 118–124, January 1994.

[39] S. C. Wong, P. S. Liu, J. W. Ru, and S. T. Lin, "Interconnection Capacitance Models for VLSI Circuits," *Solid-State Electronics*, Vol. 42, No. 6, pp. 969–977, June 1998.

[40] M. Gilligan and S. Gupta, "A Methodology for Estimating Interconnect Capacitance for Signal Propagation Delay in VLSI," *Microelectronics Journal*, Vol. 26, No. 4, pp. 327–336, May 1995.

[41] D. H. Cho, Y. S. Eo, and H. S. Park, "Interconnect Capacitance, Crosstalk, and Signal Delay for 0.35 μm CMOS Technology," *Proceedings of the IEEE International Electron Devices Meeting*, pp. 619–622, December 1996.

[42] A. B. Dowlatabadi, "Challenges in CMOS Mixed-Signal Designs for Analog Circuit Designers," *Proceedings of the IEEE Midwest Symposium on Circuits and Systems*, Vol. 1, pp. 47–50, August 1997.

[43] B. R. Stanisic, R. A. Rutenbar, and L. R. Carley, "Mixed-Signal Noise Decoupling via Simultaneous Power Distribution Design and Cell Customization in RAIL," *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 533–536, May 1994.

[44] G. B. Bronner and B. Machesney, "Epitaxy Over Trench Technology for ULSI DRAMs," *Proceedings of the IEEE Symposium on VLSI Technology*, pp. 21–22, May 1988.

[45] J. M. Casalta, X. Aragones, and A. Rubio, "Substrate Coupling Evaluation in BiCMOS Technology," *IEEE Journal of Solid-State Circuits*, Vol. 32, No. 4, pp. 598–603, April 1997.

[46] M. I. C. Simas, P. Santos, P. Casimiro, and M. Lanca, "Smart Power in MOS Technologies – An Overview," *Proceedings of the IEEE International Symposium on Industrial Electronics*, Vol. 2, pp. 371–376, February 1997.

[47] T. Ifstrom and B. Hofflinger, "A Smart Power Process in 'Direct-Bonded' Silicon on Insulator with 150 V VDMOS, CMOS and Bipolar Transistors," *Microelectronic Engineering*, Vol. 19, No. 1-4, pp. 153–156, September 1992.

[48] B. J. Baliga, "A Power Integrated Circuits - A Brief Overview," *IEEE Transactions on Electron Devices*, Vol. ED-33, No. 12, pp. 1936–1939, December 1986.

[49] W. W. T. Chan and S. S. Wong, "A Power IC Technology with Excellent Cross-Talk Isolation," *IEEE Electron Device Letters*, Vol. 17, No. 10, pp. 467–469, October 1996.

[50] J. A. Appels and H. M. J. Vaes, "High Voltage Thin Layer Devices (RESURF Devices)," *Proceedings of the IEEE International Electron Devices Meeting*, pp. 238–241, December 1979.

[51] J. L. Sutor and L. Terry, "A Novel Isolation Structure for Smart Power ICs," *Proceedings of the IEEE International Electron Devices Meeting*, pp. 214–217, December 1986.

[52] M. J. M. Pelgrom and M. Vertregt, "CMOS Technology for Mixed Signal ICs," *Solid-State Electronics*, Vol. 41, No. 7, pp. 967–974, July 1997.

[53] B. Gilbert, "The Synergy of BiCMOS in Analog Cell Design," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2681–2682, May 1992.

[54] M. Bafleur and T. Laopoulos, "Cost-Effective Smart Power CMOS/DMOS Technology: Design of Main Driving and Protection Functions," *Analog Integrated Circuits and Signal Processing*, Vol. 8, No. 3, pp. 233–246, November 1995.

[55] L. Forbes, W. T. Lim, and K. T. Yan, "Guard Ring Diodes for Suppression of Substrate Noise and Improved Reliability in Mixed-Mode CMOS Circuits," *Proceedings of the IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits*, pp. 145–148, November 1995.

[56] K. M. Fukuda, S. Maeda, T. Tsukuda, and T. Matsuura, "Substrate Noise Reduction Using Active Guard Band Filters in Mixed-Signal Integrated Circuits," *IEICE Transactions on Fundamentals of Electronics, Communications, and Computer Sciences*, Vol. E80-A, No. 2, pp. 313–320, February 1997.

[57] M. Nagatomo and T. Matsukawa, "A High Density 4M DRAM Process Using Folded Bitline Adaptive Side-Wall Isolated Capacitor (FASIC) Cell,"

Proceedings of the IEEE International Electron Devices Meeting, pp. 144–147, December 1986.

[58] T. J. Rodgers and J. D. Meindl, "An Experimental and Theoretical Analysis of Double-Diffused MOS Transistors," *IEEE Journal of Solid-State Circuits*, Vol. SC-10, No. 5, pp. 322–331, October 1975.

[59] H. L. Lin and W. N. Jones, "Computer Analysis of the Double-Diffused MOS Transistor for Integrated Circuits," *IEEE Transactions on Electron Devices*, Vol. ED-20, No.3, pp. 275–283, March 1973.

[60] K. Ohta and Y. Tarui, "Quadruply Self-Aligned MOS (QSA MOS)-a New Short-Channel High-Speed High-Density MOSFET for VLSI," *IEEE Transactions on Electron Devices*, Vol. ED-27, No. 8, pp. 1352–1358, August 1980.

[61] T. Hosoya and S. Matsuo, "A Self-Aligning Contact Process for MOS LSI (RAM Fabrication)," *IEEE Transactions on Electron Devices*, Vol. ED-28, No. 1, pp. 77–82, January 1981.

[62] M. Koyanagi and N. Hashimoto, "A 5-V Only 16-kbit Stacked-Capacitor MOS RAM," *IEEE Transactions on Electron Devices*, Vol. ED-27, No. 8, pp. 1596–1601, August 1980.

[63] A. G. Lewis and J. Y. Chen, "Three-Dimensional Effects in CMOS Latch-up," *Proceedings of the IEEE International Electron Devices Meeting*, pp. 248–251, December 1986.

[64] B. L. Gregory and B. D. Shafer, "Latch-up in CMOS Integrated Circuits," *IEEE Transactions on Nuclear Science*, Vol. NS-20, No. 6, pp. 293–299, December 1973.

[65] T. Ohzone and T. Hirao, "Silicon-Gate N-well CMOS Process by Full Ion-Implantation Technology," *IEEE Transactions on Electron Devices*, Vol. ED-27, No. 9, pp. 1789–1795, September 1980.

[66] U. Schwabe and T. Takacz, "N- and P-well Optimization for High-Speed N-Epitaxy CMOS Circuits," *IEEE Transactions on Electron Devices*, Vol. ED-30, No. 10, pp. 1339–1344, October 1983.

[67] T. Yamaguchi and G. C. Eiden, "Process and Device Performance of Submicrometer-Channel CMOS Devices Using Deep-Trench Isolation and Self-Aligned $TiSi_2$ Technologies," *IEEE Transactions on Electron Devices*, Vol. ED-32, No. 2, pp. 184–193, February 1985.

[68] R. Roop, "Trends in High Voltage Integrated Circuit Technology," *Solid-State Technology*, Vol. 27, No. 5, pp. 147–151, May 1984.

[69] D. K. Su and B. A. Wooley, "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits," *IEEE Journal of Solid-State Circuits*, Vol. 28, No. 4, pp. 420–430, April 1993.

[70] X. Aragones and A. Rubio, "Analysis and Modelling of Parasitic Substrate Coupling in CMOS Circuits," *IEE Proceedings–Circuits, Devices and Systems*, Vol. 142, No. 5, pp. 307–312, October 1995.

[71] S. Masui, "Simulation of Substrate Coupling in Mixed-Signal MOS Circuits," *Proceedings of the IEEE International Symposium on VLSI Circuits*, pp. 42–43, June 1992.

[72] T. Blalack and B. A. Wooley, "Experimental Results and Modeling of Noise Coupling in a Lightly Doped Substrate," *Proceedings of the IEEE International Electron Devices Meeting*, pp. 623–626, December 1996.

[73] K. M. Fukuda and M. Hotta, "Voltage-Comparator-Based Measurement of Equivalently Sampled Substrate Noise Waveforms in Mixed-Signal Integrated Circuits," *IEEE Journal of Solid-State Circuits*, Vol. 31, No. 5, pp. 726–731, May 1996.

[74] MEDICI, "A Two Dimensional Device Simulator Program," *Technology Modeling Associated, Inc.*, Palo Alto, CA 1993.

[75] TMA PISCES-IIB, "A Two-Dimensional Device Analysis Program with Circuit Analysis AAM," *Technology Modeling Associated, Inc.*, July 1991.

[76] E. Chiprout, "Interconnect and Substrate Modeling and Analysis: An Overview," *IEEE Journal of Solid-State Circuits*, Vol. 39, No. 9, pp. 1445–1452, September 1998.

[77] N. K. Verghese, D. J. Allstot, and M. Wolfe, "Fast Parasitic Extraction for Substrate Coupling in Mixed-Signal ICs," *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 121–124, May 1995.

[78] A. J. V. Genderen and T. Smedes, "Fast Computation of Substrate Resistances in Large Circuits," *Proceedings of the European Design and Test Conference*, pp. 560–565, March 1996.

[79] T. A. Johnson and W. Wang, "Chip Substrate Resistance Modeling Technique for Integrated Circuit Design," *Proceedings of the IEEE International Symposium on Circuits and Systems*, Vol. 2, pp. 762–765, May 1983.

[80] I. L. Wemple and A. T. Yang, "Integrated Circuit Substrate Coupling Models Based on Voronoi Tesselation," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 14, No. 12, pp. 1459–1469, December 1995.

[81] N. K. Verghese, D. J. Allstot, and S. Masui, "Rapid Simulation of Substrate Coupling Effects in Mixed-Mode ICs," *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 18.3.1–18.3.4, May 1993.

[82] K. J. Kerns, I. L. Wemple, and A. T. Yang, "Efficient Parasitic Substrate Modeling for Monolithic Mixed-A/D Circuit Design and Verification," *Analog Integrated Circuits and Signal Processing*, Vol. 10, No. 1/2, pp. 7–21, June/July 1996.

[83] N. K. Verghese, D. J. Allstot, and M. A. Wolfe, "Verification Techniques for Substrate Coupling and Their Application to Mixed-Signal IC Design," *IEEE Journal of Solid-State Circuits*, Vol. 31, No. 3, pp. 354–365, March 1996.

[84] R. Singh and S. Sali, "Method for Modeling Substrate Coupling in Large Chip Designs," *Electronic Letters*, Vol. 33, No. 11, pp. 952–954, May 1997.

[85] R. Singh and S. Sali, "Efficient Modelling of Substrate Noise and Coupling in Mixed-Signal SPICE Designs," *Electronic Letters*, Vol. 33, No. 11, pp. 132–134, February 1997.

[86] S. Ramo, J. R. Whinnery, and T. Van Duzer, *Fields and Waves in Communication Electronics*. John Wiley & Sons, 1965.

[87] R. E. Matick, *Transmission Lines for Digital and Communication Networks*. McGraw-Hill, Inc., 1969.

[88] R. E. Collin, *Foundations for Microwave Engineering*. McGraw-Hill, Inc., 1992.

[89] S. Kumasiro and A. J. Strojwas, "A New Efficient Method for the Transient Simulation of Three-Dimensional Interconnect Structures," *Proceedings of the IEEE International Electron Devices Meeting*, pp. 193–196, December 1990.

[90] M. P. Vidal and G. Sarrabayrouse, "Floating Well Based Design Methodology Aimed to Improve Latch-up Immunity in a Smart Power Technology," *Microelectronic Engineering*, Vol. 19, No. 1-4, pp. 161–164, September 1992.

[91] B. R. Stanisic, N. K. Verghese, and D. J. Allstot, "Addressing Substrate Coupling in Mixed-Mode IC's: Simulation and Power Distribution Synthesis," *IEEE Journal of Solid-State Circuits*, Vol. 29, No. 3, pp. 226–238, March 1994.

[92] J. A. Olmstead and S. Vulih, "Noise Problems in Mixed Analog-Digital Integrated Circuits," *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 659–662, May 1987.

[93] S. Mitra and D. J. Allstot, "Substrate-Aware Mixed-Signal Macro-Cell Placement in WRIGHT," *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 529–532, May 1994.

[94] T. Yeung and F. J. R. Clement, "Noise Coupling in Heavily and Lightly Doped Substrate from Planar Spiral Inductor," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 1405–1408, June 1997.

[95] E. Peeters and S. Verdonckt-Vandebroek, "Thermal Ink Jet Technology," *IEEE Circuits and Devices Magazine*, Vol. 13, No. 4, pp. 19–23, July 1997.

[96] J. M. Rabaey, *Digital Integrated Circuits, A Design Perspective.* Prentice-Hall, Inc, 1996.

[97] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits Analysis and Design.* McGraw Hill, 1996.

[98] Cadence Design Tools, "Cadence Design Systems, Inc.," *San Jose*, CA, 1998.

[99] R. Troutman, *Latchup in CMOS Technology: the Problem and Its Cure.* Kluwer Academic Publishers, 1986.

[100] D. B. Estreich, "The Physics and Modeling of Latch-up in CMOS Integrated Circuits," *Technical Report No. G-2-1-9*, Integrated Circuits Laboratory, Stanford Electronics Lab., Stanford University, November 1980.

[101] D. B. Estreich and R. W. Dutton, "Modeling Latch-up in CMOS Integrated Circuits and Systems," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. CAD-1, No. 4, pp. 347–354, October 1982.

[102] W. M. Coughran, M. R. Pinto, and R. K. Smith, "Computation of Steady-State CMOS Latch-up Characteristics," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 7, No. 2, pp. 307–323, February 1988.

[103] A. Ochoa, W. Dawes, and D. B. Estreich, "Latch-up Control in CMOS Integrated Circuits," *IEEE Transactions on Nuclear Science*, Vol. 26, No. 6, pp. 5065–5068, December 1979.

[104] M. R. Pinto and R. W. Dutton, "Accurate Trigger Condition Analysis for CMOS Latch-up," *IEEE Electron Device Letters*, Vol. 6, No. 2, pp. 100–102, February 1985.

[105] S. Odanata, M. Wakabayashi, and T. Ohzone, "The Dynamics of Latch-up Turn-on Behaviour in Scaled CMOS," *IEEE Transactions on Electron Devices*, Vol. 32, No. 7, pp. 1334–1340, July 1985.

[106] R. E. Bank, W. M. Coughran, and K. R. Smith, "Transient Simulation of Silicon Devices and Circuits," *IEEE Transactions on Electron Devices*, Vol. 32, No. 10, pp. 1992–2007, October 1985.

[107] R. D. Rung and L. G. Walker, "A Retrograde P-well for Higher Density CMOS," *IEEE Transactions on Electron Devices*, Vol. ED-28, pp. 1115–1119, December 1981.

[108] W. R. Dawes, Jr. and D. F. Derbenwick, "Prevention of CMOS Latchup in MOS Integrated Circuits," *IEEE Transactions on Nuclear Science*, Vol. NS-23, pp. 2027–2030, December 1976.

[109] J. R. Adams and J. R. Sokel, "Neutron Irradiation for Prevention of Latchup in MOS Integrated Circuits," *IEEE Transactions on Nuclear Science*, Vol. NS-26, pp. 5069–5073, December 1979.

[110] M. Sugina, L. A. Akers, and M. E. Rebeschini, "CMOS Latch-up Elimination Using Schottky Barrier PMOS," *Proceedings of the IEEE International Electron Devices Meeting*, pp. 462–465, December 1982.

[111] E. Sangiori and S. Swirhun, "Trenched Schottky Barrier PMOS for Latchup Resistance," *IEEE Electron Devices Letters*, Vol. EDL-5, pp. 293–295, August 1984.

[112] A. G. Lewis, "Latchup Suppression in Fine-Dimension Shallow P-well CMOS Circuits," *IEEE Transactions on Electron Devices*, Vol. ED-31, pp. 1472–1481, October 1984.

[113] V. Adler and E. G. Friedman, "Repeater Design to Reduce Delay and Power in Resistive Interconnect," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, Vol. CAS II-45, No. 5, May 1998.

[114] V. Adler and E. G. Friedman, "Delay and Power Expressions for a CMOS Inverter Driving a Resistive-Capacitive Load," *Analog Integrated Circuits and Signal Processing*, Vol. 14, No. 1/2, pp. 29–39, September 1997.

[115] V. Adler and E. G. Friedman, "Repeater Insertion to Reduce Delay and Power in *RC* Tree Structures," *Proceedings of the Asilomar Conference on Signals, Systems, and Computers*, pp. 749–752, November 1997.

[116] R. M. Secareanu and E. G. Friedman, "A High Speed CMOS Buffer for Driving Large Capacitive Loads in Digital ASICs," *Proceedings of the IEEE ASIC Conference*, pp. 365–368, September 1998.

[117] R. M. Secareanu, V. Adler, and E. G. Friedman, "Exploiting Hysteresis in a CMOS Buffer," *Proceedings of the IEEE International Conference on Electronics, Circuits, and Systems*, pp. 205–208, September 1999.

[118] R. M. Secareanu, E. G. Friedman, J. Becerra, and S. Warner, "A Universal CMOS Voltage Interface Circuit," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 1.242–1.245, May 1999.

[119] R. M. Secareanu, S. Warner, S. Seabridge, C. Burke, T. E. Watrobski, C. Morton, W. Staub, T. Tellier, and E. G. Friedman, "Physical Design for Noise Immunity of Digital Circuits in a Mixed-Signal Smart Power System," *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 2000.

[120] R. M. Secareanu, S. Warner, S. Seabridge, C. Burke, T. E. Watrobski, C. Morton, W. Staub, T. Tellier, and E. G. Friedman, "Substrate Noise Distribution and Placement of Substrate Contacts to Alleviate Substrate Noise in Epi and Non-Epi Technologies," *Proceedings of the IEEE 23rd Annual EDS/CAS Activities in Western New York Conference*, pp. 15–16, November 1999.

[121] R. M. Secareanu, I. S. Kourtev, J. Becerra, T. E. Watrobski, C. Morton, W. Staub, T. Tellier, and E. G. Friedman, "The Behavior of Digital Circuits under Substrate Noise in a Mixed-Signal Smart-Power Environment," *Proceedings of the IEEE International Symposium on Power Semiconductor Devices and ICs*, pp. 253–256, May 1999.

[122] X. Aragones and A. Rubio, "Experimental Comparison of Substrate Noise Coupling Using Different Wafer Types," *IEEE Journal of Solid-State Circuits*, Vol. 34, No. 10, pp. 1405–1409, October 1999.

[123] R. M. Secareanu, I. S. Kourtev, J. Becerra, T. E. Watrobski, C. Morton, W. Staub, T. Tellier, and E. G. Friedman, "Noise Immunity of Digital Circuits in Mixed-Signal Smart Power Systems," *Proceedings of the IEEE Great Lakes Symposium on VLSI*, pp. 314–317, February 1999.

[124] R. M. Secareanu and E. G. Friedman, "A Differential High-Speed Digital CMOS Buffer with Hysteresis for Improved Noise Immunity," *Proceedings of the IEEE ASIC Conference*, September 2000.

[125] R. M. Secareanu and E. G. Friedman, "Transparent Repeaters," *Proceedings of the IEEE Great Lakes Symposium on VLSI*, pp. 63–66, March 2000.

Appendix A

Representative layouts of the NMOS test circuits

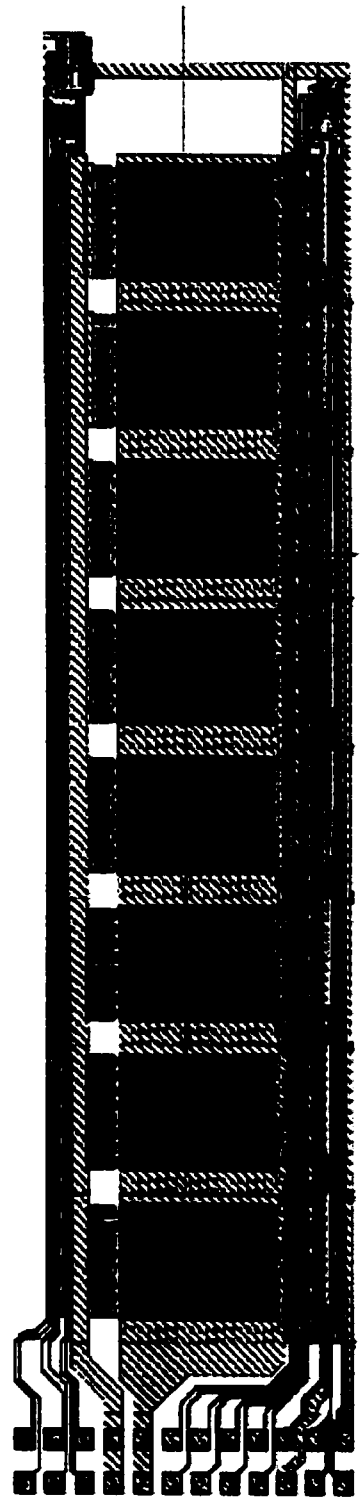


Figure A.1: The layout of a representative "upper group" circuit

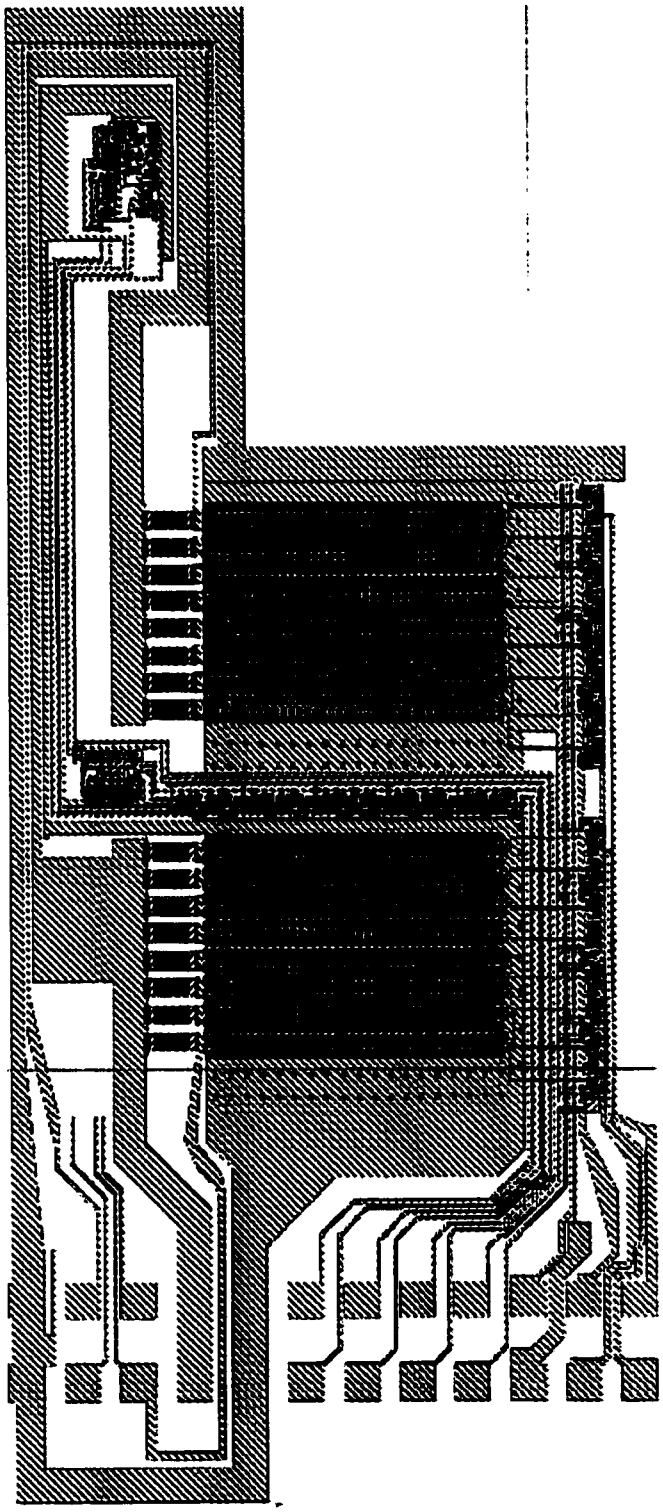


Figure A.2: The layout of a representative "middle group" circuit

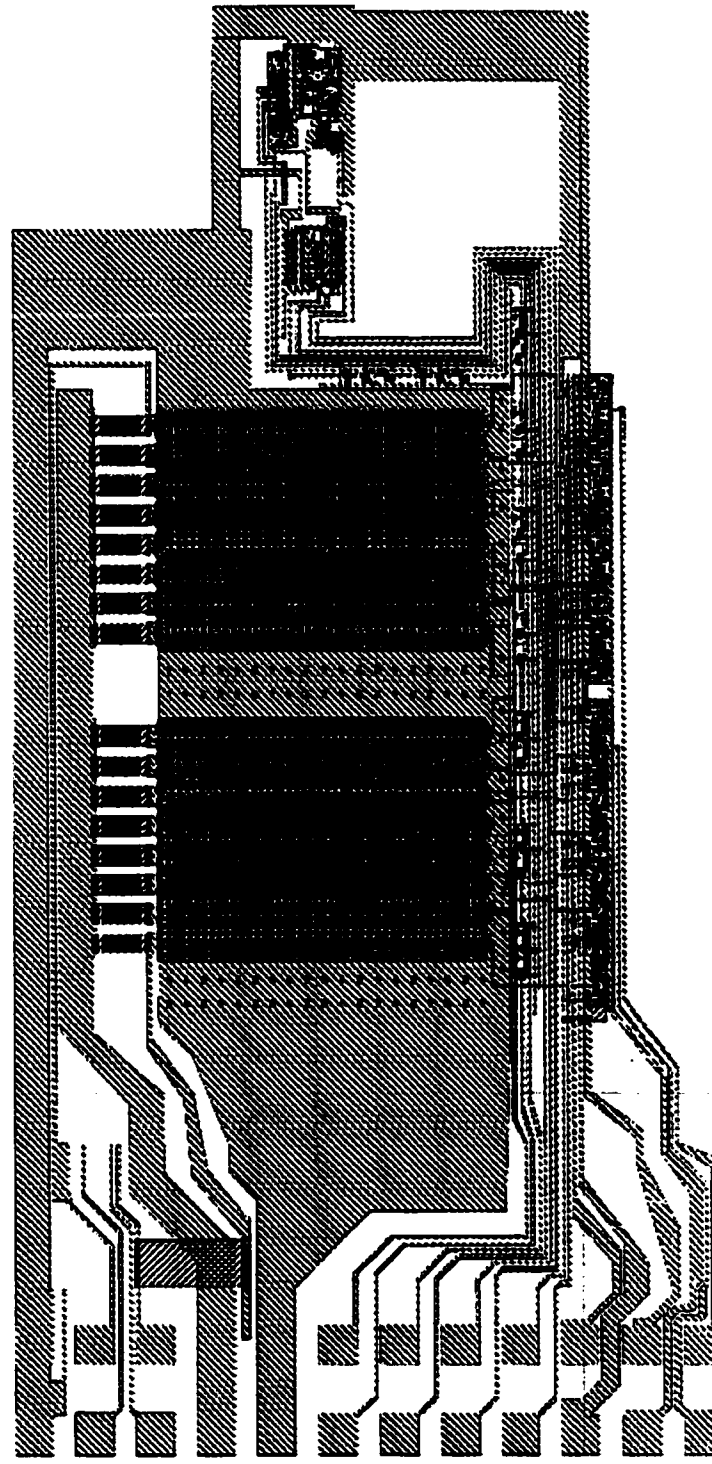


Figure A.3: The layout of a representative "lower group" circuit

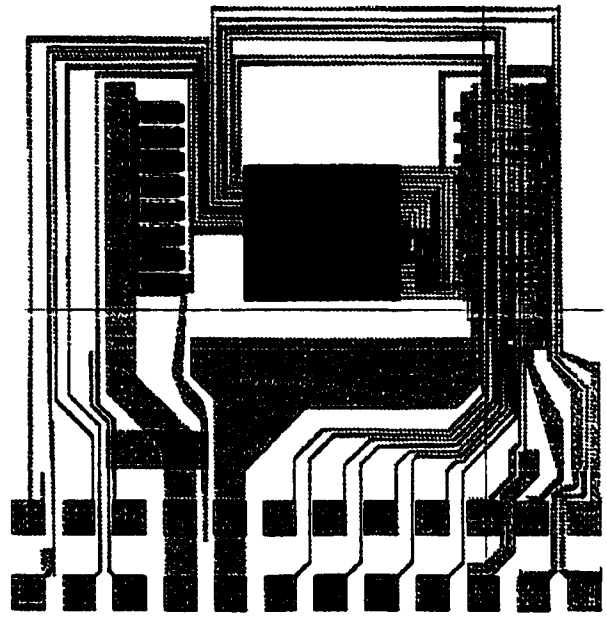


Figure A.4: The layout of a representative "group 4" circuit with only 1 driver

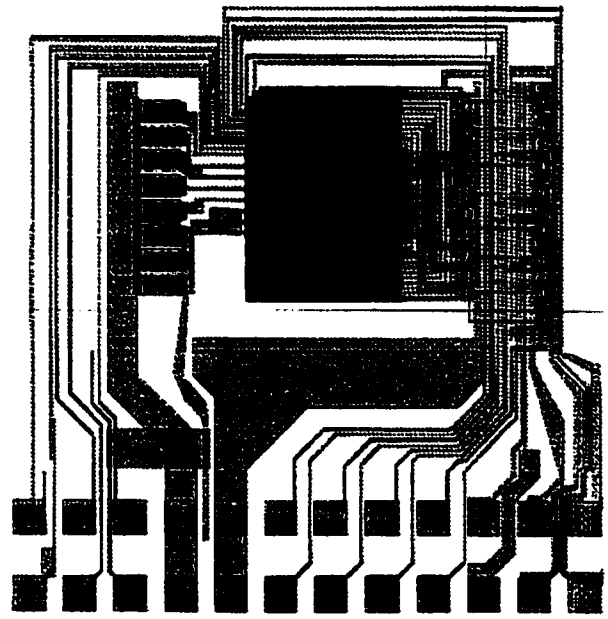


Figure A.5: The layout of a representative "group 4" circuit with 8 drivers

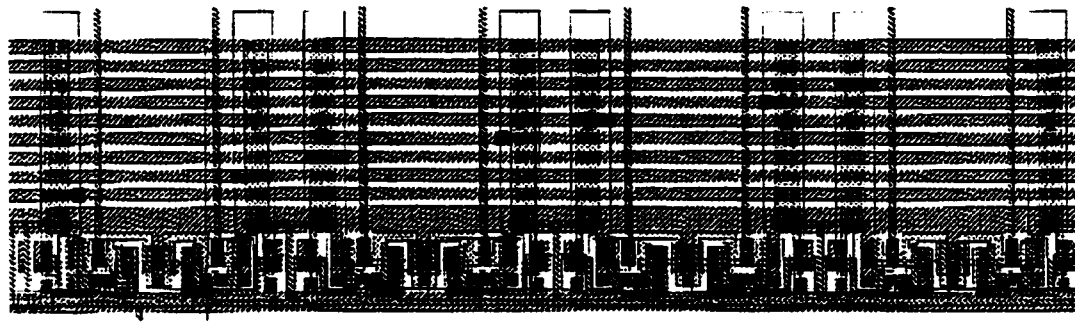


Figure A.6: The layout of 8 predrivers

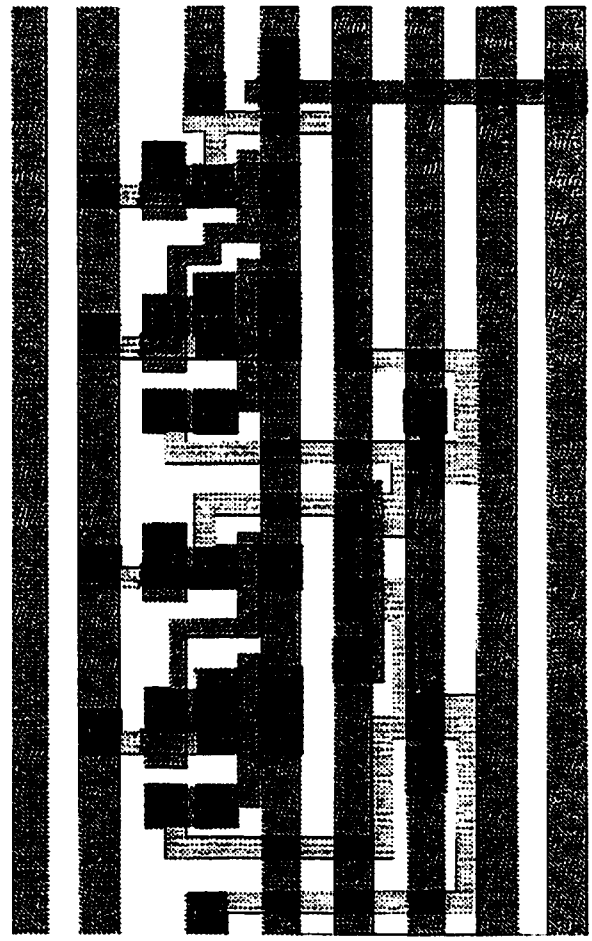


Figure A.7: The layout of a static latch

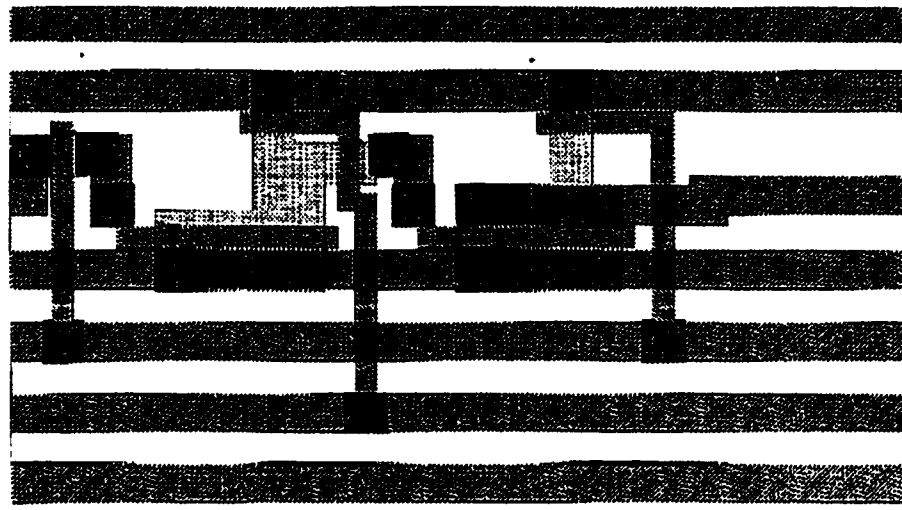


Figure A.8: The layout of a dynamic latch

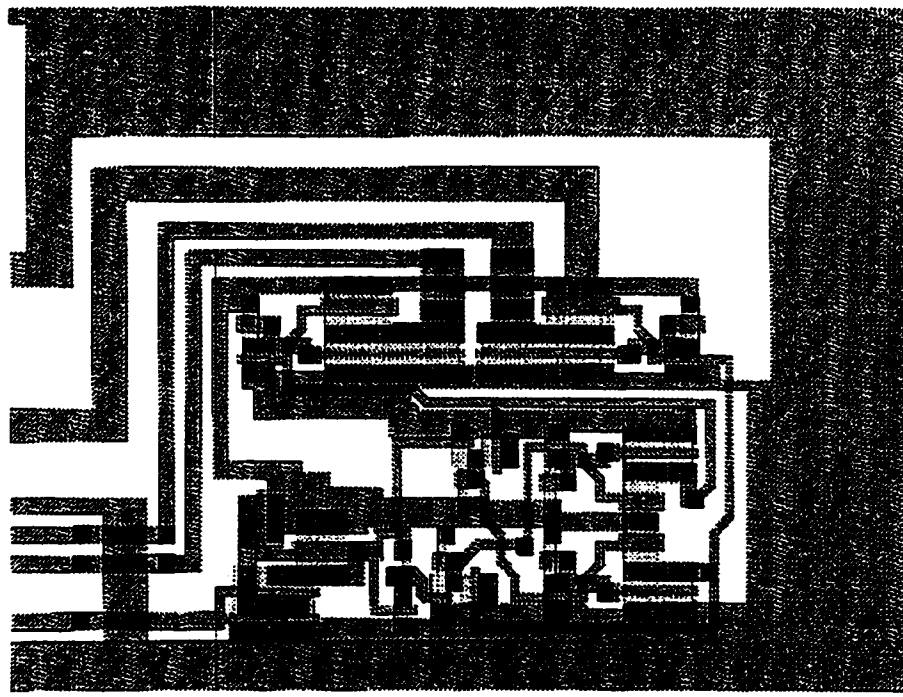


Figure A.9: The layout of the non-overlapping clock generator

Appendix B

Description, photographs, and relevant specifications of the test equipment

Primary equipment:

- Electroglas 2001X Automatic Wafer Probing System
- HP 3488A Switch/Control Unit
- HP 16500A Programmable Logic Analysis System
- HP 6624A System DC Power Supply (two units)
- HP 3457A Multimeter (two units)
- Signatone manual prober

Secondary equipment:

- Tektronix TDS 744A Color Four Channel Digitizing Oscilloscope
- Sony/Tektronix 370A Programmable Curve Tracer
- HP4156A Precision Semiconductor Parameter Analyzer

- Keithley 560 CV Analyzer

HP programmable pattern generator relevant specifications:

- Minimum period: 20 ns (+/-2%), 50 ns for strobes
- Risetime/falltime: 2.5 ns typ.
- Channel to channel skew: $\leq$ 5 ns
- Number of independent channels: 12 + 3 strobes

HP programmable logic analysis system relevant specifications:

- Minimum signal swing: 600 mV peak to peak
- Threshold accuracy: +/-300 mV
- Minimum detectable glitch: 5 ns
- Maximum input voltage: +/-40 V peak
- Sampling time stored: between 10.24 μs and 5000 s
- Minimum sample period: 10 ns
- Number of samples per acquisition per channel: 512
- Number of traces: 4. Up to 24 waveforms can be displayed, if overlapped
- Channel to channel skew: max. 4 ns

Figure B.1: A general view of the main test equipment_

Figure B.2: Another general view of the main test equipment

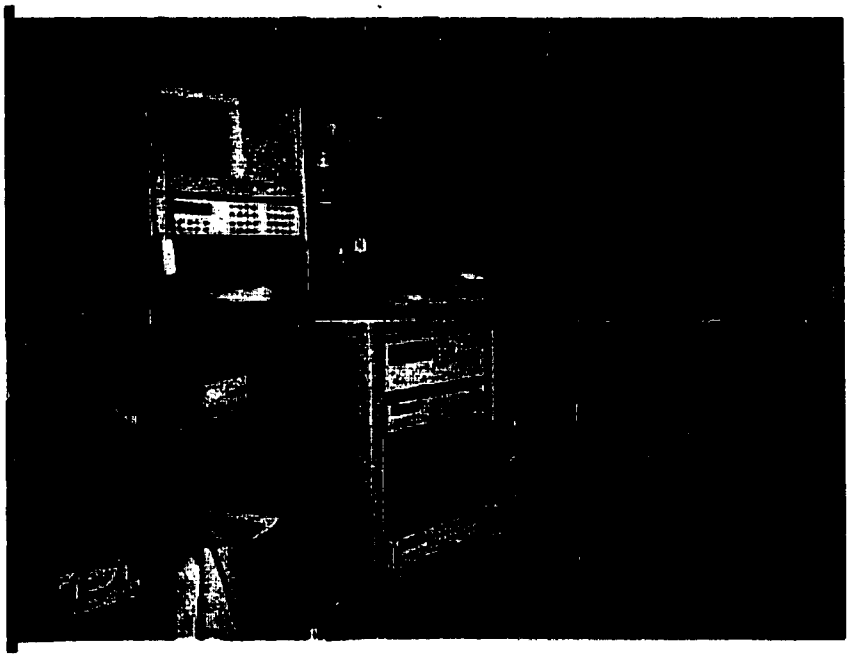


Figure B.3: A closer view of the main test equipment

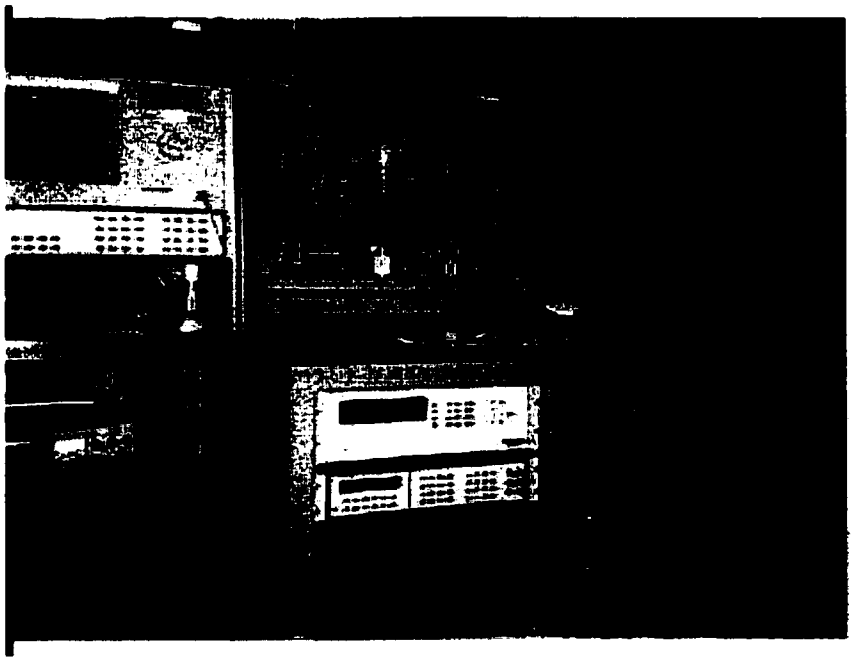


Figure B.4: Another closer view of the main test equipment

Figure B.5: A different closer view of the main test equipment

Figure B.6: Another closer view of the main test equipment

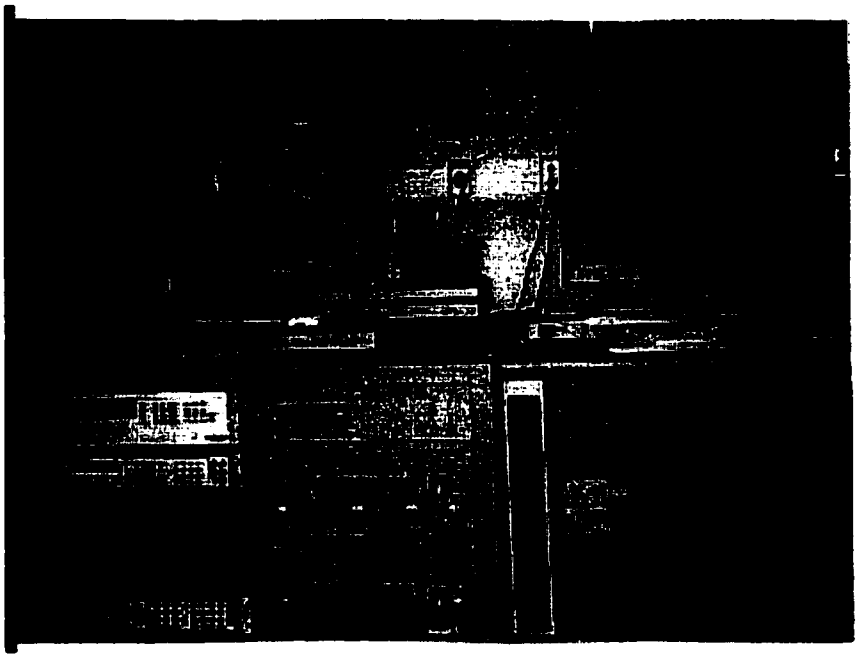


Figure B.7: A frontal view of the main test equipment-

Figure B.8: The clean loading area

Figure B.9: The manual prober with the precision semiconductor analyzer

Figure B.10: The manual prober with the precision semiconductor analyzer

Figure B.11: The manual prober with the precision semiconductor analyzer

Figure B.12: The CV analyzer and Sony/Tektronix curve tracer

Appendix C

Simulation waveforms

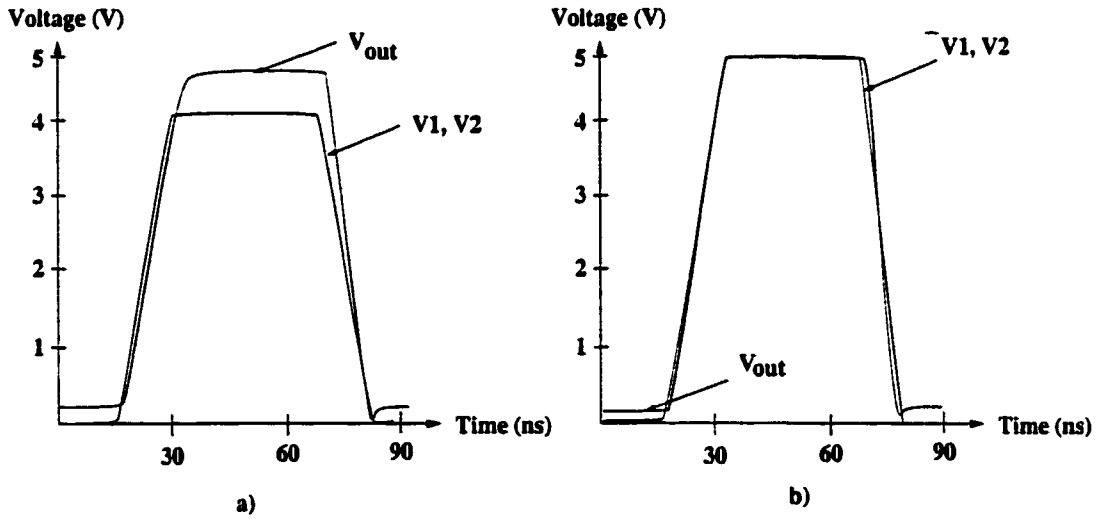


Figure C.1: a) V1=V2=4 volts, V1 and V2 are in-phase, C_L=10 fF, k_E/k_D=4, and V_{in}=5 volts b) V1=V2=5 volts, V1 and V2 are in-phase, C_L=10 fF, k_E/k_D=4, and V_{in}=5 volts

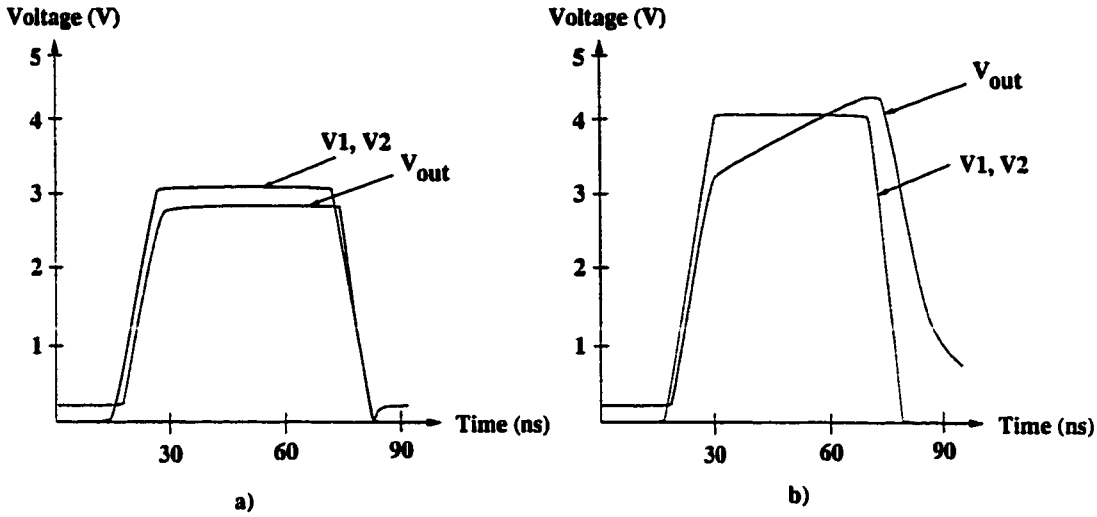


Figure C.2: a) V1=V2=3 volts, V1 and V2 are in-phase, C_L=10 fF, k_E/k_D=4, and V_{in}=5 volts b) V1=V2=4 volts, V1 and V2 are in-phase, C_L=1 pF, k_E/k_D=4, and V_{in}=5 volts

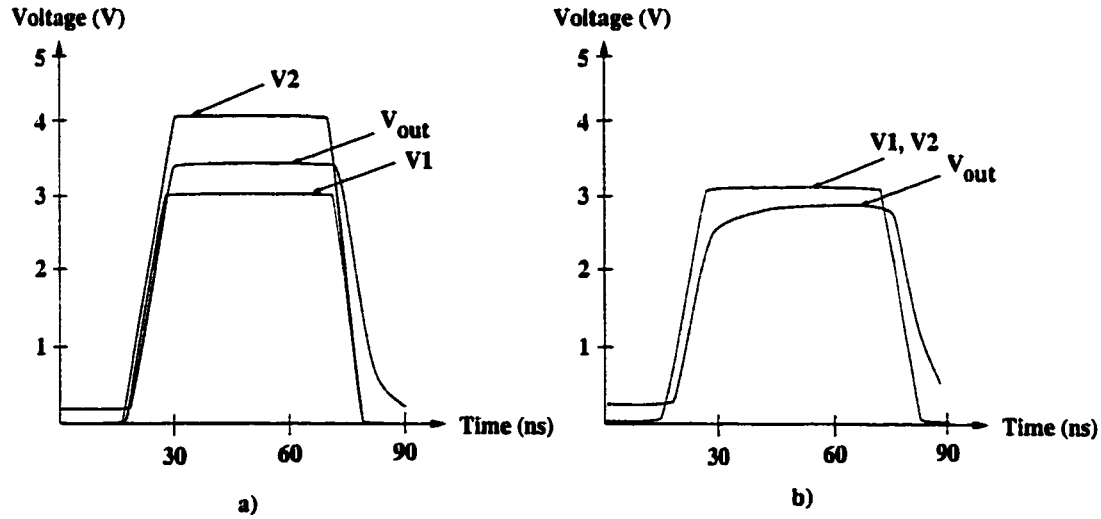


Figure C.3: a) V1=3 volts, V2=4 volts, V1 and V2 are in-phase, C_L=1 pF, k_E/k_D=4, and V_{in}=5 volts b) V1=V2=3 volts, V1 and V2 are in-phase, C_L=1 pF, k_E/k_D=4, and V_{in}=5 volts

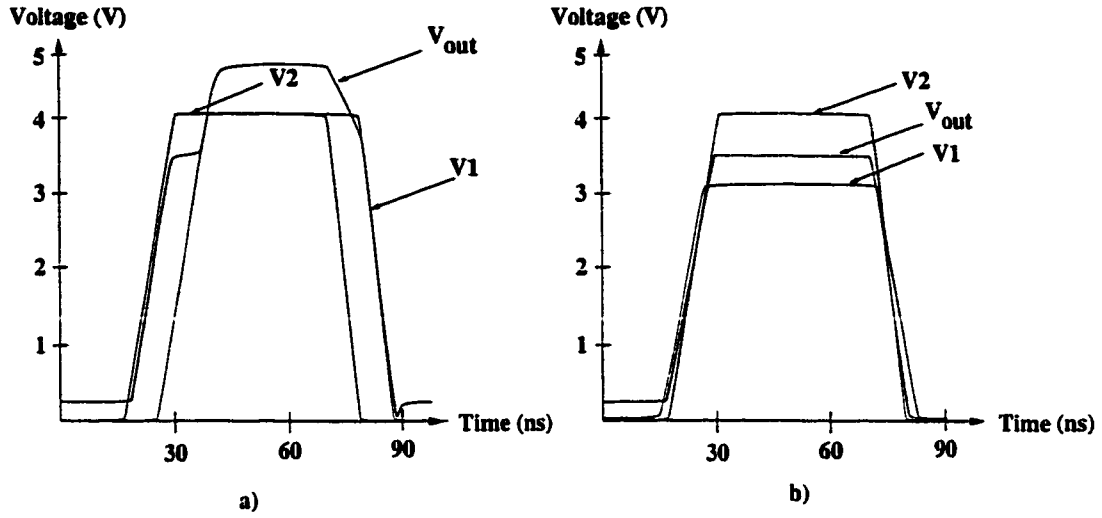


Figure C.4: a) V1=V2=4 volts, V1 delayed by 10 ns as compared to V2, C_L=10 fF, k_E/k_D=4, and V_{in}=5 volts b) V1=3 volts, V2=4 volts, V1 and V2 are in-phase, C_L=10 fF, k_E/k_D=4, and V_{in}=5 volts

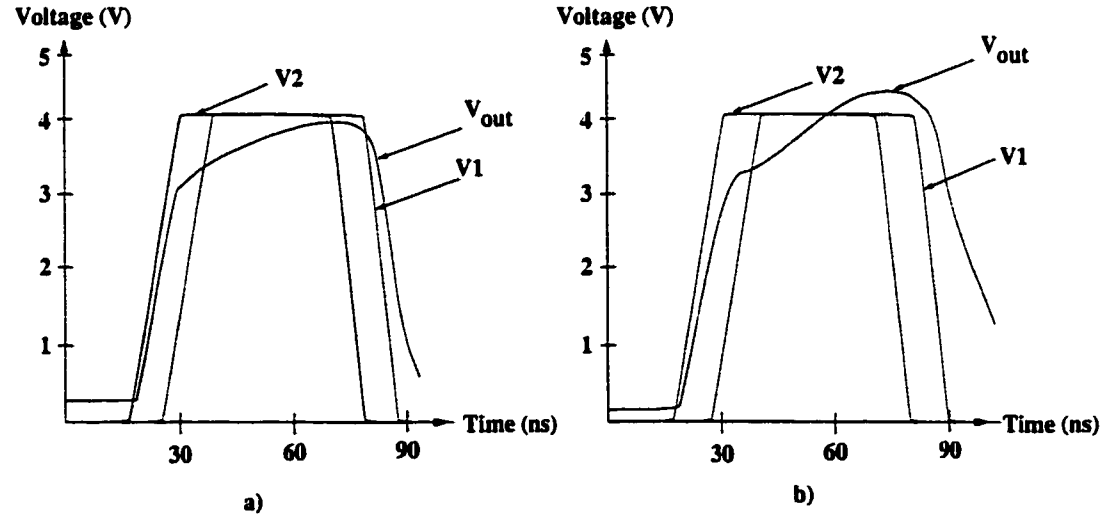


Figure C.5: a) V1=V2=4 volts, V1 delayed by 10 ns as compared to V2, C_L=1 pF, k_E/k_D=8, and V_{in}=5 volts b) V1=V2=4 volts, V1 delayed by 10 ns as compared to V2, C_L=1 pF, k_E/k_D=4, and V_{in}=5 volts

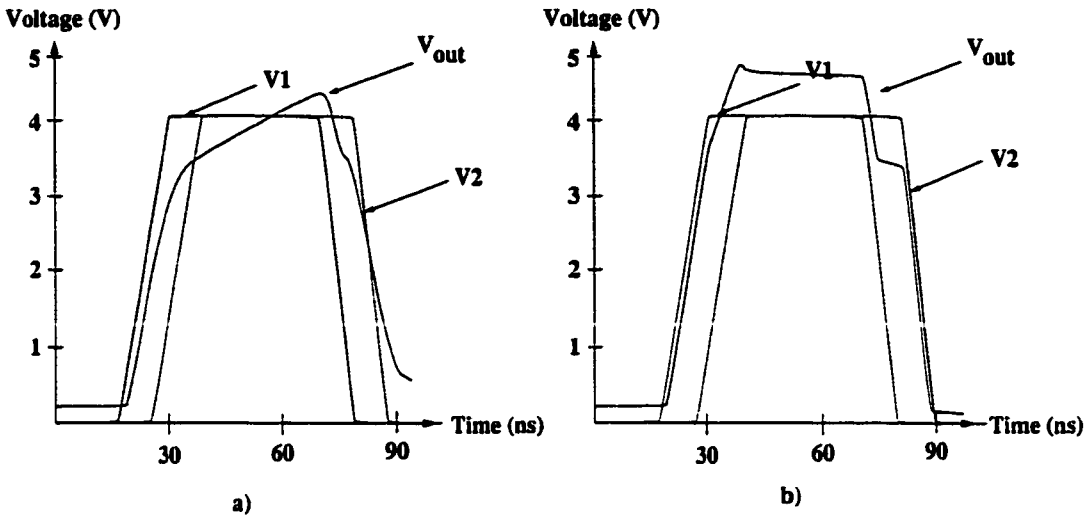


Figure C.6: a) V1=V2=4 volts, V2 delayed by 10 ns as compared to V1, C_L=1 pF, k_E/k_D=4, and V_{in}=5 volts b) V1=V2=4 volts, V2 delayed by 10 ns as compared to V1, C_L=10 fF, k_E/k_D=4, and V_{in}=5 volts

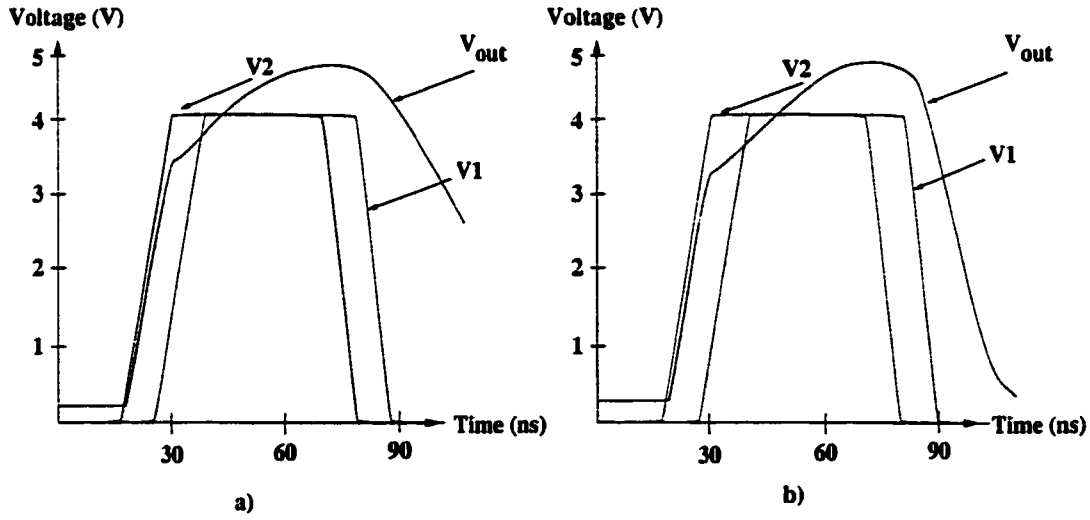


Figure C.7: a) V1=V2=4 volts, V1 delayed by 10 ns as compared to V2, C_L=1 pF, k_E/k_D=4, and V_{in}=3 volts b) V1=V2=4 volts, V1 delayed by 10 ns as compared to V2, C_L=1 pF, k_E/k_D=4, and V_{in}=4 volts

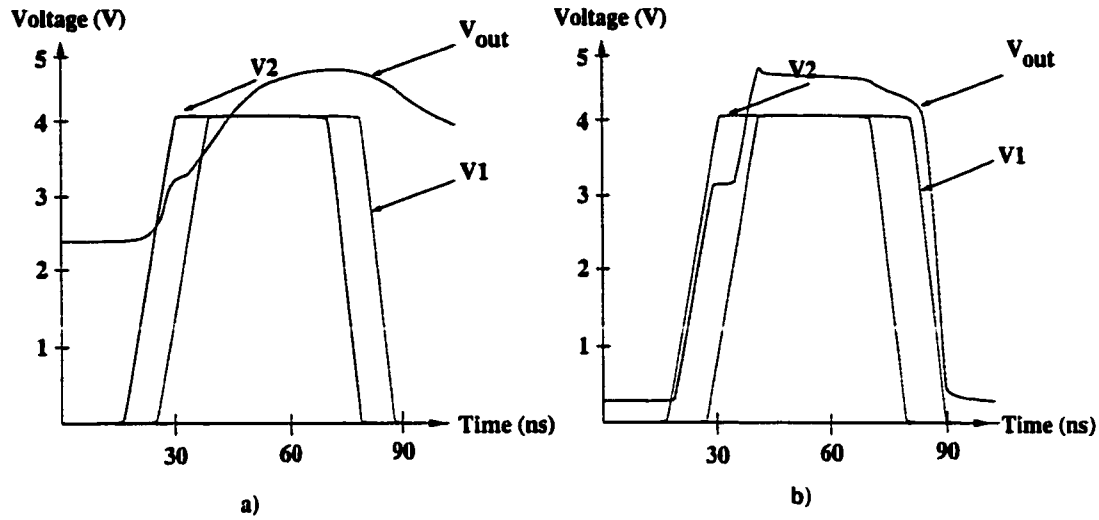


Figure C.8: a) V1=V2=4 volts, V1 delayed by 10 ns as compared to V2, C_L=1 pF, k_E/k_D=4, and V_{in}=2 volts b) V1=V2=4 volts, V1 delayed by 10 ns as compared to V2, C_L=10 fF, k_E/k_D=4, and V_{in}=3 volts

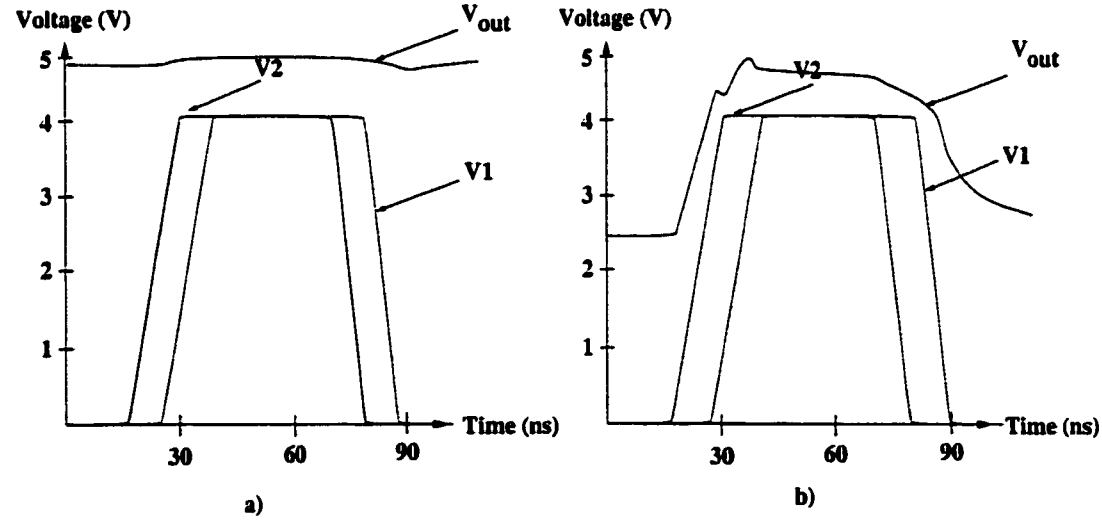


Figure C.9: a) V1=V2=4 volts, V1 delayed by 10 ns as compared to V2, C_L=1 pF, k_E/k_D=4, and V_{in}=1 volt b) V1=V2=4 volts, V1 delayed by 10 ns as compared to V2, C_L=10 fF, k_E/k_D=4, and V_{in}=2 volts

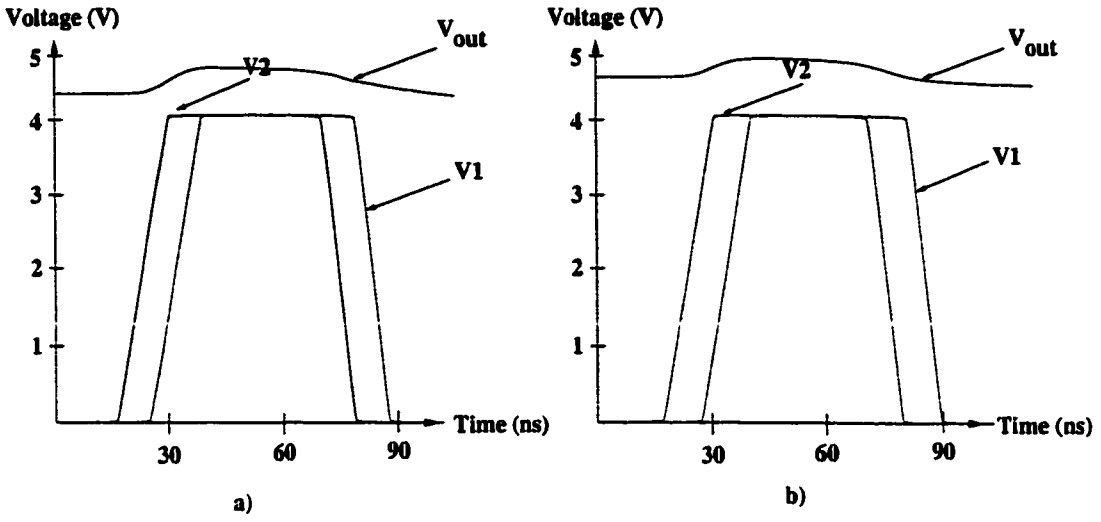


Figure C.10: a) V1=V2=4 volts, V1 delayed by 10 ns as compared to V2, C_L=1 pF, k_E/k_D=8, and V_{in}=1.4 volts b) V1=V2=4 volts, V1 delayed by 10 ns as compared to V2, C_L=1 pF, k_E/k_D=4, and V_{in}=1.4 volts

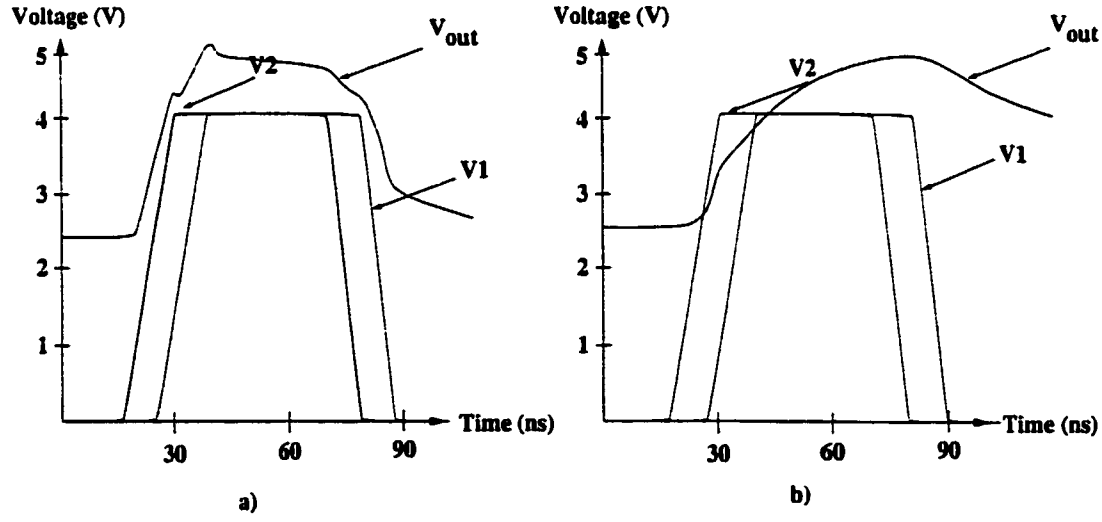


Figure C.11: a) V1=V2=4 volts, V1 delayed by 10 ns as compared to V2, C_L=10 fF, k_E/k_D=8, and V_{in}=1.7 volts b) V1=V2=4 volts, V1 delayed by 10 ns as compared to V2, C_L=1 pF, k_E/k_D=8, and V_{in}=1.7 volts

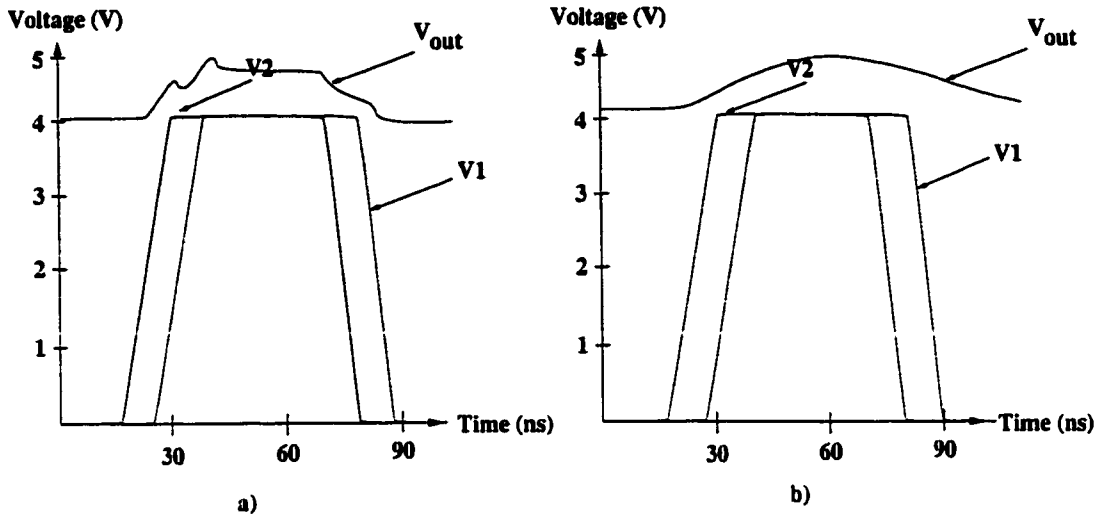


Figure C.12: a) V1=V2=4 volts, V1 delayed by 10 ns as compared to V2, C_L=10 fF, k_E/k_D=4, and V_{in}=1.7 volts b) V1=V2=4 volts, V1 delayed by 10 ns as compared to V2, C_L=1 pF, k_E/k_D=4, and V_{in}=1.7 volts

Appendix D

Publications

1. R. M. Secareanu, Scott Warner, Scott Seabridge, Cathie Burke, T. E. Watrobski, C. Morton, W. Staub, T. Tellier, and E. G. Friedman, "Physical Design to Improve the Noise Immunity of Digital Circuits in a Mixed-Signal Smart-Power System," *Proceedings of the IEEE International Symposium on Circuits and Systems,* May 2000.

2. R. M. Secareanu and E. G. Friedman, "Transparent Repeaters," *Proceedings of the IEEE Great Lakes Symposium on VLSI,* pp. 63–66, March 2000.

3. R. M. Secareanu, Scott Warner, Scott Seabridge, Cathie Burke, T. E. Watrobski, C. Morton, W. Staub, T. Tellier, and E. G. Friedman, "Substrate Noise Distribution and Placement of Substrate Contacts to Alleviate Substrate Noise in Epi and Non-Epi Technologies," *Proceedings of the IEEE 23rd Annual EDS/CAS Activities in Western New York Conference,* pp. 15–16, November 1999.

4. R. M. Secareanu, Victor Adler, and E. G. Friedman "Exploiting Hysteresis in a CMOS Buffer," *Proceedings of the IEEE International Conference on Electronics, Circuits, and Systems,* pp. 205–208, September 1999.

5. R. M. Secareanu and E. G. Friedman, "A High Precision CMOS Current-Mirror Divider," *Proceedings of the IEEE International Symposium of Circuits and Systems,* pp. 2.314–2.317, May 1999.

6. R. M. Secareanu, E. G. Friedman, J. Becerra, and Scott Warner, "A Universal CMOS Voltage Interface Circuit," *Proceedings of the IEEE International Symposium on Circuits and Systems,* pp. 1.242–1.245, May 1999.

7. R. M. Secareanu, I. S. Kourtev, J. Becerra, T. E. Watrobski, C. Morton, W. Staub, T. Tellier, and E. G. Friedman, "The Behavior of Digital Circuits under Substrate Noise in a Mixed-Signal Smart-Power Environment,"

Proceedings of the IEEE International Symposium on Power Semiconductor Devices and ICs, pp. 253–256, May 1999.

8. R. M. Secareanu, I. S. Kourtev, J. Becerra, T. E. Watrobski, C. Morton, W. Staub, T. Tellier, and E. G. Friedman, "Noise Immunity of Digital Circuits in Mixed-Signal Smart Power Systems," *Proceedings of the IEEE Great Lakes Symposium on VLSI*, pp. 314–317, February 1999.

9. R. M. Secareanu and E. G. Friedman, "A High Speed CMOS Buffer for Driving Large Capacitive Loads in Digital ASICs," *Proceedings of the IEEE International ASIC Conference*, pp. 365–368, September 1998.

10. R. M. Secareanu and E. G. Friedman, "A CMOS Current Mirror/Divider for High Precision Applications," *Proceedings of the IEEE 21st Annual EDS/CAS Activities in Western New York Conference*, pp. 11, November 1997.

11. R. M. Secareanu, S. Nan, M. Serbanescu, and P. Cazimirovitz, "Electrical Characterization of ZnO Based Varistors" *Proceedings of the IEEE Romanian Annual International Semiconductor Conference "CAS-1994,"* October 1994.

Submissions

1. R. M. Secareanu, Scott Warner, Scott Seabridge, Cathie Burke, T. E. Watrobski, C. Morton, W. Staub, T. Tellier, and E. G. Friedman, "A Comparative Study of the Behavior of NMOS and CMOS Digital Circuits under Substrate Noise," *Proceedings of the IEEE ASIC Conference*, September 2000.

2. R. M. Secareanu and E. G. Friedman, "A Differential High-Speed Digital CMOS Buffer with Hysteresis for Improved Noise Immunity," *Proceedings of the IEEE ASIC Conference*, September 2000.

3. R. M. Secareanu, Scott Warner, Scott Seabridge, Cathie Burke, T. E. Watrobski, C. Morton, W. Staub, T. Tellier, and E. G. Friedman, "Placement of Substrate Contacts to Minimize Substrate Noise in Mixed-Signal Integrated Circuits," *Analog Integrated Circuits and Signal Processing Journal.*

4. R. M. Secareanu, Scott Warner, Scott Seabridge, Cathie Burke, T. E. Watrobski, C. Morton, W. Staub, T. Tellier, and E. G. Friedman, "Placement of Substrate Contacts to Alleviate Substrate Noise in Epi and Non-Epi Technologies," *Proceedings of the IEEE Midwest Symposium on Circuits and Systems*, August 2000.

5. R. M. Secareanu and E. G. Friedman, "Low Power Digital CMOS Buffer Systems for Driving Highly Capacitive Interconnect Lines," *Proceedings of the IEEE Midwest Symposium on Circuits and Systems,* August 2000.

Patent applications

1. R. M. Secareanu and E. G. Friedman, "Current Mirror and/or Divider Circuits," *Application number UR-0155CV, US Patent Application Serial No.: 09/312,744,* patent pending.

2. R. M. Secareanu and E. G. Friedman, "Digital Buffer Circuits," *Application number UR-0156CV, US Patent Application Serial No.: 09/318,421,* patent pending.

3. R. M. Secareanu and E. G. Friedman, "Digital CMOS Voltage Interface Circuits", *Application number UR-0163P, US Provisional Patent Application Serial No.: 60/134,738.*