Performance Characteristics of 14 nm Near Threshold MCML Circuits

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***Abstract*—Near threshold circuits (NTC) are an attractive and promising technology that provides significant power savings with some delay penalty. The feasibility of NTC technology with MOS Current Mode Logic (MCML) based on a 14 nm FinFET process node is examined in this paper. A 32 bit Kogge Stone adder is chosen as a demonstration vehicle for simulation and feasibility analysis. MCML yields enhanced power efficiency when operated with a 100% activity factor above 1 GHz as compared to CMOS. Standard CMOS does not achieve frequencies above 9 GHz without a dramatic increase in power consumption. MCML is most efficient beyond 9 GHz over a wide range of activity factors. MCML also exhibits significantly lower noise levels as compared to standard CMOS. The results of the analysis demonstrate that pairing NTC and MCML is efficient when operating at high frequencies and activity factors.**

I. Introduction

Near threshold circuits (NTC) consume an order of magnitude less power than circuits operating under nominal voltages while not suffering from the significant delay penalty found in subthreshold circuits. NTC has therefore become an attractive methodology for sub-30 nm CMOS circuits [1]. In this work, NTC [2] is paired with MOS Current Mode Logic (MCML) to compensate for the vulnerable aspects of each technology.

MCML is a differential circuit topology driven by a constant tail current. The lack of switching transients contributes to a low noise environment as compared to standard CMOS. The low noise environment is particularly beneficial for NTC due to the low voltages.

The paper is structured as follows. In Section II, MCML is introduced. The simulation environment and results are summarized in Section III. Some conclusions are provided in Section IV.

II. MOS current mode logic

MCML circuit technology is reviewed in the following sections.

A. Power efficiency of MCML

The power consumed by an MCML gate is

$$P_{MCML} = I_{BIAS} \times V_{DD}. \quad (1)$$

Note that the power consumed by an MCML gate does not depend on the operating frequency. An MCML gate consumes constant current (and power) from the power supply network. This behavior is in contrast to the CV^2f power dissipated by conventional CMOS, where the power consumed by a static CMOS gate exhibits a linear relationship with the operating frequency. MCML is therefore more power efficient at high frequencies as compared to static CMOS. MCML circuits operating near the threshold voltage are introduced in this paper to reduce the frequency at which MCML dissipates less power than static CMOS from between 5 to 10 GHz to around 1 GHz.

B. Low noise environment of MCML

CMOS circuits suffer from simultaneous switching noise (SSN), which accounts for a major portion of the total on-chip noise. In contrast, the constant current of MCML significantly lessens on-chip SSN. The low noise of MCML is particularly relevant when combined with NTC due to the exponential sensitivity of NTC circuits to noise. In this work, the simultaneous switching noise of a 32 bit CMOS adder is compared to the SSN noise generated by a 32 bit MCML adder.

C. Logic circuits

Basic MCML gates share certain standard characteristics. Only one gate, therefore, needs to be optimized. NAND, AND, NOR, OR, and XOR gates are considered in this work. The first four gates are based on the circuit shown in Figure 2. The XOR gate is shown in Figure 3. Note that the MCML XOR gate is significantly smaller than a static CMOS XOR gate.

III. Simulation results

The simulations are based on 14 nm low power (LP) FinFET predictive technology models [3]. A standard threshold voltage of $V_{th} = 350$ mV is assumed. The supply voltage is set to 400 mV to operate near the threshold voltage with an MCML input/output voltage swing of 100 mV.

A 32 bit Kogge Stone adder has been evaluated in both standard CMOS and MCML. The following subsections present a summary of the power and noise characteristics.

1) Power: The power characteristics shown in Figure 1 is for a 32 bit Kogge Stone adder. The maximum frequency corresponding to each power consumption value is the inverse of the circuit delay. The power dissipated by an MCML circuit is therefore not constant since the power is a function of the maximum frequency (as opposed to simply the frequency).

There are two primary circuit behaviors of interest, as illustrated in Figure 1. At 1 GHz, the power consumed by MCML is less than CMOS at a 100% activity factor. At

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9 GHz, the CMOS circuit reaches the maximum operating frequency at a nominal supply voltage with minimum sized gates. To further lower the delay (to increase the frequency), the CMOS gates need to be larger, exponentially increasing the power dissipation. At 9 GHz, the MCML circuit is more power efficient than CMOS at 20% and 10% activity factors. Unlike standard CMOS, MCML is capable of operating at frequencies well beyond 9 Ghz (in 14 nm technology).

2) Noise: To demonstrate the low noise of MCML technology, the maximum induced noise in a power network due to switching activity is listed in Table I. The SSN in MCML circuits is, on average, an order of magnitude lower than in static CMOS.

IV. Conclusions

The combination of NTC and MCML exploits the advantages of each technology. Unlike standard CMOS, MCML circuits operating near the threshold voltage perform better at higher frequencies and higher activity factors. Unlike standard CMOS, 14 nm MCML circuits operating near the threshold voltage can achieve high operating frequencies and power efficiencies at frequencies above 9 GHz.

References

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TABLE I
Comparison of noise in CMOS and MCML circuits

Power network parasitic impedances			Noise induced on power network [mV]		
			MCML	CMOS	
PN Res [ohm]	PN Cap [fF]	PN Ind [nH]	Absolute value	Absolute value	Ratio
2	50	1	0.56	6.27	11
2	50	2	0.94	9.92	11
2	50	4	0.70	14.64	21
2	100	1	1.28	6.19	5
2	100	2	0.95	9.14	10
2	100	4	1.81	13.51	7
2	200	1	0.55	6.21	11
2	200	2	0.93	9.96	11
2	200	4	0.66	12.56	19
5	50	1	1.32	6.50	5
5	50	2	0.84	9.75	12
5	50	4	1.71	14.63	9
5	100	1	0.51	6.52	13
5	100	2	0.93	9.29	10
5	100	4	0.72	13.24	18
5	200	1	1.25	6.60	5
5	200	2	0.83	10.02	12
5	200	4	1.61	12.16	8

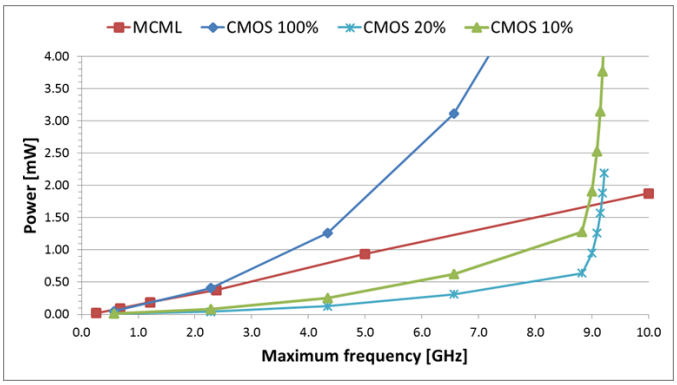

Fig. 1. Power vs maximum frequency of MCML and standard CMOS for activity factors of 100%, 20%, and 10%

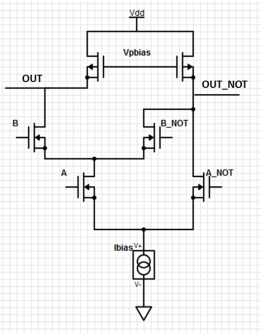

Fig. 2. MCML universal gate

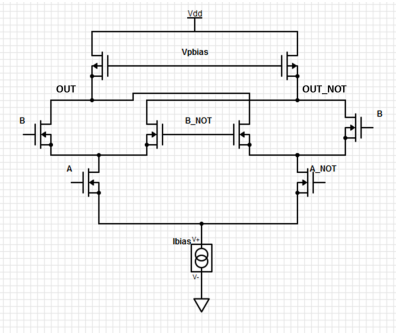

Fig. 3. MCML XOR gate

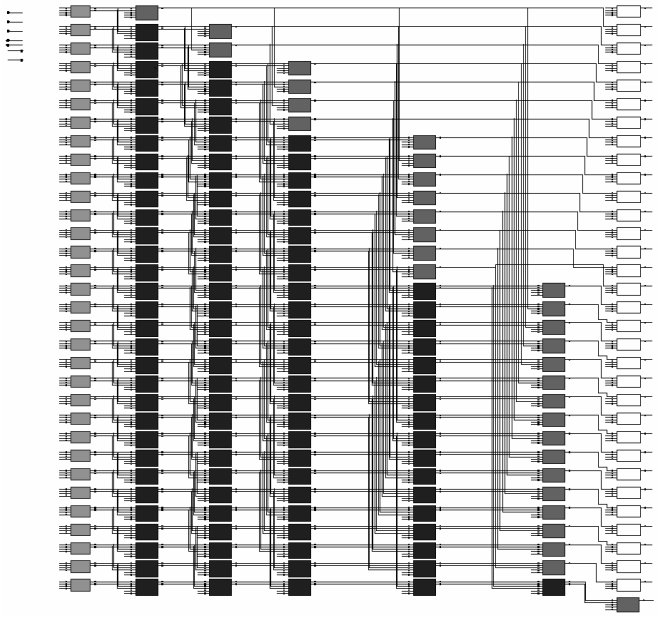

Fig. 4. Schematic of 32 bit Kogge Stone adder. Light grey represents the bit propagate and generate cells, grey represents the group generate cells, black represents the group generate and propagate cells, and white represents the XOR gates.