Global Interconnects in VLSI Complexity Single Flux Quantum Systems

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ABSTRACT

On-chip signal routing has become an issue of growing importance in modern VLSI complexity single flux quantum (SFQ) systems. In this paper, different routing methods for these systems are described. The routing methods include either passive transmission lines (PTLs) or Josephson transmission lines (JTLs) as interconnects. Driving multiple SFQ gates is also a challenging issue in automated layout and clock tree synthesis (CTS) due to the limited fanout of SFQ gates. To support multiple fanout, splitters are used to distribute multiple SFQ pulses. These splitters require significant area, delay, and power. In this paper, several area and power efficient splitters are proposed for large scale SFQ integrated circuits. A primary issue within a long SFQ interconnect is resonance effects due to the imperfect match between the PTLs and Josephson junctions. A repeater insertion methodology for long interconnect to reduce and manage these resonance effects is also described. Summarizing, guidelines and tradeoffs appropriate for automated layout and synthesis are described for driving long and short interconnect in VLSI complexity SFQ systems.

KEYWORDS

Single flux quantum, superconductive integrated circuits, superconductive digital electronics.

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1 INTRODUCTION

Superconductive single flux quantum (SFQ) technology is one of the most promising beyond-CMOS technologies for ultra-high speed and ultra-low power digital applications [1]. Significant development in the design and manufacture of superconductive electronics for prospective exascale computing systems has led to device densities exceeding 600,000 junctions/cm^2 and circuit speeds approaching 770 GHz [2–5]. Recent progress in the fabrication of SFQ circuits emphasizes the need for advanced EDA tools targeting SFQ design and analysis. While certain principles and techniques commonly used in CMOS are applicable to SFQ technology, several notable differences between these digital circuit families exist. Novel algorithms, methodologies, and tools are therefore required to enhance the design and analysis of VLSI complexity SFQ circuits and systems.

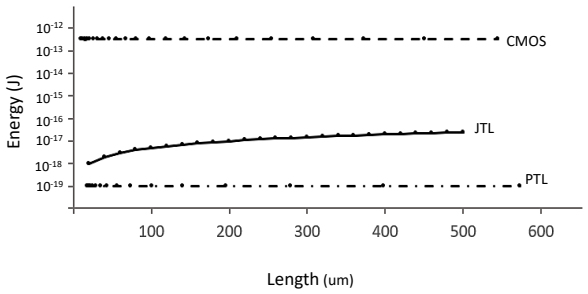

Figure 1: Energy vs. length of CMOS (dash line), JTL (solid line), and PTL with one Josephson junction in the receiver (dash-dotted line) [10–14].

An important characteristic of SFQ circuits is absolute zero DC resistance interconnects [6]. SFQ circuits utilize two distinct types of interconnect - active Josephson transmission lines (JTL) and passive transmission lines (PTL), composed of a microstrip or stripline with a matched driver and receiver [7–9]. A comparison of the energy dissipated by interconnects for CMOS and SFQ is shown in Fig. 1. The energy of a 16 nm CMOS interconnect technology is evaluated with an RLC model [10]. The energy of a chain of JTLs increases linearly with distance between gates. The PTL line exhibits a constant energy independent of length. The energy of the CMOS interconnect is approximately six orders of magnitude greater than the energy dissipated by a passive superconductive interconnect [11–14].

The physical design and layout of SFQ circuits play an important role in the timing characteristics of high speed VLSI complexity SFQ systems. The layout of these large scale SFQ circuits requires automated design methodologies. Recent progress in automated layout tools provides effective techniques for clock tree synthesis, and placement and routing of VLSI complexity SFQ circuits [15–17]. Two different approaches exist for routing signals in SFQ systems. These routing approaches support either short or long superconductive interconnects.

A challenging issue in automated routing methodologies in integrated SFQ circuits is the limited fanout of SFQ gates. Most SFQ

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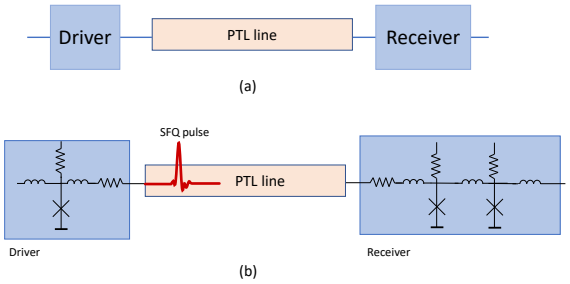

Figure 2: PTL interconnect topology, a) PTL line between driver and receiver, and b) PTL line with two JJs in the receiver and one JJ in the driver.

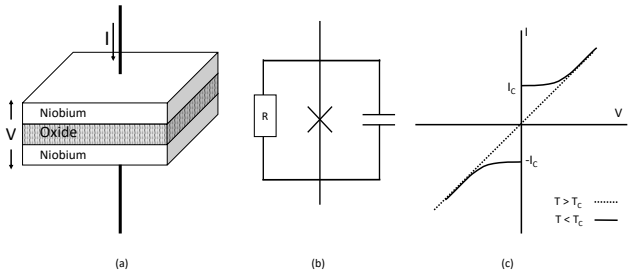

Figure 3: Josephson junction, (a) structure, (b) RCSJ model, and (c) I-V curves.

logic gates and flip flops exhibit a fanout of one [18]. A splitter gate is used to produce multiple output pulses [1]. To support multiple fanout, a large splitter tree is typically used in clock and data paths, significantly increasing the delay and power dissipation. Novel area and power efficient splitters are needed to reduce this overhead while supporting large fanout.

SFQ pulses propagate along a PTL at approximately one-third the speed of light without dissipation [19]. This feature motivates SFQ logic as a strong candidate for VLSI complexity ultra-high speed, ultra-low power digital applications. Utilizing PTLs rather than JTLs for long lines in SFQ circuits lowers the area, delay, and power dissipation [20–22].

A primary concern of automated routing methodologies in integrated SFQ circuits is pulse reflections in long transmission lines due to an imperfect impedance match between the SFQ load and the PTL line. A typical PTL topology with an input SFQ pulse is shown in Fig. 2. Due to the coincidence of the input SFQ pulse with the reflection of the previous pulse, resonant effects occur in long passive transmission lines [11]. The resonance in PTLs is dependent on the length of the PTL segment and the frequency of the SFQ signal. Specialized algorithms and guidelines for SFQ-based automated routing tools are needed to assign the interconnect length for each line and driver/receiver configuration when propagating a signal along a long passive interconnect [7, 20–24].

In this paper, the principles of SFQ technology and circuits are briefly reviewed in section 2. To support multiple fanout, several splitter topologies are discussed in section 3. Different routing methods are proposed for driving short and long interconnects. The properties of JTL interconnect are discussed in section 4. The properties of PTL interconnect are discussed in section 5. The characteristics of a PTL interconnect when inserting a repeater (driver/receiver pair) are reviewed in section 6. Avoiding resonance effects in long lines driven by these repeaters is also described in section 6. Automated routing in SFQ circuits is summarized in section 7. Clock routing for SFQ systems is discussed in section 8. Future work to improve SFQ routing methods is briefly reviewed in section 9. The paper is concluded in section 10.

2 PRINCIPLES OF SFQ LOGIC

The fundamental principles of SFQ logic are discussed in this section. The operation of a Josephson junction (JJ) is described in section 2.1. SFQ logic is explained in section 2.2. The primary routing components to propagate an SFQ pulse are reviewed in section 2.3.

2.1 Josephson junctions

Superconductive materials exhibit zero electrical resistance when cooled below a temperature known as the critical temperature T_C [25]. The Josephson effect is described as quantum tunneling in a superconductor across a thin insulator barrier by overlap of the wave function of a Cooper pair in two superconductive layers [26]. Operation of a Josephson junction (JJ) is based on this effect. The JJ is the primary active device in superconductive electronics. A JJ consists of two superconductive niobium layers separated by a thin layer of oxide [27, 28]. A JJ loses superconductivity when the bias current, temperature, or magnetic field exceed, respectively, a critical current I_C, critical temperature T_C, or critical magnetic field B_C. The structure of a JJ is illustrated in Fig. 3(a). Josephson junctions are modeled as a resistively and capacitively shunted junction (RCSJ). The RCSJ model of a Josephson junction is illustrated in Fig. 3(b). The I-V characteristics of a junction are shown in Fig. 3(c).

2.2 SFQ logic

An SFQ circuit consists of Josephson junctions and inductors. In SFQ circuits, information is transferred as picosecond duration voltage pulses $V(t)$ within a quantized area [1, 29–31]. Elementary logic gates in this circuit family can generate, pass, store, and reproduce picosecond voltage pulses. Switching a JJ is described as a 2π change in phase, producing a voltage pulse equal to a quantum of flux ($\phi_\circ = 2.07 \times 10^{-15}\ V{\cdot}s$) [32],

$$\int V(t)dt = \phi_\circ \equiv \frac{h}{2e}. \tag{1}$$

The existence of a flux quantum represents a logic '1,' otherwise, the absence of a pulse is a '0.' Most SFQ gates are clocked [1]. The incoming SFQ pulse changes the internal state of an RSFQ gate. The output can change once a clock pulse arrives at a gate.

2.3 Components of SFQ interconnect networks

An SFQ routing system is typically composed of splitters and interconnects. In this section, the components to enable SFQ routing, splitters and interconnect, are described.

2.3.1 Splitters. A splitter transfers a pulse from one location to two independent locations [1] due to the limited fanout of SFQ gates. These splitters convert a quantum pulse into multiple flux quanta, providing the ability to drive multiple SFQ circuits. SFQ-based automated layout and CTS tools utilize a tree of splitters to enable higher fanout. This splitter tree should exhibit robust timing characteristics to support high speed, large scale SFQ systems.

2.3.2 Interconnects. In SFQ circuits, two types of interconnects can transmit an SFQ pulse between gates, Josephson transmission lines and passive transmission lines. In SFQ circuits, a JTL interconnect transmits pulses without reflections. PTL lines transfer pulses with extremely low loss at approximately one-third the speed of light in a vacuum. Generally, for short interconnects, JTLs are preferable; for long interconnects, PTLs are preferable.

3 SFQ SPLITTERS

The distribution of data and clock pulses to multiple fanout is a primary concern in VLSI complexity SFQ systems. Most SFQ gates and flip flops exhibit a fanout of one. A splitter gate is required to convert a quantum pulse into multiple quanta without a significant decrease in amplitude. A splitter is typically placed at the output of an SFQ gate when driving multiple fanout. A standard active splitter is shown in Figs. 4(a) and 4(b) [33]. This active splitter can produce two SFQ pulses. A splitter tree with a fanout of four is depicted in Fig. 4(c). An important issue in this active splitter is the limited fanout while requiring a large bias current. To support multiple fanout, additional splitters are included within a binary tree structure, significantly increasing the total bias current, physical area, and dissipated power.

Novel splitter topologies have been developed to support multiple outputs while requiring less area and power and exhibiting lower delay. These area and power efficient splitters are 1) active splitter trees requiring fewer JJs, 2) passive splitters, and 3) multi-output active splitters [34]. The multi-output splitters dissipate less power and require smaller area than the active splitter trees since fewer JJs and lower bias currents are required.

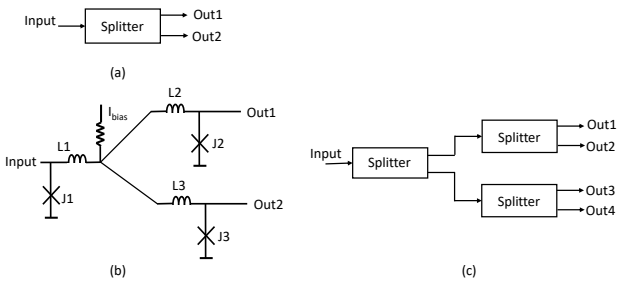

Figure 4: Standard SFQ splitters, a) block diagram with fanout of two, b) circuit with fanout of two, and c) block diagram of splitter tree with fanout of four.

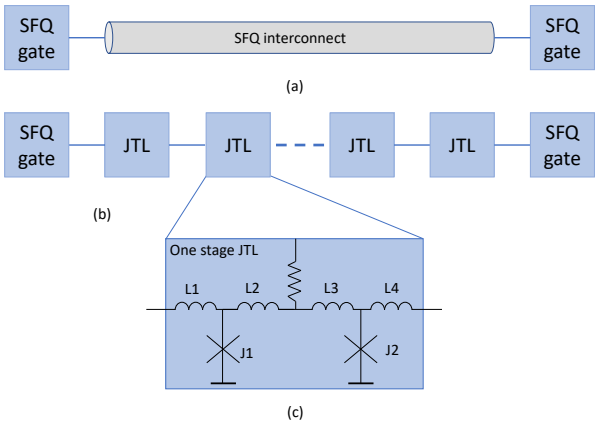

Figure 5: JTL interconnect topology, a) interconnect between two SFQ gates, b) chain of JTLs as interconnect between gates, and c) single stage JTL.

4 JOSEPHSON TRANSMISSION LINES

The propagation of SFQ pulses plays an important role in the efficiency of complex SFQ circuits. Josephson transmission lines are typically composed of basic cells to locally transfer an SFQ pulse between gates. JTLs also amplify an SFQ pulse between gates [1]. A Josephson transmission line can therefore be used as an interface between these gates [35]. JTLs, however, have certain disadvantages and restrictions.

A JTL is typically composed of uniformly sized Josephson junctions with a uniform inductance L between junctions. A chain of JTLs behaves as an SFQ interconnect, as shown in Fig. 5. The number of JTLs depends upon the distance between the SFQ cells. The length of one JTL stage is approximately 20 μm [7] (in a 10 kA/cm^2 technology). For example, for a distance of 200 μm between SFQ cells, ten JTLs are required.

The number and size of the JJs in the interconnect topologies affect the delay and physical characteristics. The delay of one JTL stage is about 5 ps. The delay of a chain of JTLs increases linearly with the number of JTLs. For a short line, a JTL requires less area with comparable delay as compared to a PTL. The JTL interconnect is located within the active gate layers. JTL-based SFQ interconnect consumes significant area, power, and delay when connecting distant SFQ circuits. Although not a significant issue in current MSI SFQ circuits, the greater area, power, and delay of a JTL are a significant challenge for prospective VLSI complexity SFQ circuits. Furthermore, certain constraints exist on the inductance within a JTL cell, which reduces the design flexibility of the physical layout [7, 8, 36–38].

5 PASSIVE TRANSMISSION LINES

In large scale SFQ circuits, PTLs are used to connect distant RSFQ gates. PTL interconnects decrease the propagation delay in long interconnections while amenable with automated routing and CTS layout algorithms. PTL interconnect use fewer JJs and dissipate less power than JTLs in long interconnects.

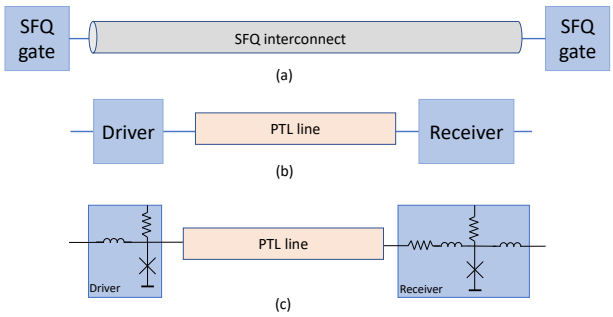

Figure 6: PTL interconnect topology, a) interconnect between two SFQ gates, b) PTL configuration as interconnect between gates, and c) PTL interconnect with the last JJ of the previous SFQ gate as the driver and one JJ in the receiver.

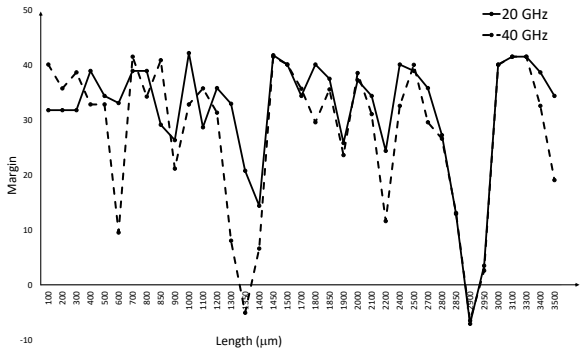

Figure 7: Resonance effects in a lossless superconductive transmission line at 20 and 40 GHz.

The length and area of a PTL interconnect affect both the JJ layers and the routing layers. A typical PTL consists of a superconductive microstrip or stripline in the routing layers, one JJ, a small inductance in the driver circuit, and two JJs with an inductance in the receiver within the active gate layers (see Fig. 2(b)) [39]. With three bias currents and JJs in a typical PTL topology, significant area and energy requirements are introduced into the bias network.

Fewer JJs within a PTL reduce the area, delay, and bias current of a PTL interconnect. A reliable topology for a PTL in a 10 kA/cm^2 technology is introduced in [7] to decrease the overhead. A PTL topology with one JJ in the receiver is shown in Fig. 6. The PTL driver includes the last JJ within the previous SFQ gate which produces the flux quantum pulse. The PTL receiver is composed of one JJ and a large inductance. The length of the line within the routing layer is dependent upon the distance between the two gates. For long interconnect, the delay and area of a PTL are significantly lower than the delay of a chain of JTLs. However, congestion in the routing layers, assuming space within the cell layers is available, can make a JTL the preferable choice for interconnect despite the greater area, power, and bias requirements.

A primary issue in superconductive PTLs is the impedance match between the PTL and the Josephson junctions. Due to the partial reflection and imperfect match between the PTL and the driver and receiver, resonant effects can occur in long PTL lines [11, 40–42]. This resonant effect depends upon the length of the PTL and the frequency of the SFQ signal. A methodology to manage and mitigate these effects is discussed in section 6.

6 REPEATER INSERTION IN SFQ INTERCONNECTS

One of the primary concerns of automated routing methodologies in integrated SFQ circuits is resonance effects within passive superconductive transmission lines. This effect occurs in a PTL line when the reflections of the SFQ signal from the receiver or driver coincide with the pulse within a line. These resonance effects decrease the bias margins or can produce incorrect circuit behavior.

An analysis of the bias margins of a receiver within a PTL is depicted in Fig. 7 for different interconnect lengths at 20 GHz and 40 GHz. The dependence of the bias margins on the PTL segment length is also depicted in this figure. The set of resonance lengths of a PTL segment depends upon the frequency of the applied SFQ signal which peaks at the lowest margin (see Fig. 7). The relationship between the resonant length of an interconnect segment and the frequency of an SFQ pulse is

$$f_{resonance} = \frac{n v_{phase}}{2L_l} \quad , \tag{2}$$

which v_{phase} is the phase velocity [11] of the superconductive passive interconnect. L_l is the physical length of the PTL interconnect, and n is an integer multiplier that describes the harmonics of the resonance frequency.

In Fig. 7, a sharp peak in the bias margin at 40 GHz (the dashed line) occurs at 1.35 mm and a second peak occurs at 2.9 mm. At lower frequencies, the resonance lengths occur in longer lines. The second resonance length at 40 GHz occurs at the same length as the first resonance effect at 20 GHz, consistent with (2). This resonance behavior affects the bias margins and can cause a circuit to not function properly.

For any frequency SFQ pulse, a set of forbidden PTL lengths is produced, which corresponds to the main resonant length, consistent with (2). To prevent this resonance effect from degrading circuit operation, this set of forbidden lengths should be avoided. The length of a PTL segment is limited to less than the shortest resonant length.

Similar to conventional CMOS circuits, repeaters are inserted into long passive transmission lines to partition a line into shorter segments [43, 44]. An SFQ PTL line with and without repeaters is shown in Fig. 8. The repeaters are located to ensure that the length of each interconnect segment is outside the set of forbidden lengths [11].

The objective of the repeater insertion process in SFQ interconnect is to determine the number of repeaters and the length of each segment within a long PTL. Assuming a bias margin for the receiver at 40 GHz, repeaters are inserted into a long PTL line, determining the number of repeaters and the length of each segment. A bias margin analysis in the PTL interconnect at 40 GHz (for a 10 kA/cm^2

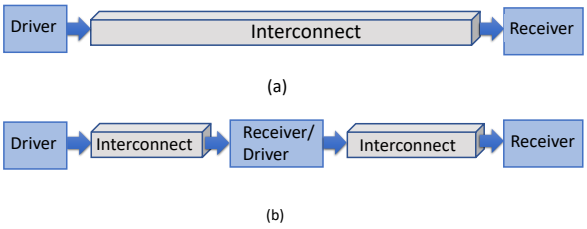

Figure 8: SFQ interconnect, a) no repeater, and b) with repeaters.

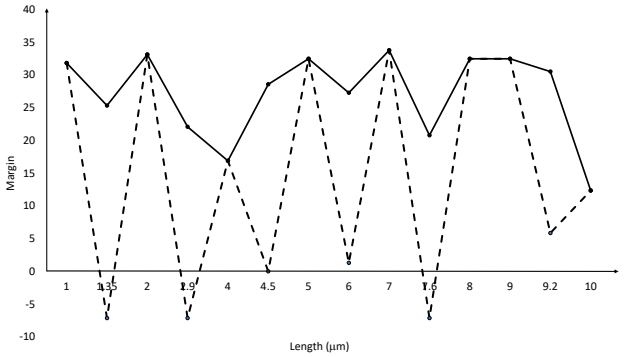

Figure 9: The effects of resonance on the bias margins of a receiver in a lossless PTL at 40 GHz with repeaters (solid line) and without repeaters (dashed line).

technology) is depicted in Fig. 9 without repeaters (dashed line) and with repeaters (solid line). These results illustrate the improvement in the bias margins of an interconnect with repeaters. The repeater insertion process in SFQ interconnect also improves the robustness of the receiver due to the wider margins.

7 AUTOMATED ROUTING IN SFQ SYSTEMS

For complex SFQ systems, the automated routing process determines the topology and method to connect cells while satisfying design constraints. These methods are intended as guidelines for EDA tools to enable robust routing with superconductive interconnects [3, 45, 46]. Routing in SFQ systems is preferably performed with one of two approaches, based on whether the path is local or global.

Global routing methodologies are typically used for long interconnects in SFQ systems. An objective of global routing is to produce the minimum interconnect lengths and/or skews [47–49]. Global routing divides the routing region into leaves (tiles), determining the path between these leaves. Global routing of SFQ circuits can be applied to clock distribution networks to produce near zero skew clock networks [50–54]. Local routing is an essential requirement to connect the data and clock paths between SFQ gates within lower level blocks. Longer interconnects typically require higher routing priority.

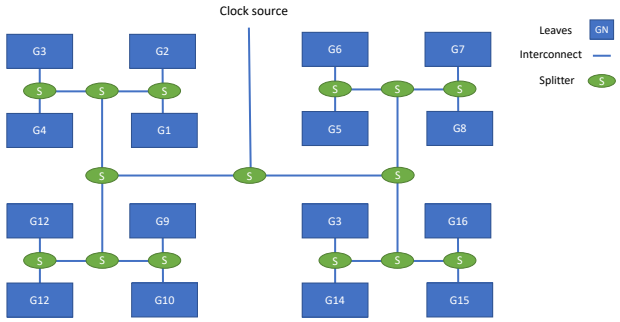

Figure 10: 16 leaf SFQ H-tree topology with splitters, interconnects, and leaves.

8 CLOCK TREE SYNTHESIS IN SFQ SYSTEMS

Clock tree synthesis is a process to distribute a clock signal to the individual clocked SFQ elements. The clock network typically has the highest priority to avoid competition with the data signals for resources. In SFQ circuits, a clock signal is required for most logic gates (except for splitters, JTLs, buffers, and mergers [1, 18]). An SFQ clock network is significantly larger than a CMOS clock network due to the need for multiple splitters. Clock routing in SFQ systems is often performed with two approaches, global symmetric clock networks [55] followed by local asymmetric clock networks [19].

Global clock synthesis of SFQ circuits is often designed to produce a near zero skew clock network. A commonly used global clock network topology is a symmetric H-tree network with asymmetric leaves to propagate the clock signal to the individual SFQ gates. A symmetric H-tree network is often used to distribute the high speed clock signals in VLSI complexity RSFQ circuits [55–60]. The structure of an SFQ H-tree clock network is shown in Fig. 10. The tree is composed of interconnects, splitters, and leaves. The symmetric structure ensures near zero clock skew between the leaves of the clock tree. Each leaf represents a functional block composed of a large number of SFQ gates. An SFQ H-tree clock network with N leaves requires $N - 1$ splitters, consuming significant area and increasing the clock path delay. PTL interconnects are typically used in these long lines in symmetric H-tree clock networks.

Local clock synthesis of SFQ circuits is used to produce a useful skew clock tree network within each block of the H-tree. A routing technique for asymmetric clock networks, based on the method of means and medians is proposed in [19] to minimize the skew within an SFQ clock tree. The location and number of clock sinks determine the topology of the clock tree network. The location of the splitters and the length of the interconnects determine the clock skew and delay of each clock path. JTLs are often used within each block if the distance between cells is short [49, 61, 62].

9 FUTURE WORK

Many issues exist in routing SFQ systems to ensure effective manufacturability. At present, routing guidelines are limited to coupling between interconnect lines. The SFQ signals propagating on the

PTL lines can magnetically couple to other lines, producing significant noise. In the physical layout of SFQ circuits [8, 28, 63], the PTL lines are placed between two ground planes. This feature increases coupling between the PTL lines. Bias lines carrying high current also affect the operation of the PTLs. Characterizing the local coupling sources between the PTL lines and the bias lines is needed to provide guidelines for enhancing the robustness of automatically routed layouts.

10 CONCLUSIONS

The propagation of signals is a significant issue in high speed, high complexity SFQ circuits. Several routing approaches for SFQ circuits are reviewed in this paper. Specific guidelines are summarized for PTL and JTL interconnect to determine how and when to use PTL or JTL interconnects. The JTL interconnect is faster and smaller than PTLs for short interconnects. The PTL interconnect exhibits lower complexity, area, power, and delay, making a PTL an appropriate structure for long interconnect in the automated layout of VLSI complexity SFQ circuits.

Resonance effects occur in passive superconductive transmission lines. These resonance effects constrain the routing process, producing a set of forbidden PTL lengths to be avoided. Repeaters are inserted into passive interconnects to prevent resonance effects in long PTL lines. Summarizing, guidelines to enable efficient routing of robust superconductive interconnects are necessary for evolving single flux quantum systems.

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