Clock Distribution Architectures for 3-D SOI Integrated Circuits

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I. INTRODUCTION

Distributing the clock signal in 3-D ICs is a complex and challenging task as sequential elements synchronized by the same clock signal can be located on multiple planes. Recent papers consider thermal effects on buffered 3-D clock trees [1] and H-tree topologies [2], [3]. No experimental characterization of 3-D clock distribution networks, however, has been presented. Measurements from a 3-D test circuit fabricated by the MIT Lincoln Laboratories (MITLL) [4] employing several clock distribution architectures are presented for the first time here.

In the following section, a brief summary of the MITLL process is provided. The design of the 3-D test circuit is reviewed in Section III. Experimental results of the three clock distribution networks are presented in Section IV. Some conclusions are offered in Section V.

II. FABRICATION TECHNOLOGY

The manufacturing process developed by MITLL for fully depleted silicon-on-insulator (FDSOI) 3-D circuits is summarized here [4]. SOI technologies are particularly suitable for 3-D circuits, since the SOI device layers can be used for both monolithic [5] and wafer level 3-D integrated systems. In the latter case, SOI constitutes a better solution for 3-D circuits due to the capability to more aggressively etch the wafers as compared to standard CMOS technologies. This situation is due to the high selectivity of the etching solutions. Solutions with a Si to SiO_2 selectivity of 300:1 are possible [6]. This capability results in significantly shorter through silicon vias (TSVs), which is a critical component in 3-D systems. The primary obstacle for 3-D SOI technologies is the high thermal resistance of the oxide which impedes the heat removal process.

The MITLL process is a wafer level 3-D integration technology with up to three FDSOI wafers bonded to form a 3-D circuit. The diameter of the wafers is 150 mm. The minimum feature size of the devices is 180 nm, with one polysilicon layer and three metal layers interconnecting the devices on each wafer. An attractive feature of this process is the high density TSVs. The dimensions of these vias are 1.75 μm × 1.75 μm, much smaller than the size of the TSV in many existing 3-D technologies [7]. A cross section of a 3-D circuit based on this process is shown in Fig. 1.

III. DESIGN OF THE 3-D TEST CIRCUIT

The test circuit consisting of three blocks is described in this section. Each block includes the same logic circuit but implements a different clock distribution architecture, and contains about 30,000 transistors. The power supply voltage is 1.5 volts.

The function of the logic circuit common to the three blocks is to emulate different switching patterns and load conditions for the clock distribution networks under investigation. Random switching patterns are generated in each block by combining pseudorandom number generators and several groups of four-bit counters that switch current loads over different time intervals. In addition, each of the circuit blocks is supplied by separate power and ground pads to ensure that each block can be individually tested.

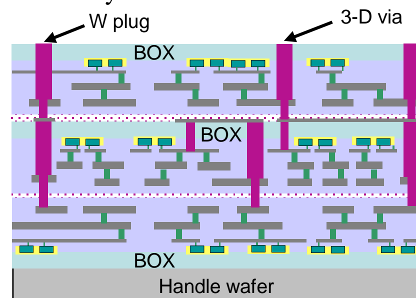

Fig. 1 Cross section of the MITLL 3-D fabrication technology [4].

Each of the three blocks includes a different clock distribution structure, which are schematically illustrated in Fig. 2. The dashed lines depict vertical interconnects implemented by TSVs. In each of the circuit blocks, the clock buffer driving the entire clock network is located on the middle plane. The location of the clock driver is chosen to ensure that the clock signal propagates through similar vertical interconnect paths to the top and bottom planes. The clock driver is implemented with a traditional chain of tapered buffers. Buffers are also inserted to drive the leaves of each H-tree in all three topologies.

IV. EXPERIMENTAL RESULTS

The clock distribution network topologies of the 3-D test circuit are evaluated in this section. These architectures combine different topologies, such as H-trees, rings, and meshes [8]. The fabricated 3-D test circuit is illustrated in Fig. 3. The highest achieved operating frequency is 1.4 GHz.

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The clock skew between the planes and the power consumed by each block operating at 1 GHz is listed in Table I. The H-tree topology produces the lowest skew as compared to the other two topologies but requires three H-trees and, consequently, dissipates the greatest power. Furthermore, the skew between the first and bottom planes corresponds to the delay of a stacked TSV traversing all three planes. The delay of the TSVs is small due to the short length of the vias, favoring SOI technologies for 3-D circuits.

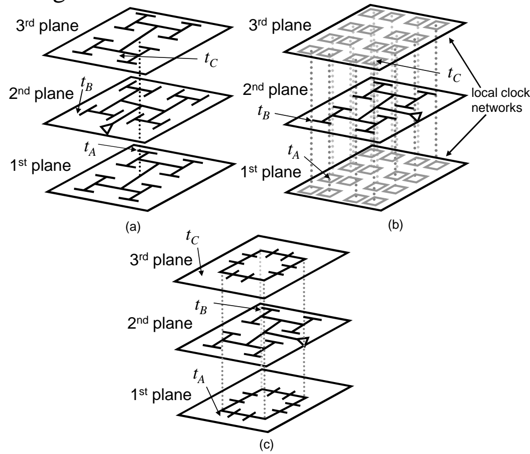

Fig. 2 Three 3-D clock distribution networks within the test circuit, (a) H-trees, (b) H-tree and local rings/meshes, (c) H-tree and global rings.

The clock skew among the planes is greater for the local mesh topology as compared to the H-tree topology, primarily due to the unbalanced clock load from the local meshes. The increase in skew, however, is moderate, while this topology dissipates the lowest power as only one H-tree is required for the global clock distribution network.

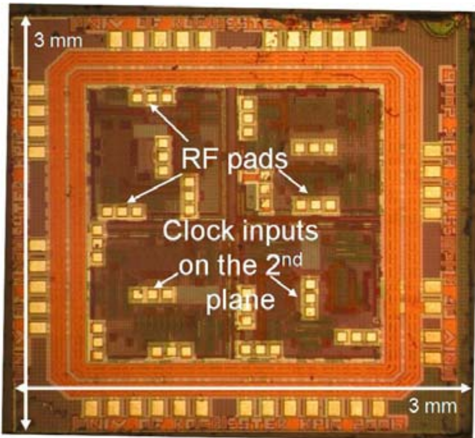

Fig. 3 Fabricated 3-D circuit. Some of the RF pads are also depicted.

The clock distribution network that includes global rings exhibits the highest clock skew among all of the topologies and slightly smaller power consumption than the H-tree topology. Since the clock distribution network on the second plane is implemented with an H-tree, the skew between adjacent planes is significantly larger than the skew between the top and bottom planes. Finally, the global rings block consumes less power than the H-tree topology due to the reduced amount of wiring resources used by the global clock network although the skew is the greatest.

Table I Measured clock skew among the planes and power consumption of each 3-D clock distribution network.

Clock distribution network	*Power consumption [mW]*	*Clock skew [ps]*		
		$t_{BA} = t_B - t_A$	$t_{BC} = t_B - t_C$	$t_{AC} = t_A - t_C$
Fig. 2a	260.3	32.5	28.3	-4.2
Fig. 2b	168.3	-68.4	-18.5	49.8
Fig. 2c	228.5	-112.0	-130.6	-18.6

V. CONCLUSIONS

Three topologies to globally distribute a clock signal in 3-D circuits have been evaluated. A 3-D test circuit, based on the MITLL 3-D IC manufacturing process, has been designed, fabricated, and measured and is shown to operate at 1.4 GHz. Clock skew measurements indicate that a topology that combines the symmetry of an H-tree on the second plane and local meshes on the other two planes will result in low clock skew for 3-D circuits while consuming the lowest power as compared to the other investigated topologies.

ACKNOWLEDGMENTS

The authors would like to thank Yunliang Zhu, Lin Zhang, and Professor Hui Wu of the University of Rochester for their help during testing and the MIT Lincoln Laboratories for fabricating the 3-D test circuit.

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