A 150-MHz 1.25 um CMOS/SOS DSP Integrated Circuit

W. L. Marking, S. R. Powell, R. R. Siviy, W. S. Kephart, and E. G. Friedman
Hughes Aircraft Company
6155 El Camino Real
Carlsbad, CA 92009

The delay and multiply chip, shown in Figure 1, was developed to demonstrate the performance capability of the Hughes Aircraft 1.25 um CMOS/SOS process and design methodology under stringent spacecraft environmental requirements. The block diagram of the chip, which implements a binary differential phase detection is shown in Figure 2. The circuit was designed to operate at extremely high clock rates under severe environmental conditions. The chip was fabricated and exhibited correct functionality at speed on first silicon. Packaged parts were shown to operate up to a tester limited 150-MHz at 5 volts. After a total dose irradiation of .5 MRad, parts were found to be completely functional up to 120-MHz. The circuit exhibited a pre-radiation power dissipation characteristic of .58 uW/gate/MHz at 3.3 volts, exemplifying the low power capability of this SOS technology. High speed testing utilized a bench test set-up integrated with a built-in self-test capability which automatically generated the test vectors on-chip. The built-in test vector generation was achieved by designing the data input registers to be configurable as linear sequence generators. The timing characteristics of the circuit have been compiled and preliminary results show excellent agreement with design specifications.

As shown in Figure 2, the basic architecture of the chip consists of two multipliers and one adder. Due to the nature of the architecture, a structured custom methodology [1] was applied in the design of the circuit. Specifically, our in-house developed Module Assembler Program (MAP)[2] was used to generate compiled SOS macrocells that were then interconnected with a minimal amount of routing and glue logic. The entire design was heavily pipelined (75% of the total transistors are in registers) in order to meet the high clock frequency requirements. There are approximately 8,400 transistors within 11,000 square mils, providing a density of approximately .76 transistors per square mil. By using MAP generated SOS macrocells for the two multipliers and the adder, the density of the internal portion of the chip is 1.4 transistors per square mil. The chip required special high speed output buffers able to provide 5 ns rise/fall times driving 25pF capacitive loads under worst case post-radiation conditions. The design of several different flip flop cells to eliminate possible internal race conditions was required due to the heavy use of pipelining.

Figure 1 depicts the advantages of using a structured custom approach. The two 6x6 bit multipliers are shown as long verticle rectangles at the top with the 13 bit adder at the bottom. The signal flow through the multipliers is such that the inputs come in at the top with the outputs leaving at the bottom which feed directly into the adder. This is similar to the signal flow for the entire delay and multiply chip in which the input buffers are located in the top half of the chip and the output buffers are in the lower half. As can be seen in Figure 1, the structured custom approach minimizes the amount of chip level routing, thereby minimizing the total chip size and design time (the total design, processing, and test time for this effort was less than six months). Thus, this circuit exemplifies the performance capability of CMOS/SOS, particularly within radiated environments.

References

[1] E. Friedman, G. Yacoub, and S. Powell, "A CMOS/SOS VLSI Design System," Journal of Semicustom ICs, Vol. 2, No. 4, pp. 5-11, June 1985.

[2] S. Powell and B. Barouch, "MAP: A Parameterizable Module Generator Development System Oriented to IC Design," Proceedings of the Custom Integrated Circuits Conference, pp. 5-8, May 1987.

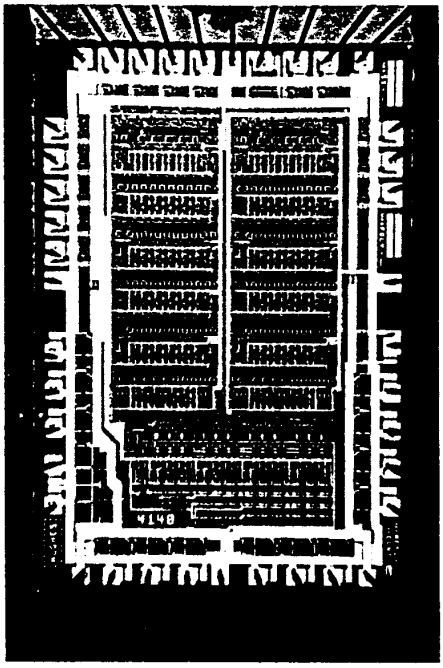

Figure 1 The delay and multiply chip.

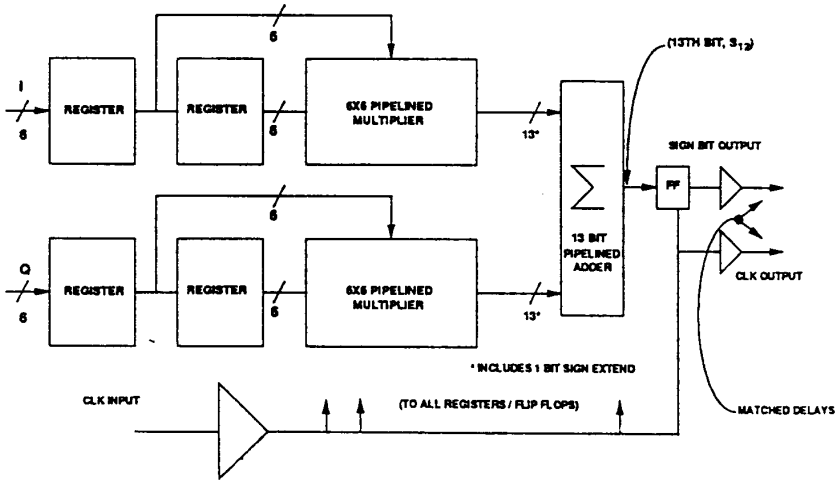

Figure 2 Basic architecture of the chip, consisting of two multipliers and an adder.