3-D Heterogeneous Sensor System on a Chip for Defense and Security Applications

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Abstract

This paper describes a new concept for ultra-small, ultra-compact, unattended multi-phenomenological sensor systems for rapid deployment, with integrated classification-and-decision-information extraction capability from a sensed environment. We discuss a unique approach, namely a 3-D Heterogeneous System on a Chip (HSoC) in order to achieve a minimum 10X reduction in weight, volume, and power and a 10X or greater increase in capability and reliability – over the alternative planar approaches. These gains will accrue from (a) the avoidance of long on-chip interconnects and chip-to-chip bonding wires, and (b) the cohabitation of sensors, preprocessing analog circuitry, digital logic and signal processing, and RF devices in the same compact volume. A specific scenario is discussed in detail wherein a set of four types of sensors, namely an array of acoustic and seismic sensors, an active pixel sensor array, and an uncooled IR imaging array are placed on a common sensor plane. The other planes include an analog plane consisting of transductors and A/D converters. The digital processing planes provide the necessary processing and intelligence capability. The remaining planes provide for wireless communications/networking capability. When appropriate, this processing and decision-making will be accomplished on a collaborative basis among the distributed sensor nodes through a wireless network.

1. INTRODUCTION

An ultra-small, ultra-compact, unattended multi-phenomenological sensor system providing an integrated classification-and-decision-information extraction capability from the sensed environment, is illustrated in Fig. 1. These systems are critically important for defense and security applications.

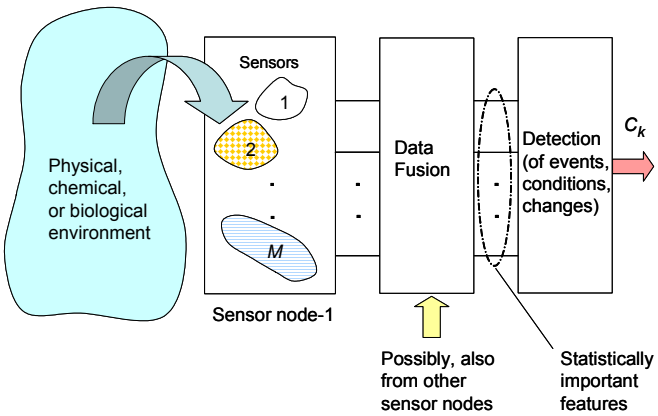


Fig. 1 Integrated sensing and information extraction system.

Unattended/Unmanned Ground, Ocean, and Air Sensor Technologies and Applications VI, edited by Edward M. Carapezza, Proc. of SPIE Vol. 5417 (SPIE, Bellingham, WA, 2004) · 0277-786X/04/$15 · doi: 10.1117/12.548199

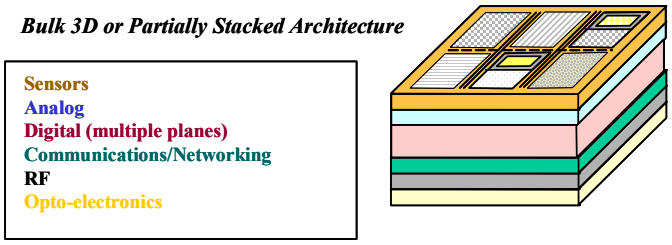


Fig. 2 3D Heterogeneous System on a Chip

Toward this goal, we describe a unique approach, namely a 3-D Heterogeneous System on a Chip (HSoC), as illustrated in Fig. 2. The target is to achieve a minimum 10X reduction in weight, volume, and power and a 10X or greater increase in capability and reliability – over alternative planar approaches. These gains will accrue from (a) the avoidance of long on-chip interconnects and chip-to-chip bonding wires, and (b) the cohabitation of sensors, preprocessing analog circuitry, digital logic and signal processing, and RF devices in the same compact volume. This concept is shown in Fig. 3 in greater detail, wherein a set of four types of sensors, namely an array of acoustic and seismic sensors, an active pixel sensor array, and an uncooled IR imaging array are placed on a common sensor plane. The other planes include an analog plane consisting of transductors and A/D converters. The digital processing planes provide the necessary processing and intelligence capability. The remaining planes provide for wireless communications/networking capability. When desired, this processing and decision-making will be accomplished on a collaborative basis among the distributed sensor nodes through a wireless network. Although a few example sensors have been previously cited, other important sensors in the sensor pool would be biochemical and general fluidic sensors. The application domain of these 3-D HSoCs would range from defense to security and biometrics/authentication.

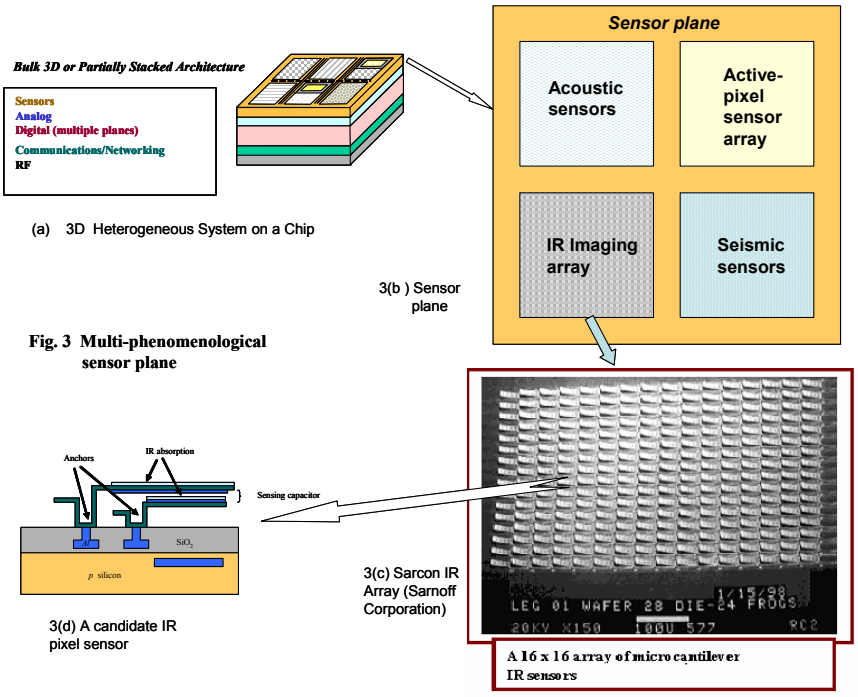


Fig. 3 Multi-phenomenological sensor plane

From a broader perspective, the realization of the concept will be ultra-small unattended 3-D multi-phenomenological sensor systems for rapid deployment with integrated classification-and-decision-information extraction capability from the sensed environment. Application scenarios of such 3-D Heterogeneous System on Chips (HSoCs) are depicted in Figs. 4 and 5. A conceptualization of one of many applicable battlespace deployments is illustrated in Fig. 4, and multi-level networking of the HSoCs for a wide-area coverage is shown in Fig. 5.

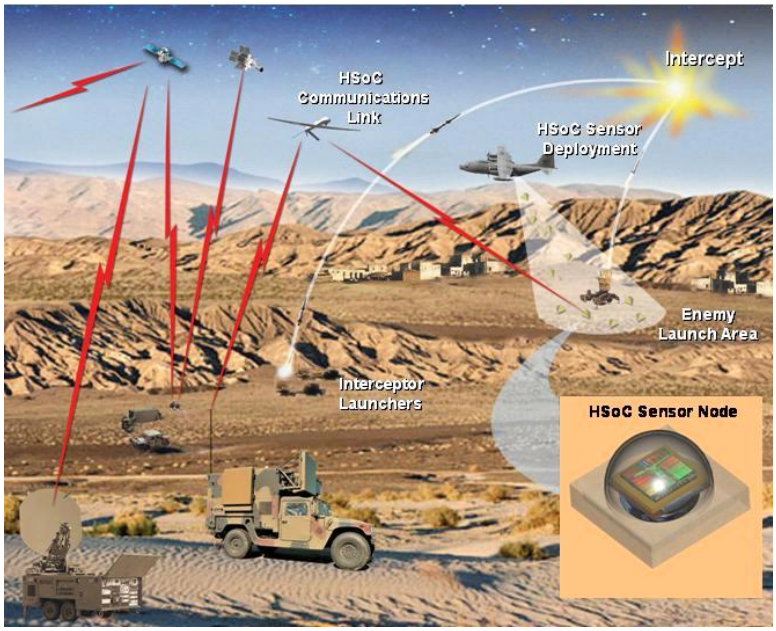


Fig. 4 A notional battlespace Deployment of unattended 3-D HSoC sensors (Harris Corp.)

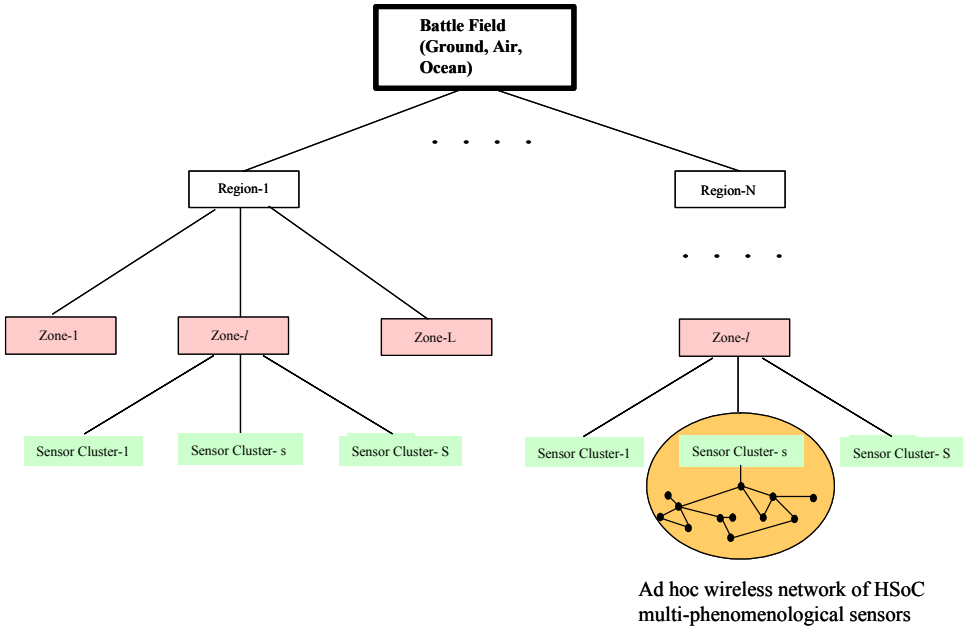


Fig. 5 Multi-level networking of the HSoCs

2. BREAKTHROUGH ADVANCES AND ENABLERS

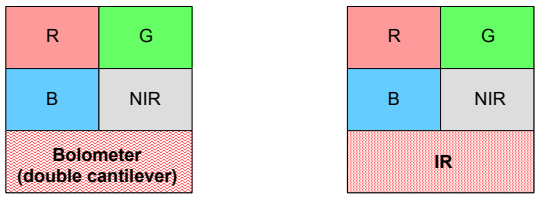
This section consists of seven parts, Parts 2.1 to 2.7, as described below.

Breakthrough advances:

2.1 Integration of four diverse sensor types on a common silicon substrate

The first challenge is that of integrating acoustic and seismic sensors, an Active Pixel Sensor (APS) imager, and an IR bolometer on the same silicon substrate in ways that create reliable and high sensitivity devices. In addition, the following new challenges are envisioned: (a) *combining the APS imager and IR bolometer into integrated hyperspectral pixels* such that a single lens system can create multi-spectral images of a common imaged-volume ranging from visible (380-740 nm in three color ranges) to near-infrared (with an NIR APS to 1090 nm) to deep infrared spectra; and (b) exploring the possibility of a materials/fabrication process that would enable silicon itself to detect farther into the IR region with photocurrent type devices, thereby eliminating the need for micro-cantilever bolometer subpixels (see Fig. 6). Part b is highly speculative, albeit with a potential for significant pay-off, producing higher sensitivity and more tunable far IR detection. In addition to materials and fabrication process innovations, resolution of issues related to noise and defect tolerance as well as interfacing to the transduction plane, will be the pathway to successfully demonstrating this sensor plane.

Fig. 6 Combining visible spectrum and IR spectrum sensing into a single pixel



(a) Combined IR to visible pixel

(b) All silicon combined IR to visible pixel

2.2 3-D heterogeneous system on a chip

Our 3-D System on a Chip (SoC) concept, illustrated in Figs. 2 and 3, will be developed with a view toward accurate detection of objects and events of interest with high sensitivity. The SoC includes a sensor plane which will be populated with a set of sensors, Sensor-1 …. Sensor-N, selected from a larger pool of sensors. In this paper we describe the use of acoustic sensors, active-pixel imaging array, IR imaging array, and seismic sensors. Also, it will be possible to soft-configure these sensors, remotely if desired, to suit a particular mission. For the accurate detection of objects and events of interest with high sensitivity, the *multi-phenomenological data will be fused and processed in an integrative way*. The feature extraction phase will utilize techniques such as ICA (Independent Component Analysis) upon the multi-domain data, in spectral and/or multi-resolution representations, which will be followed by either neural network techniques or Bayesian networks to arrive at classification-and-decision. Inter-plane switching will be used with a view toward fault tolerance, and dynamically allocating computational resources.

Besides the challenges of developing the individual planes with heterogeneous technologies, the following technology challenges are envisioned: (a) wafer thinning, (b) alignment and bonding, and (c) packaging, all *in the context of 3D HSoC*. Each of these four challenges will represent a significant leap forward with a large potential pay-off. In addition, the mapping of fusion algorithms, such as the ICA, integrally into a systolic DSP array on board the HSoC will represent a major advance.

2.3 Modeling and design of 3-D HSoC at the physical and circuit levels

Some of the physical and circuit level issues that will be particularly important for HSoC 3-D circuits are thermal Issues, electromagnetic interference, interconnect design, and clock and power distribution. In 3-D technologies the device densities per unit volume are much larger (as compared to the planar counterparts) with some device layers buried between two other device layers with no easy way to radiate the generated heat, thereby resulting in higher temperatures. This kind of mutual dependence between the thermal and electrical characteristics of the circuit requires a simultaneous use of *thermoelectrical* modeling, simulation, and design methodologies. The electromagnetic interference in 3-D HSoCs structures will be different in nature from planar technologies in many respects. The existence of several layers of devices would make the problem of vertical coupling among devices directly through the intermediate substrates much harder. In addition, interconnect will run vertically over nontrivial distances across Si substrates, which are semiconducting, and produce coupling that is not present in planar technologies. Finally, the large variety of devices – analog, digital, and sensors – will pose a serious challenge in maintaining signal integrity.

This research will provide solutions to the aforementioned problems by also developing tools and design methodologies. Issues involved in 3-D HSoC design and possible design alternatives to handle these issues are illustrated in Fig. 7. The targeted verification platform for heterogeneous SoCs, including thermal effects, is shown in Fig. 8. This verification and analysis platform will be used iteratively throughout the design methodology to enhance the resulting circuit design to satisfy target performance and reliability metrics.

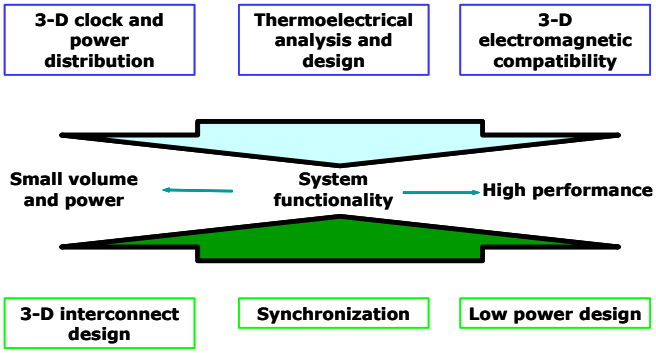


Fig. 7 Design methodology for 3D HSoC

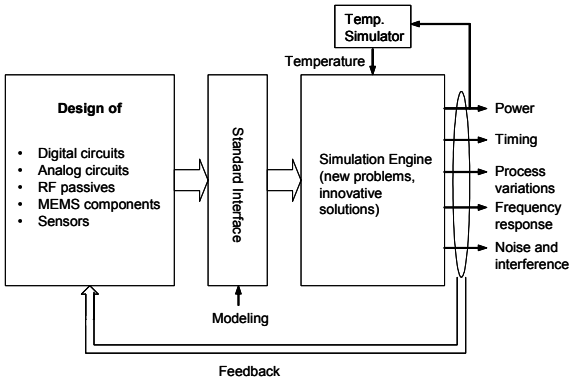


Fig. 8 Modeling and verification platform

Enablers:

The following will serve as enablers for propelling and completing the development of the first concept prototype. It is important to note, however, that each of these enablers represents a major technological advance.

2.4 Advanced RF design and *ad hoc* networking

RF components -- active and passive circuits, MEMS, and planar antenna, will be integrated onto the 3-D structure. An external plane (see Fig. 9) together with some of the adjacent planes will support embedded RF cores, leading to ultra-high performance systems within a small volume. Another aspect of the concept objective is to develop a low cost yield-enhancing non-intrusive probing methodology for on-chip testing of multi-GHz RF circuits, analog circuits, and mixed-signal circuits. The final result will be a fully integrated BIST architecture for the RF plane.

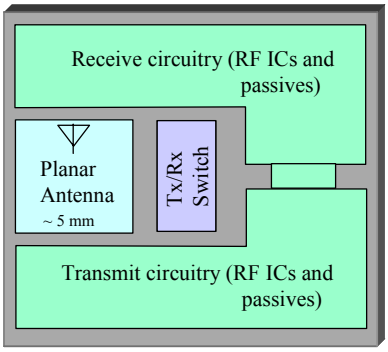


Fig. 9 RF plane (an outer plane)

2.5 Hierarchical 3-D interconnection network

Critical to the design and performance of the 3-D HSoC will be the interconnection network, binding the diverse planes and elements. In order to facilitate on-chip communication while minimizing the number of vertical channels, we propose to use a hierarchical interconnection network, such as the TESH, "Tori connected mESHes (TESH)." The key features of the TESH network are its hierarchy, thus allowing exploitation of computation locality as well as easy expansion, and compatibility with 3-D VLSI implementation since far fewer vertical wires are required than almost all known multi-computer networks (see Fig. 10). Redundancy will be used to circumvent faulty devices, including failed sensors and defective interconnect, especially faulty vias for vertical interconnect. Extension of the network to mixed signals will be a key focus in that a single network will bind all devices and computing modules.

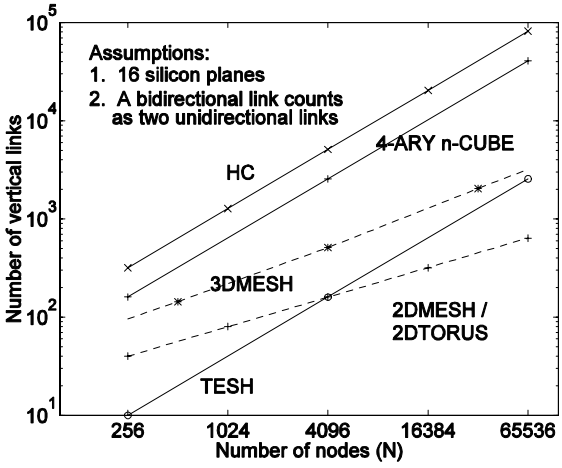


Fig. 10 Vertical links needed for various interconnection networks

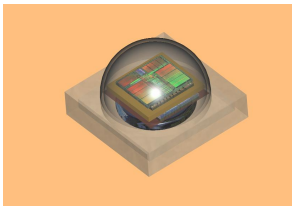
2.6 Reconfigurable DSP cells and mapping of advanced fusion techniques such as ICA

The central idea for managing the design gap is platform-based design, in which predefined architectures support the rapid creation of application-specific derivatives. In line with this strategy, we will develop and use a Field Programmable Function Array (FPFA)-based design methodology for the digital planes of the 3-D HSoC system. We have developed *coarse grain* cells designed for high functionality, performance, and reconfigurability. It is proposed to further develop and use these cells for the 3-D SoC with signal and image processing applications, including the mapping of the ICA technique to demix and separate the independent signal components of the multi-phenomenological sensor data for subsequent detection of objects/events. Another function of the DSP cell array will be to compensate for the actual positions of the functional sensors, which may be different from the nominal positions due to defect circumvention.

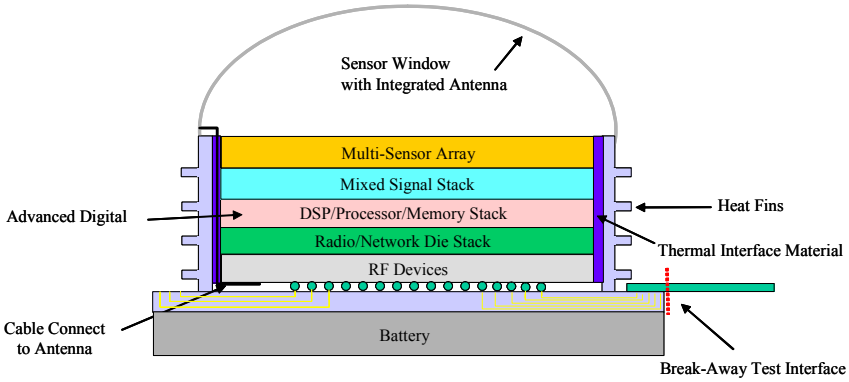
2.7 Micro-system integration, packaging, and multifunctional materials

Harris Corporation has developed technology and processes that enable the integration and packaging for 3-D HSoC, including techniques that accommodate the environmental accesses that are required by the multiple onboard sensors (acoustic, seismic, active-pixel sensor imaging array, and infrared imaging array). Harris will facilitate the transition to 3-D-HSoC-required integration, packaging and testing technologies by applying its innovative micro-miniaturization techniques within this new domain. The use of multifunctional materials will enable the ongoing improvement of micro-miniaturization by merging the functions of interconnection-substrates and packaging, and by eliminating most or all of the discrete passive components in the RF plane. In the framework of 3-D HSoC, the goal is volumetric efficiency, and Harris will contribute by utilizing its embedded passives, and conformal antenna technologies. Harris Corporation is focused on the system effectiveness of 3D-HSoC for defense-related capabilities, and accordingly will incorporate wireless

ad hoc networking in the communication architecture. Figure 11 depicts an objective monolithic packaging concept. A stack of five planes is shown, but some of these in turn could be stacks themselves. Integrated into the sensor window in Fig. 11(b) is a conformal cross-bow antenna. Also note the test interface, which will be removed after the final test.



(a)



(b)

Fig. 11 Objective monolithic package

3. DETAILS OF TECHNICAL APPROACH

The discussion is based in part on the different planes of the 3-D HSoC (see Fig. 2), and on the beakthrough advances and enabling technologies discussed in Section 2.

3.1 Sensor Plane:
All four types of sensors – seismic, acoustic, visible imaging (APS), and IR imaging – will be co-located on a common silicon substrate.

Acoustic and Seismic Sensors: Micromachined microphones will be used to detect acoustic and seismic waves on the order of 0.01Hz to 20 kHz. The source of perturbation will be spatially resolved based on the tailored design of an array of acoustic membranes. The required detection range will be met by arraying the basic microphone unit. Higher sensitivity and a flatter frequency response will be achieved by membranes of varying materials, thickness, and dimensions. To overcome possible fabrication or run time defects, a redundant array will be used; for example, if an $N \times N$ functional array is targeted, an $N \times (N+1)$ array will be fabricated and alternate routing used to harvest a working $N \times N$ array. DSP algorithms, in the digital stack, will be designed to compensate for changes in sensor distribution created by this harvesting. The response of the microphone would be tuned, exploiting the geometry of the diaphragm. The process flows would be investigated to fabricate the membranes of varying thickness on the same silicon membrane. Fabrication of multi-material microphones would be carried out to investigate the frequency response, sensitivity, and directivity for improved performance of the sensor as compared to the use of a single material membrane array.

Visible and IR Imaging Sensors:
HyperSpectral Detectors combining Active Pixel Sensors (APS) and IR bolometers: RGB APS, IR filtered APS and long wavelength bolometers will all be integrated into each pixel for spectral identification of emissions/reflections in order to achieve superior object discrimination.
New APS Designs: High reliability redundant APS pixels, with immunity to both high levels of fabrication defects and field time defects (e.g., due to radiation), and with low area, will be developed. Enhanced Adaptive Range Multiexposure APS will provide both expanded dynamic range and pixel by pixel real time

exposure adjustment. Image Time Differentiation APS would automatically detect the time related changes between two scenes, potentially providing both intensity and spectral time base changes within the APS.
Silicon Enhanced Long IR Detection: the potential for using heavy doping (with unconventional materials) to create silicon electronic detectors more sensitive to longer IR waves than those constrained by the current bandgap limit of 1.12 eV (corresponding to a maximum wavelength of 1071 nm) will be investigated. Reduced bandgaps are envisioned ranging from 0.6 to 0.25 eV with corresponding wavelengths of 2000 nm to 5000 nm.

3.2 Analog Plane Innovations:
The analog plane would house transductors and A/D converters. Innovations would include the use of resource sharing. To reduce volume and conserve power, resource-sharing will be used as shown in Fig. 12. Specifically, this economy will be realized by allowing multiple sensors to share transductors, and multiple transductors/AD-converters to share a common signal processing array. Another important aspect will be defect and fault tolerance through redundancy and reconfiguration.

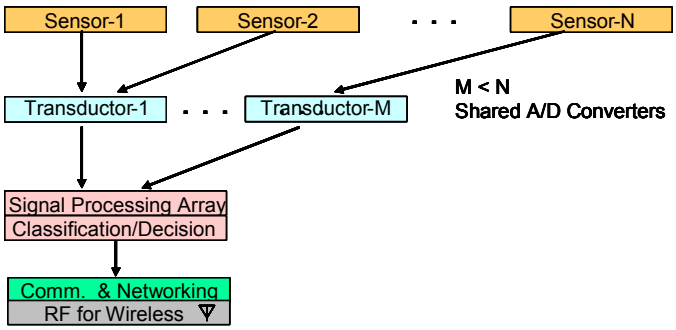


Fig. 12 Economy and flexibility through resource sharing

3.3 3-D Network Through All Planes:
In order to facilitate the on-chip communication, while minimizing the number of vertical channels, we propose to use the TESH ("**T**ori connected m**ESH**es") hierarchical interconnection network. Extension of the network to mixed signals will be a key focus. Also, redundancy to overcome possible defects in the modules or interconnect will be employed. This redundancy will enable successful communication among the modules and devices despite fabrication and processing defects. The latter would include defects in via generation due to misalignment or inadequate aspect ratios.

3.4 Reconfigurable DSP Cells and Mapping of Advanced Fusion Through ICA:
A *coarse grain* reconfigurable cell approach will be developed and implemented for the digital planes targeted at high functionality, performance, and reconfigurability of the 3-D HSoC signal and image processing objectives, including the mapping of the ICA technique to demix and separate the independent components of the multi-phenomenological sensor data for subsequent detection of objects/events. Reconfigurability will be useful both for mapping multiple applications to the same cell array, as well as for defect tolerance. A novel single-cycle nonlinear processor cell will be used to achieve a 10X or greater reduction in nonlinear computations that are pervasive in ICA computations.

3.5 Development of 3-D HSoC Physical and Functional Integration Technology: The Heterogeneous System on a Chip (SoC) concept will be developed with a view toward accurate detection of objects and events of interest with high sensitivity. Practical issues will include (a) placement of subsystems and subunits in the appropriate stack, more specifically one of its planes; selecting optimum areas and thicknesses of the various planes; contacts for vertical wires, (b) the thinning of the planes of the stack and their alignment and bonding, (c) generation of the deep vias through multiple planes and stacks for vertical communication, (d)

clock and power distribution, and (d) thermal management. At the functional end, the issues are (a) sensor signal conditioning in the analog plane/stack, including A/D conversion, (b) redundancy for overcoming defects, (c) resource-sharing to minimize volume, (d) inter-plane switching for reducing hot-spots and load-balancing, and (e) mapping of multiple DSP functions to a common pool of coarse-grain computational cells.
3.6 Clock and Power Distribution Networks for 3-D HSoC: A 3-D system will require effective strategies for synchronizing the data flow. Different synchronization strategies will target a 3-D topology. If fully synchronous, a novel clock distribution architecture will be required to manage the synchronization constraints for a 3-D system. These architectures and related circuit constraints will be integrated into a cohesive methodology for designing high performance 3-D oriented clock distribution networks. Architectures for power distribution that support a non-uniform HSoC structure will be developed to support these requirements. Additionally, DC and transient voltage drops within the power network will be incorporated into an overall methodology for designing a 3-D based power distribution network.

3.7 Interconnect Design: Issues such as locally distributed noise, power density issues, and asymmetric thermal characteristics such as local hot spots and related power removal constraints, all operating under high performance (high speed and low power) and density requirements, will be addressed and an effective solution produced.

3.8 Simultaneous Thermo-Electrical Analysis and Design of 3-D SoC Circuits: In 3-D technologies, device densities per unit volume are much larger with some device layers buried between two other device layers with no easy way to radiate the generated heat, resulting in higher temperatures. These high temperatures produce adverse effects on the device mobility and interconnect reliability. In addition, these thermal effects are in turn dependent on the electrical and run time characteristics of the circuit since the radiated heat depends on the switching activity and the circuit characteristics. This kind of mutual dependence between the thermal and electrical characteristics of the circuit will be addressed through simultaneous *thermoelectrical* modeling, simulation, and related design methodologies.

3.9 Electromagnetic Coupling in 3-D SoC Circuits: Electromagnetic interference in 3-D HSoCs structures is different in nature from planar digital technologies in many respects. The existence of several layers of devices will make vertical coupling between devices much more challenging. Previously, devices coupled through a single substrate. However, in a 3-D scenario, devices can couple directly through the intermediate substrates, significantly changing the nature of the problem. In addition, interconnect will run vertically over nontrivial distances across semiconducting silicon substrates, causing new forms of coupling effects that are not present in planar technologies. Finally, the large number of analog and digital circuits as well as sensors will pose a serious challenge for maintaining signal integrity. These problems will be addressed though new models and simulation techniques, and associated design techniques.

3.10 Micro-system Integration, Packaging, and Testing: In this technology transition to 3D heterogeneous sensor systems on a chip, the associated integration, packaging and testing technologies will also undergo a transition. Harris' innovative micro-miniaturization techniques will facilitate this transition when applied to the new tasks and challenges within the 3D HSoC context.

3.11 Multifunctional Materials and Embedded Passives: The use of multifunctional materials enables the ongoing improvement of micro-miniaturization by merging the functions of interconnection substrates and packaging and by eliminating most or all discrete passive components. Harris Corporation's embedded-passives and conformal-antenna technologies provide important contributions to the volumetric efficiency goal.

4. GENERAL DISCUSSION OF OTHER RESEARCH IN THIS AREA

Three dimensional (3-D) integration, combining multiple layers of planar devices with a high density of in-plane and out-of-pane interconnects, is a promising approach to extending performance beyond device and interconnect scaling limits [1]-[14]. 3-D integration provides high device integration density, high interconnectivity, reduction of long global wires and the related power consumption, novel architectures, and improved performance for system-on-chip (SOC) applications. One of the primary benefits of 3D integration is the freedom and efficiency in partitioning and integrating modules with mixed-signal or mixed-technology designs, such as logic, memory, analog, RF/Microwave, FPGA and Optical I/O. As compared to conventional ICs, 3-D ICs can mitigate processing complexity and cost in the heterogeneous integration of disparate materials such as Si, SiGe, GaAs or different circuit technologies such as CMOS, BiCMOS, and optoelectronic devices on separate device layers. Furthermore, improved noise coupling isolation among logic and analog/RF circuit blocks on separate device layers can be achieved with judicious separation of device types and the reduction of noise coupling through a common substrate.

MIT Lincoln Labs have developed an example of a 3-D IC [1]-[3] for low power and high bandwidth using a bonding approach. They have integrated two layers, namely an SOI wafer with imaging circuits and inverters to an SOI wafer with A/D converter circuits and inverters, using a combination of deep and shallow vias. This work shows the feasibility of stacking SOI circuits to build 3D ICs with dense vias and the results are being applied to the development of higher performance systems. A Cornell University team has developed a new single crystal Si layering and front-end-compatible interconnect fabrication process [4], [5] appropriate for mixed signal applications. Called MLBS, the technique combines a dual damascene process for in-plane and out-of-plane interconnects, chemical-mechanical polishing for bondable roughness, direct wafer bonding, and critical low–temperature silicon layering. A Japanese team from the Association of Super-Advanced Electronics Technologies has reported a 3-D stacking technology [6] using advanced bonding processes and DRIE for vias filled with copper to form microbump interconnections.

Indeed, the work of numerous other teams [7]-[13] has been examined. However, building ultra-small, ultra-compact, unattended *multi-phenomenological sensor system, with integrated classification-and-decision-information extraction capability* from the sensed environment on a 3-D Heterogeneous Sensor System Chip, has not been attempted, and is far and away more challenging. Our multi-university team together with our industry partner, Harris Corporation, will develop this capability, thereby achieving a quantum advance in technology, focusing on mission-specific performance.

5. MAJOR INNOVATIONS

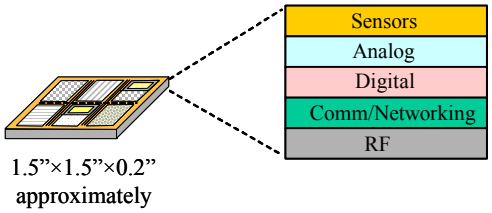
As stated in the abstract, the goal of this endeavor is to build ultra-small, ultra-compact, unattended multi-phenomenological sensor systems for rapid deployment with integrated classification-and-decision-information extraction capability from the sensed environment. Toward this goal, we propose a unique approach, namely a 3-D Heterogeneous System on a Chip (HSoC), as illustrated previously in Figs. 2, 3, and 11. This section delineates the anticipated innovations. On one of the planes of the 3-D HSoC, four types of sensors, namely an array of acoustic and seismic sensors, an active pixel sensor array, and an uncooled IR imaging array will be placed. Indeed, if successful, a plug-and-play capability can be imagined. That is, the sensor plane could, in the future, be populated with a set of N sensors, selected from a larger pool of sensors according to the requirements of the mission, and plugged into the 3-D HSoC without physically altering the other planes. Also, it would be possible to soft-configure these sensors, remotely if desired, to suit a particular mission. For the accurate detection of objects and events of interest with high sensitivity, the *multi-phenomenological data will be fused and processed in an integrative way*. The feature extraction phase will

utilize techniques such as ICA upon the multi-domain data, in spectral and/or multi-resolution representations, which will be followed by either neural network techniques or Bayesian networks to arrive at the classification-and-decision. The major challenges will be in the integration of the various planes with heterogeneous technologies into the overall stack, and indeed also in forming the planes which might themselves be formed as a stack of homogeneous technology planes.

From a higher-level perspective, our vision encompasses no less than the beginning of the "3-D integrated-system" technology revolution that will eventually supersede the 2-D "integrated circuit" revolution. As stated in Subsection 2.5E, building ultra-small, ultra-compact, unattended *multi-phenomenological sensor systems, with integrated classification-and-decision-information extraction capability* from the sensed environment on a 3-D Heterogeneous Sensor System Chip, has not been attempted. The successful realization of this objective will benefit not only the nation's defense, but will also provide the industry a launch pad for a new generation of innovation. A list of anticipated technical advances is given below.

- 3-D Heterogeneous system on a chip
- Multiple functionalities on the same chip: sensing, processing, and networking
- Vertical integration of the planes
- Multiphenomenological sensors on a common plane and on the same silicon substrate
- Combined APS and IR imaging pixels leading to a merged hyperspectral APS and IR imaging array
- Multi-exposure APS
- Novel reconfigurable DSP array, and sensor fusion at multiple stages
- Hierarchical interconnection network with aggregation for vertical links
- Collaborative sensing
- Efficient methodology for designing 3-D systems
- Simulation, prediction, and minimization of heating effects
- Power minimized architectures, placement, and technologies
- Drastic reduction in interconnect lengths and the efficient use of repeaters
- Design tools for 3-D systems
- RF plane subsystem
- Stand alone packaging of HSoC
- Defect and fault tolerance at all planes of the 3-D HSoC

Reduction in size and weight: since an integrated system with the capability of four types of sensors, namely arrays of acoustic and seismic sensors, an active pixel sensor array, and an IR imaging array, together with classification-and-decision-information extraction capability from the sensed environment does not, to our knowledge, exist, it is not possible to correctly estimate the size in terms of today's planar technology. Even so, we estimate the size with today's planar technology to be at least 6"×6"×1". Correspondingly, a very approximate sizing of the HSoC, excluding the package, is shown in Fig. 13.



HSoC: four types of sensors (acoustic, seismic, visible spectrum and IR imaging), decision capability, and *ad hoc* networking. Not shown is the package.

Fig. 13 Reduction in volume

Figure of Merit: A figure-of-merit is the following:

$$FoM \triangleq \frac{\{Weight, Volume\} \times Accuracy}{Power}$$

where '*accuracy*' is the accuracy or reliability from a functional or detection point of view. A 100X or greater increase in FoM relative to current implementations is envisioned. Naturally, the '*accuracy'* will consider the probability of missing a true event of interest and the probability of a false alarm.

5. CONCLUSIONS

A 3-D Heterogeneous System on a Chip (HSoC) concept for ultra-small, ultra-compact, unattended multi-phenomenological sensor systems for rapid deployment, with integrated classification-and-decision-information extraction capability from the sensed environment was presented in this paper. This approach is aimed at a minimum 10X reduction in weight, volume, and power, and a 10X or greater increase in capability and reliability – over the alternative planar approaches. Remote unattended sensors are invaluable for defense and security if they are deployable, affordable, sensitive, specific, reliable, long-lived, and rapidly transmit usable information to where it is needed. The 3-D HSoC technology is a way to provide improvements in sensory data collection, in conjunction with improved detection, classification and autonomous decision-making, in a smaller, lighter, package with greater energy efficiency and effective wireless inter-networking. This is all the more important because the 3-D HSoC technology is also a high risk but possible next step in the continuing integrated circuit revolution.

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