Chip-scale demonstration of 3-D integrated intra-chip free-space optical interconnect

Hui Wu[a], Berkehan Ciftcioglu[a], Rebecca Berman[b], Jianyun Hu[a], Shang Wang[a], Ioannis Savidis[a], Manish Jain[b], Duncan Moore[b], Michael Huang[a], Eby G. Friedman[a], and Gary Wicks[b]

[a]Department of Electrical and Computer Engineering, and [b]Institute of Optics
University of Rochester, Rochester, NY 14627, U.S.A.

ABSTRACT

This paper presents the first chip-scale demonstration of an intra-chip free-space optical interconnect (FSOI) we recently proposed.[1] This interconnect system uses point-to-point free-space optical links to construct an all-to-all intra-chip communication network. Unlike other electrical and waveguide-based optical interconnect systems, FSOI exhibits low latency, high energy efficiency, and large bandwidth density with little degradation for long distance transmission, and hence can significantly improve the performance of future many-core chips. A 1×1-cm^2 chip prototype is fabricated on a germanium substrate with integrated photodetectors. A commercial 850-nm GaAs vertical-cavity-surface-emitting-laser (VCSEL) and fabricated fused silica micro-lenses are 3-D integrated on top of the germanium substrate. At a 1.4-cm distance, the measured optical transmission loss is 5 dB and crosstalk is less than -20 dB. The electrical-to-electrical bandwidth is 3.3 GHz, limited by the VCSEL.

Keywords: Optical interconnect, free space optics, photonic integrated circuits

1. INTRODUCTION

The performance of microprocessors continues to improve with technology scaling, especially by increasing the number of cores. Communications in these chips, e.g. between processor cores and at the memory/processor interface, will demand larger I/O bandwidth, smaller latency and better signal integrity. To meet these demands, conventional electrical interconnects need better materials to minimize transmission loss, and increased circuit complexity (e.g. equalization) to compensate for bandwidth degradation for longer transmission distance, both of which increase energy consumption. Therefore, a fundamental change is required in the intra- and inter-chip interconnects. Optical interconnect exhibits inherent advantages in loss, delay and bandwidth compared to its electrical counterpart, and can potentially lead to significant performance gains and energy savings.[2–4] For inter-chip communications, optical interconnect systems with point-to-point topologies have already been developed, typically using on-board waveguides and directly modulated laser sources.[5,6]

For intra-chip communications, however, optical interconnect schemes proposed previously create new challenges: a packet-switching optical interconnect architecture requires either all-optical switching, which is still difficult for silicon, or repeated electrooptic (E/O) and optoelectronic (O/E) conversions, which increases latency and power consumption. A bus/ring architecture operating at a single wavelength does not satisfy the bandwidth requirement, particularly due to the link bandwidth degradation with the transmission distance.[7] Wavelength division multiplexing (WDM) can multiply the bandwidth of these systems, but require precise optical filters (e.g. microrings) with accurate wavelength control and minimal transmission loss,[8,9] which are difficult to fabricate in large-scale chips and require significantly more power if thermal tuning is needed. In addition, all of these waveguide-based systems use an power-hungry external laser source as the optical power supply, which is difficult to integrate and of high cost, especially in the WDM case.

As an alternative, free-space optics can be used to overcome some of the technical challenges of waveguide-based systems. Free-space optics has been successfully applied in board-to-board[10,11] and inter-chip applications.[12–16] These earlier proposals use arrays of discrete vertical-cavity surface emitting lasers (VCSELs) [17] and photodetectors (PDs), and interconnect them using free-space optics. In,[11,12] diffractive mirrors and fused silica slabs were used to guide light beams. Due to the small diffraction angle of the mirrors, a large number of reflections are required within the silica slab, resulting

Send correspondence to Hui Wu.
Hui Wu: Email: hui.wu@rochester.edu, Telephone: 1 585 275 2112

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in a long optical path even for a short distance. In,[10,13] lenses with large aperture size and focal length are shared among multiple VCSELs and photodetector arrays to increase bandwidth density. However, these macro-scale lenses are too thick to be fabricated using standard microfabrication processes, and the long throw distance results in a large link latency. Improved designs using microlenses[15,16] has been proposed to overcome these limitations.

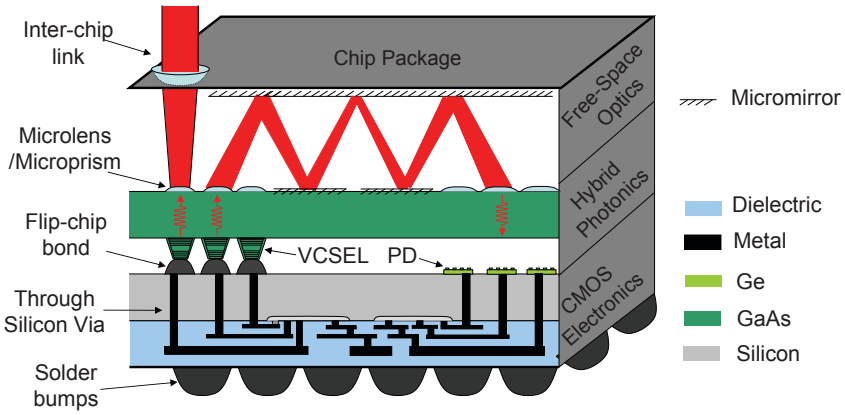


Figure 1. Cross-sectional view of the proposed 3-D integrated FSOI system. It can also be used for inter-chip communications with other chips.

Recently, we proposed an intra-chip interconnect system based on free-space optics and 3-D integrated photonic devices.[1,18] The main motivation is to construct an all-to-all communication network with large bandwidth density and without switching. As shown in Fig. 1, this free-space optical interconnect (FSOI) system consists of a photonics layer and a free-space optical guiding medium constructed using micromirrors and microlenses, which are stacked on top of the CMOS electronics layer by 3-D chip integration. The light beam generated by an electrically modulated VCSEL is focused by a microlens at the backside of the GaAs substrate, similar to.[19,20] After bouncing from the mirrors on the package multiple times, it is focused by another microlens onto a PD, where it is converted back into an electrical signal and then processed by the CMOS transceiver electronics. In this system, optical communication links are constructed directly between communicating nodes in a totally distributed fashion, without requiring a centralized arbitration system. Therefore, it has significant signaling and networking advantages. First, FSOI avoids packet-switching and the associated intermediate routing and buffering, and arbitration delays in electrical networks or packet-switching optical networks, providing low latency. Second, FSOI exhibits very low propagation loss, minimal dispersion, and no bandwidth degradation regardless of topological distance. Third, FSOI saves a significant amount of interconnect and total energy consumption in the system by a) eliminating packet-switching related energy consumption, b) powering VCSELs down in low duty-cycle operation, and c) avoiding thermal tuning of sensitive E/O modulators in WDM systems. Finally, FSOI's good signal integrity simplifies CMOS transceiver electronics to a conventional driver in the transmitter and an amplifier in the receiver. In this paper, we report the design, fabrication, integration and measurement results of the first chip-scale prototype to demonstrate this intra-chip FSOI system.

2. DESIGN OF CHIP PROTOTYPE

The proposed chip-scale intra-chip FSOI system is shown in Fig. 2. It is designed based on the following specifications and constraints: the target chip has an area 1×1-cm^2 limited by the autostepper lithography and mask size, and the longest optical path is 1.4 cm, diagonally crossing the chip after bouncing twice from the mirrors. The Ge substrate is used to build PDs and serve as a carrier for the VCSELs and microlenses. The MSM Ge PDs have 62×62-μm^2 area and achieve more than 12-GHz bandwidth. The microlenses are fabricated on a 525-μm thick fused silica substrate. The VCSELs used in the prototype is a commercial VCSEL array (Finisar V850-2092-001S, 1x4 array) with a pitch size of 250 μm, and provides 2-mW optical power at 850-nm with a 5-GHz modulation bandwidth. The pitch size between microlenses is chosen as 250-μm, matching the pitch size of the commercial VCSEL array chip. To facilitate wirebonding VCSELs and PDs to the Ge carrier, a silica spacer is inserted between the microlenses and the VCSEL/PDs. The prism is only for testing purposes.

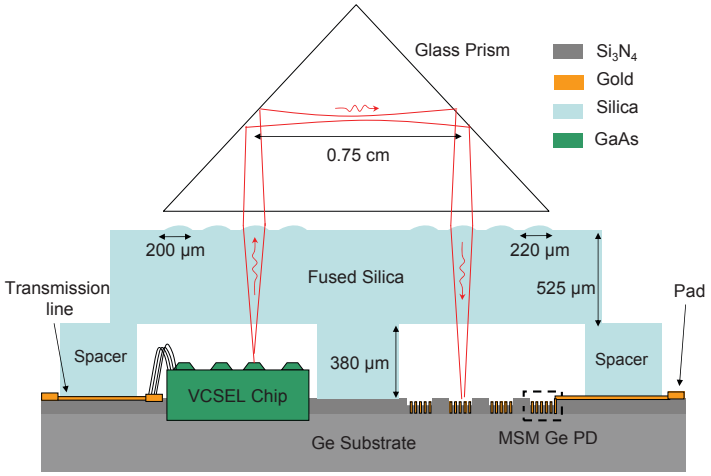


Figure 2. Schematic of the chip-level FSOI prototype.

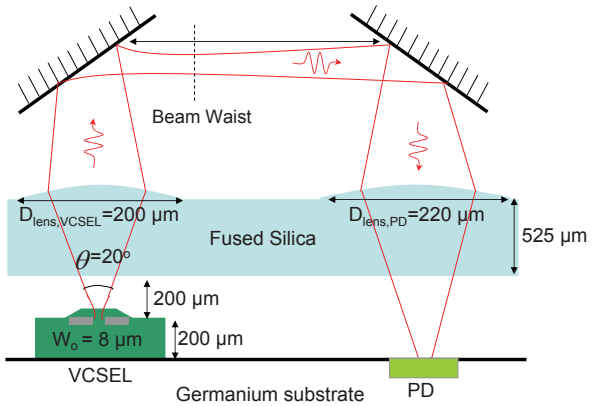


Figure 3. Schematic of the FSOI link designed for the chip prototype. The total distance is 1.4 cm, corresponding to crossing the chip diagonally. The optical parameters of the commercial VCSEL are from the datasheet and test results. The parameters of MSM germanium PD are simulated in DAVINCI.

2.1 Optics Design

The optics design involves several device parameters: VCSEL aperture size/divergence angle, microlens aperture size and focal length, and device spacing, as shown in Fig. 3. The 850-nm commercial VCSEL has an aperture size of 8 μm, and the full-width half-maximum (FWHM) far-field divergence angle is measured as 20^o in free space at the operation bias point. Since there is a 200-μm height difference between the VCSEL chip and PD, the microlens aperture and focal length need to be adjusted correspondingly. The VCSELs and PDs are located 200-μm and 400-μm away from the back of the fused silica layer, or 565-μm and 765-μm from the lenses in air. The corresponding focal lengths are slightly less than these values because source and detector needs to be placed further away from the focal planes in order to construct the link, as depicted in Fig. 3.

As discussed in Sec. 3, microlenses are fabricated based on the photoresist melt-and-reflow technique. The desired microlens aperture size is defined by lithography, and its focal length is achieved by selecting the photoresist thickness,[21] as shown in Fig. 4. Assuming that the VCSEL is placed nearby the focal point of the VCSEL lens to capture more than 98% of the light, the minimal aperture size should be 200 μm. The corresponding photoresist thickness to achieve a 200-μm aperture and a 560-μm focal length lens is 10 μm, as shown in Fig. 4. Similarly, the same photoresist thickness achieves 725-μm focal length for a 220-μm aperture size lens at the detector end. Note that the focal length for the PD lens should be slightly less than the 760-μm detector distance to the microlens, in order for the PD to receive the smallest spot size.

Using the designed focal length and aperture sizes, the beam waist size and its distance from the first microlens is calculated with respect to Δz, the relative position of the VCSEL source to the focal point of the lens based on Gaussian

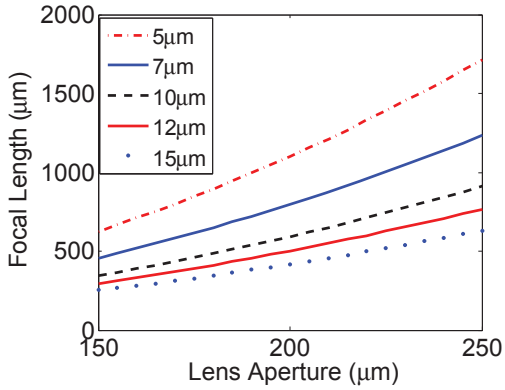


Figure 4. Microlens focal lengths (in free space) vs. aperture size for different photoresist thickness. Using 10-μm photoresist, 200-μm and 220-μm aperture size microlenses can achieve the desired focal lengths.

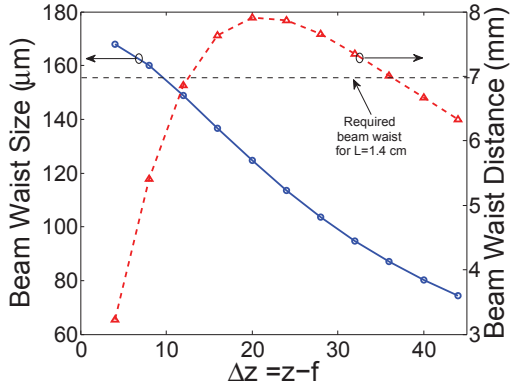
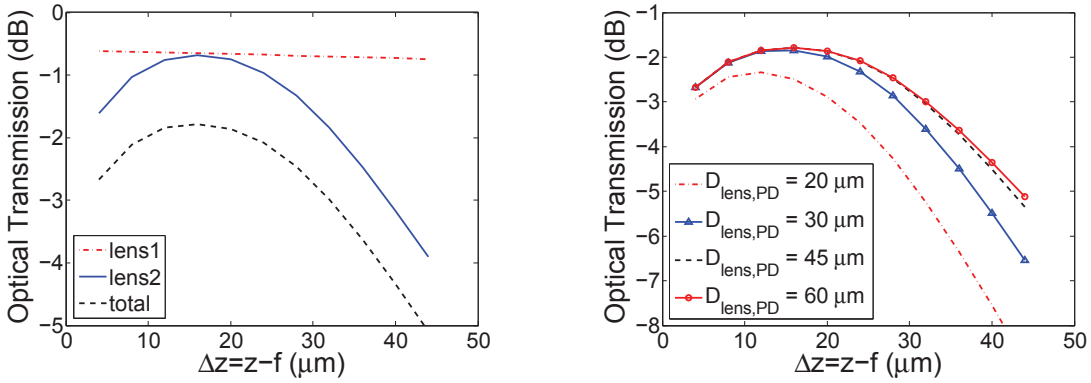


Figure 5. Calculated beam waist size and position from the first microlens. The beam waist distance to the PD microlens for total 1.4-cm link distance needs to be 7 mm or longer for a 14-mm throw distance.



(a) (b)

Figure 6. Calculated optical transmission (a) through the lenses and at the PD for a infinite large PD diameter, and (b) at the PD for different PD diameters with respect to relative position of the VCSEL source to focal point of the microlens. The path distance is 1.4 cm and the light bounces twice from the 95% reflective mirrors. Note that all power is captured by the PD beyond 45-μm diameter.

beam propagation. As shown in Fig. 5, the beam waist distance after the first lens is larger than 7 mm, i.e., half of the longest link distance, when the VCSEL is placed between 10 μm and 40 μm away from the lens. Within this range, the beam waist size changes between 110 μm and 160 μm. Cascading it with the PD lens, the normalized optical power transmitted through the lenses for the 1.4-cm link distance is plotted with respect to Δz in Fig. 6-a, when the PD has infinite size. Optical transmission peaks at Δz between 10 and 20 μm, matching that of the beam waist distance in Fig. 5. Considering the power loss due to finite a PD size, the detected power is calculated as shown in Fig. 6-b. The detected power does not change for PDs beyond 45-μm detector diameter. Adding tolerance for possible integration errors, the PD size is chosen as 62×62 μm^2.

2.2 Signaling

In order to evaluate interconnect performance, the values of the PD responsivity, VCSEL slope efficiency, and the device bandwidths are needed. Based on our prior work ,[22] an MSM Ge PD with hydrogenated a-Si (a-Si:H) is designed and simulated in DAVINCI. A device with a 20-nm thick a-Si:H layer, 1.25-μm contact width, 2-μm contact spacing, with a low stress Si_3N_4 anti-reflection coating on the top of the 62×62-μm^2 area achieves 0.224-μA dark current and 0.37-A/W responsivity at 7-V bias. The simulated bandwidth is 12.1 GHz with a 80 fF device capacitance, corresponding to a 40-GHz extrinsic bandwidth when terminated with 50 Ohm. The commercial VCSEL has a slope efficiency of 0.4 W/A and 2-mW optical power at 850-nm. In a single-bit FSOI link, the electrical-to-electrical link gain, which is expressed as the product of the slope efficiency, responsivity and the optical transmission efficiency, is -20.6 dB. The simulated bandwidth of the MSM PD is 12.1 GHz at 5-V bias, and the VCSEL has a modeled small-signal bandwidth of 5 GHz at 3 mA forward bias current and 1.7-V bias.

Based on the optics and link parameters, a 1×1-cm^2 FSOI chip has 5.7-Tbps aggregate bandwidth for an 8-bit communications network. Corresponding channel and bandwidth densities are calculated as 570 cm^{-2} and 5.7-Tbps/cm^{-2}, respectively, assuming that half of the chip area is reserved for mirrors to guide the beams.

3. DEVICE FABRICATION, CHARACTERIZATION, AND INTEGRATION

3.1 PDs and the Carrier Chip

This FSOI system is designed to support 10-Gbps data rate per optical link at 850 nm. Ge is chosen over other semiconductor materials thanks to its CMOS integration compatibility, which is crucial in large-scale electronic-photonic integrations, and its good optical and electrical properties, allowing PDs to exhibit good sensitivity and large bandwidth. A metal-semiconductor-metal (MSM) structure is chosen over p-i-n ones to reduce parasitic capacitance per area, to allow less stringent microlens-to-PD alignment for efficient light coupling, and to simplify the contact definition in the fabrication to a single step, while achieving reasonably good bandwidth and responsivity.[22]

The fabrication procedure begins with the passivation of the Ge wafer by consecutive HCl and HF dip cycles, followed by 20-nm thick hydrogenated amorphous Si (a-Si:H) deposition, serving as the surface passivation and Schottky barrier enhancement layers in order to provide low dark current and large bandwidth. Then, 240-nm thick low-stress Si_3N_4 is chemical-vapor-deposited (CVD) on top of the a-Si layer, serving as an isolation between the electrical lines and substrate, as well as an anti-reflection coating in the active region. In the first lithography step, the alignment markers are etched into the carrier chip. A 1.45-μm deep groove for the VCSEL is then patterned in the and etched into the Ge substrate by via plasma enhanced reactive-ion-etching (RIE). The third lithography step defines the active PD area, where the metal contacts are connected to the substrate. The next step is the removal of 140 nm of the 240-nm thick Si_3N_4, leaving a 98-nm thick Si_3N_4 film at the active region. In the final lithography step, the contact widths of 1.25 μm and spacings of 2 μm are patterned. The 98-nm thick Si_3N_4 layer at the metal contact regions is etched down to the a-Si:H layer. Subsequently, 11-nm thick Ti and 230-nm thick Au are evaporated and then lift-off is performed. The remaining 98-nm thick Si_3N_4 in between contacts in the active PD region serves as an anti-reflection coating, and improves the responsivity. The chip photo of Ge carrier with integrated PDs is shown on the left side of Fig. 9-a.

Each MSM Ge PD occupies a 62×62-μm^2 area, exhibiting 83-fF capacitance, and have a 0.315-A/W responsivity and 7-μA dark current (Fig. 7-b), both better than .[22] The PD bandwidth is 9.3 GHz at a 7-V bias, mainly limited by the transit time of carriers, and wirebonds from the chip to the PCB trace (Fig. 7-c).

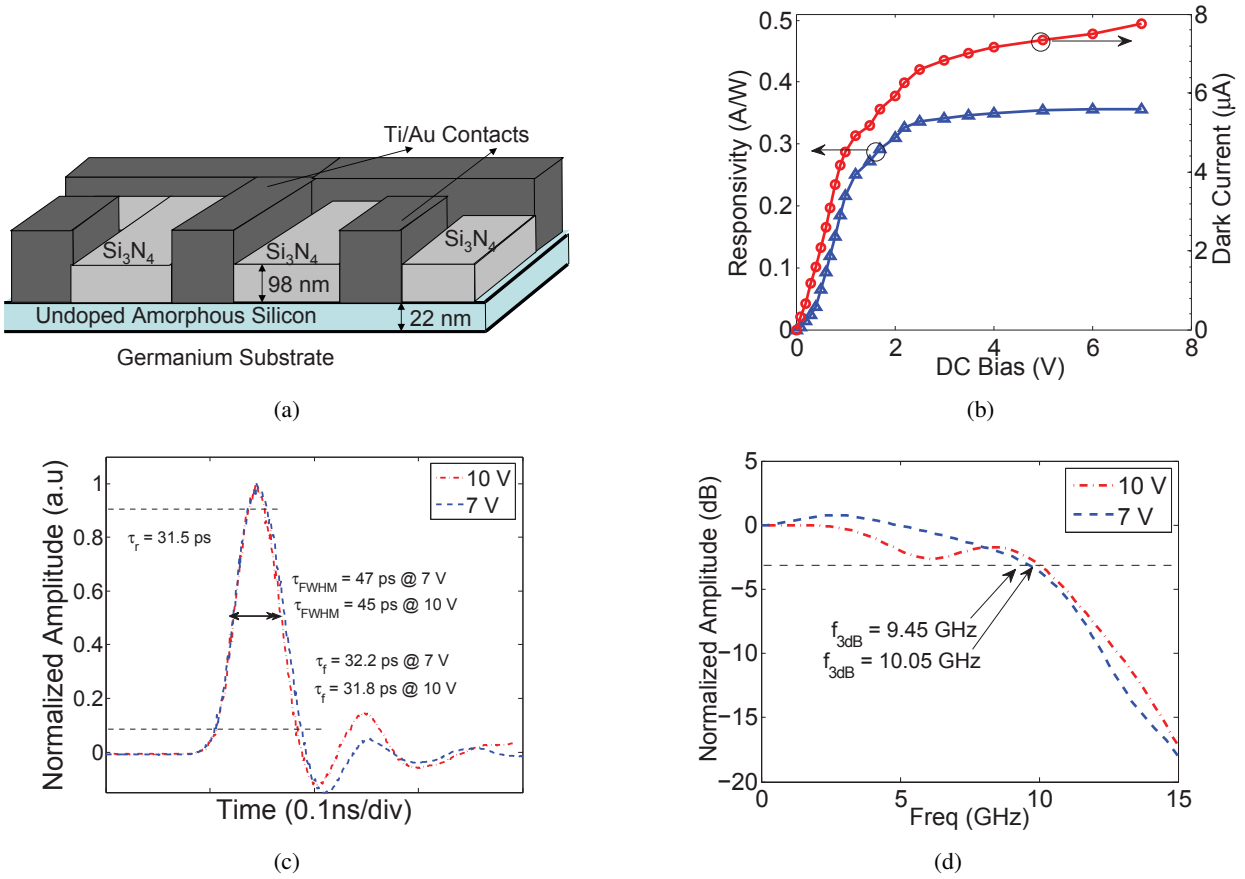


Figure 7. (a) The structure, (b) responsivity at 850-nm illumination and dark current, (c) impulse response using 50-GHz sampling oscilloscope at 7-V and 10-V biases, and (d) DFT converted measurement results for the 62×62-μm^2 area Ge MSM PD with 98-nm Si_3N_4 anti-reflection coating. The dark current density is measured as 1.7 nA/μm^2 at 7-V.

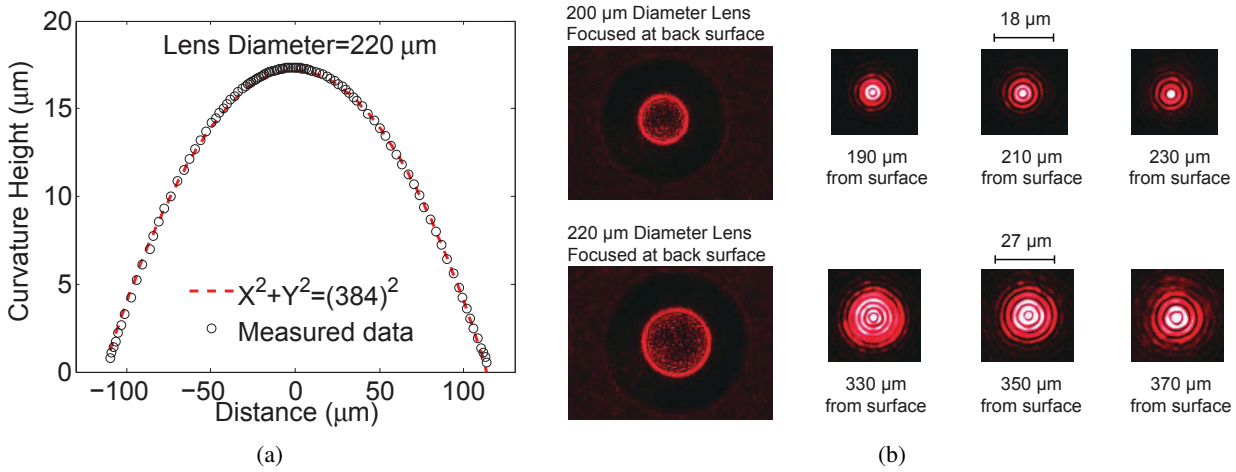
3.2 Microlenses

In microlens fabrication, the goal is to implement lenses with low transmission loss, and accurate focal length and aperture sizes. Fused silica offers very low optical transmission loss at 850-nm wavelength, is compatible with CMOS processes, and can be easily 3-D integrated with silicon substrates.

The lenses are built by melting and reflowing of the photoresist into a spherical shape and then dry etching the pattern into silica wafer. Fabrication begins with the plasma etching of the wafer-to-wafer alignment marks into the fused silica wafer. In the second lithography step, 9.8-μm thick cylindrical photoresist patterns with 200 and 220-μm diameters are defined, and subsequently melted and reflown on a temperature controlled hot plate similar to.[23] The height of the photoresist curvature is 17 μm for 220-μm aperture lens, corresponding to a focal point of 710 μm in air. Finally, after the lens curvature are defined, the photoresist is transferred into the fused silica wafer by dry etching without significantly deviating from a spherical wave shape. The sample is finally cleaned with O_2 plasma to remove the photoresist remnants. The final lens thickness is measured as 15.3 μm. The fabricated microlenses for VCSELs and PDs have 200 and 220-μm aperture size with focal point 580 and 730 μm in air, respectively (Fig. 8-c), exhibiting a 1.55-dB total optical transmission loss per lens. The total microlens chip area, shown on the right side of Fig. 9-a, is 0.84×0.84 cm^2.

3.3 Chip Prototype Integration

The VCSEL and fabricated microlens chips need to be integrated with the Ge-carrier with high accuracy, minimal tilt and rotational errors. We use non-conductive epoxy to bond the chips together and use wirebonding to electrically connect them. In order to increase the integration accuracy, the tilt and rotational errors between each chip are checked under the optical interferometer and minimized before curing. The detailed integration steps are explained as following:



(a) (b)

Figure 8. (a) The measured shape of the photoresist after the melt and reflow process, (b) spot sizes of collimated beams at the back surface of the 200-μm and 220-μm aperture size lenses. Based on the photoresist refractive index of 1.54 and the measured radius of curvature of 384 μm, the focal length in air is calculated as 710-μm for the 220-μm aperture lens. The peak-to-peak surface roughness is approximately 0.9 μm, corresponding to a measured 1-dB optical scattering loss.

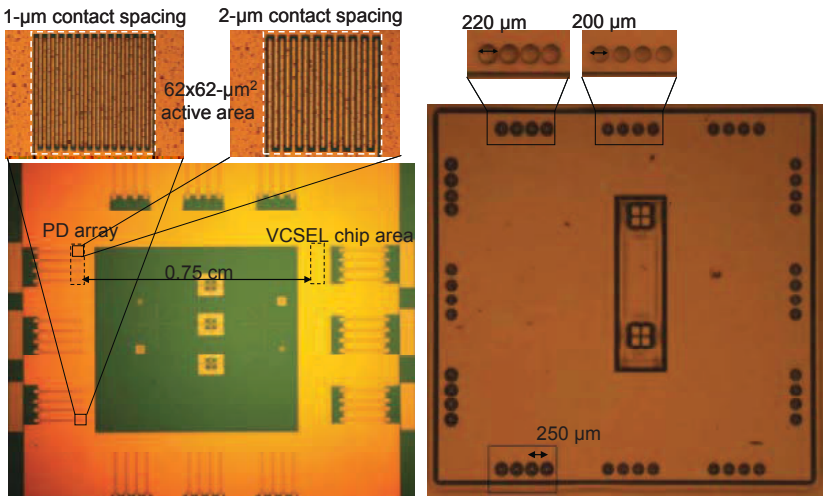
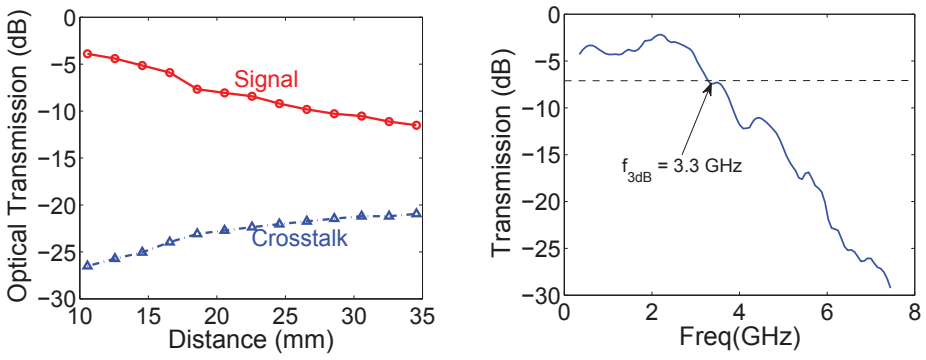


Figure 9. Images of the Ge carrier and fused silica microlens substrate of the FSOI system.



(a) (b)

Figure 10. (a) Transmission and crosstalk for increasing different link distances, and (b) small-signal bandwidth at L=1 cm. Note that the optical transmission changes between -4 at 1-cm distance due to the reflection and scattering losses of the lenses. The sharp increase in loss due to distance can be alleviated by using larger NA lenses.

First, the 200-μm high VCSEL chip is mounted on the designated 1.45-μm deep grooves on the Ge substrate via UV-curing non-conducting epoxy. After the stability and the flatness of the VCSEL chip array is ensured, silver conducting epoxy is placed at the bottom edges of the VCSEL chip to provide a low resistance ground contact. The VCSEL and PDs are 0.75 cm apart, and both are wirebonded to the 1-mm long 50-Ω transmission lines on the Ge substrate. Then, a 380-μm thick fused silica spacer layer is placed on the Ge substrate and glued via UV-curing to provide a large enough gap between bondwires on the chip and the microlens layer. Finally, the fused silica chip is aligned to the carrier chip and glued using non-conductive epoxy. For measurement purposes, the outer ends of the 1-mm long transmission lines in the 3-D integrated chip are wirebonded to a PCB with RF connectors. This prototype chip is mounted on an optical test bench with a prism which functions like two face-to-face mirrors with a 45 degree angle.

4. MEASUREMENT RESULTS OF FSOI LINK

After the prototype is assembled, dc and small-signal measurements are performed to characterize the FSOI link. In the dc measurements, the transmitted optical power of a single link is measured with respect to transmission distance. Note that in this prototype, the distance between the VCSEL chip and PDs is fixed at 0.75 cm. Therefore, the prism is moved away from the surface of the fused silica to change the transmission distance. The crosstalk power between two adjacent links is also measured.

The electrical-to-electrical current gain of the link is measured using a network analyzer, e.g., -27 dB at 1.4-cm distance, which is used to extract the optical transmission based on the VCSEL slope efficiency and PD responsivity. As shown in Fig. 10-a, the optical link achieves 4-dB optical transmission loss at 0.8-mW VCSEL optical power and 1-cm distance. The optical transmission loss increases to 5 dB and 8 dB at 1.4 and 2-cm distance. The crosstalk with the adjacent link is -23 dB at 1 cm and -16 dB at 2 cm. The microlenses and focal lengths for the link are designed and optimized for 1.4 cm; therefore, the transmission loss is less than 6 dB at distances below 15 mm. Beyond this distance, optical loss and crosstalk between adjacent links increase due to the larger beam size. The loss is 2.5 dB higher than the calculated values, primarily due to the surface roughness of the microlenses.

The measured small-signal bandwidth of the optical link at 5-V PD bias is 3.3 GHz with a 5.1-mW total power consumption (Fig. 10-b). The bandwidth does not show any discrepancy when the PD is biased at 7 V, because it is primarily limited by the VCSEL bandwidth and the bondwires from the chip to the PCB.

5. CONCLUSION

This paper demonstrated a new intra-chip free-space optical interconnect (FSOI) system. The FSOI system achieves low loss, low latency, large bandwidth and large energy efficiency for future many-core chips. The first 3-D integrated chip-scale prototype with a 1×1-cm^2 area is designed based on real-world optical and photonic device parameters. MSM PDs are fabricated on a Ge carrier chip, and GaAs VCSELs and fused silica micro-lenses are 3-D integrated on the Ge carrier. The prototype achieves 4-dB optical loss, -23-dB crosstalk, and 3.3-GHz small signal bandwidth at a 1-cm transmission distance. Optical loss increases slightly to 5 dB with -21-dB crosstalk when the distance increases to 1.4 cm.

Acknowledgment

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