Estimation of On-Chip Simultaneous Switching Noise on Signal Delay in Synchronous CMOS Integrated Circuits

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Abstract—**On-chip parasitic inductance inherent to the power distribution network has becoming significant in high speed digital circuits. Therefore, current surges result in voltage fluctuations within the power distribution network, creating delay uncertainty. On-chip simultaneous switching noise should therefore be considered when estimating the propagation delay of a CMOS logic gate in high speed synchronous CMOS integrated circuits.**

I. Introduction

As the operating frequency increases, the average on-chip current required to charge (and discharge) total load capacitance also increases, while the time during which the current is switched decreases [1]. Therefore, a large change of the on-chip current occurs within a short period of time. The primary sources of the on-chip current surges are those logic gates that switch close in time to the clock edges in a synchronous CMOS integrated circuit. Because of the non-negligible parasitic inductance inherent to the on-chip power distribution network, large current surges result in voltage fluctuations in the power distribution network [2]. These voltage fluctuations are called on-chip simultaneous switching noise (SSN).

On-chip simultaneous switching noise affects the signal delay, creating delay uncertainty since the power supply level temporally changes the local drive current [3, 4]. Furthermore, logic malfunctions may be created and excess power may be dissipated due to faulty switching if the power supply fluctuations are sufficiently large [5]. A modified tapered buffer design technique is presented by Vemuru in [4] which considers the delay uncertainty caused by off-chip simultaneous switching noise. In addition to the many constraints encountered in the design of on-chip clock and power distribution networks, on-chip simultaneous switching noise should be considered when estimating the propagation delay of a logic gate in a synchronous CMOS integrated circuit [6].

II. On-Chip Simultaneous Switching Noise

An analytical expression characterizing the on-chip simultaneous switching noise voltage at the ground rail is developed in this section for a high-to-low output transition. $L_{V_{ss}}$, $R_{V_{ss}}$, and $C_{V_{ss}}$ are the parasitic inductance, resistance, and capacitance of the ground rail, respectively, as shown in Fig. 1. In order to develop an analytical expression characterizing the on-chip simultaneous switching noise on the ground rail, the short-circuit current is neglected based on an assumption of a fast ramp input signal,

$$V_{in}(t) = \frac{t}{\tau_r} V_{dd} \quad \text{for} \quad 0 \le t \le \tau_r. \tag{1}$$

Once the input voltage exceeds the threshold voltage of an NMOS transistor, the NMOS transistor turns ON and is assumed to operate in the saturation region during the input transition. The current through the NMOS transistor (I_N), the parasitic inductance (I_L), and the simultaneous switching noise voltage (V_s) are given, respectively, as

$$I_N = B_n(V_{in} - V_{TN} - V_s)^n, \tag{2}$$

$$I_L = mI_N - C_{V_{ss}} \frac{dV_s}{dt}, \tag{3}$$

$$V_s = R_{V_{ss}} I_L + L_{V_{ss}} \frac{dI_L}{dt}, \tag{4}$$

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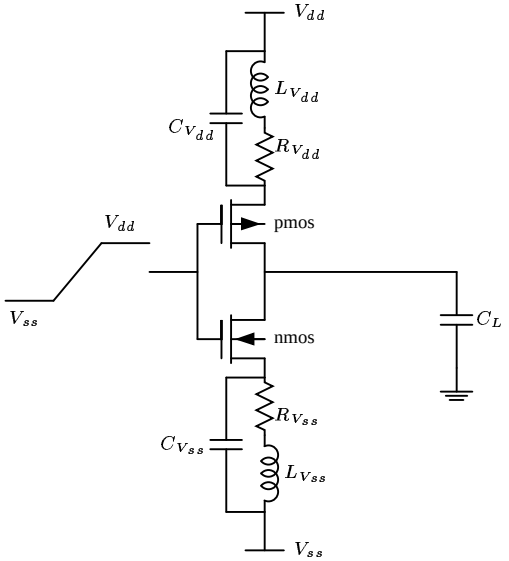

Fig. 1. Equivalent circuit for analyzing on-chip simultaneous switching noise

where m is the number of simultaneously switching logic gates and B_n is the transconductance of the NMOS transistor. Assuming that the magnitude of V_s is small as compared to $V_{in} - V_{TN}$, I_N can be approximated as

$$I_N \approx B_n(V_{in} - V_{TN})^n - \frac{dI_N}{dV_{GS}} V_s. \tag{5}$$

Rewriting (5),

$$f_1 = \frac{dI_N}{dV_{GS}} = nB_n(V_{in} - V_{TN} - V_s)^{n-1}. \tag{6}$$

f_1 is a function of V_{GS} (V_{in} for the case of an inverter). In order to simplify the derivation, f_1 is approximated using V_{in} equal to $0.5\ V_{dd}$.

No closed form solution of these differential equations exists due to the non-integer value of n and $n-1$. In order to derive an analytical expression for these differential equations, $(\frac{t}{\tau_r} - \frac{V_{TN}}{V_{dd}})^n$ and $(\frac{t}{\tau_r} - \frac{V_{TN}}{V_{dd}})^{n-1}$ are approximated by a polynomial expansion to the fifth order, where the average error is less than 3%. The solution of the simultaneous switching noise voltage in this region, $\tau_n \le t \le \tau_r$, is [7]

$$V_s(t) = c_0[1 - e^{-\tau_1(t-\tau_n)}] + c_1\xi + c_2\xi^2 + c_3\xi^3 + c_4\xi^4 + c_5\xi^5 \tag{7}$$

where $\tau_1 = \frac{1}{\gamma\tau_r}$, $\gamma = \frac{R_{V_{ss}}C_{V_{ss}} + L_{V_{ss}} f_{1,m}}{(R_{V_{ss}} f_{1,m} + 1)\tau_r}$, $f_{1,m} = mnB_n(0.5V_{dd} - V_{TN})^{(n-1)}$, and $\xi = (\frac{t}{\tau_r} - \frac{V_{TN}}{V_{dd}})$. The on-chip simultaneous switching noise voltage reaches a maximum when the input voltage completes the transition, *i.e.*, at $t = \tau_r$.

The NMOS transistor is assumed to remain saturated after the input transition is completed. The on-chip simultaneous switching noise voltage in this region, $\tau_r \leq t \leq \tau_{sat}$, can be expressed as

$$V_s(t) = V_{s,1} + [V_s(\tau_r) - V_{s,1}]e^{-\tau_2(t-\tau_r)}, \quad (8)$$

where

$$V_{s,1} = \frac{mB_nR_{Vss}(V_{dd} - V_{TN})^n}{R_{V_{ss}}f_{2,m} + 1}, \quad (9)$$

$$\tau_2 = \frac{R_{V_{ss}}f_{2,m} + 1}{R_{V_{ss}}C_{V_{ss}} + L_{V_{ss}}f_{2,m}}, \quad (10)$$

$$f_{2,m} = mnB_n(V_{dd} - V_{TN} - V_s(\tau_r))^{(n-1)}. \quad (11)$$

After τ_{sat}, the NMOS transistor operates in the linear region. In order to derive a tractable expression, the drain-to-source current is approximated by $\gamma_n V_{DS}$, where γ_n is the effective output conductance of the NMOS transistor. The on-chip simultaneous switching noise voltage in this region is

$$V_s(t) = K_1e^{-\frac{\beta_1 t}{2}} + K_2e^{-\frac{\beta_2 t}{2}} \quad \text{for} \quad t \geq \tau_{sat}, \quad (12)$$

where $\beta_1 = B_1 + \sqrt{B_1^2 - 4B_2}$, $\beta_2 = B_1 - \sqrt{B_1^2 - 4B_2}$, and

$$B_1 = \frac{mR_{V_{ss}}C_L + R_{V_{ss}}C_{V_{ss}} + \frac{C_L}{\gamma_n}}{R_{V_{ss}}C_{V_{ss}}\frac{C_L}{\gamma_n} + mL_{V_{ss}}C_L + L_{VssC_{V_{ss}}}}, \quad (13)$$

$$B_2 = \frac{1}{R_{V_{ss}}C_{V_{ss}}\frac{C_L}{\gamma_n} + mL_{V_{ss}}C_L + L_{VssC_{V_{ss}}}}. \quad (14)$$

C_L is the load capacitance. K_1 and K_2 are integration constants and can be determined from $V_s(\tau_{sat})$ and $V_s'(\tau_{sat})$. However, the effective output conductance of an MOS transistor also depends upon the output voltage in the linear region, changing from γ_{nsat} to $2\gamma_{nsat}$ [8]. In order to accurately characterize the on-chip simultaneous switching noise voltage, γ_n is chosen between γ_{nsat} and $2\gamma_{nsat}$. The on-chip simultaneous switching noise voltage can be approximated by forcing the imaginary part to zero [4],

$$V_s(t) = V_s\tau_{sat}e^{-\frac{\beta_3(t-\tau_{sat})}{2}}\frac{cos(\beta_4 t)}{cos(\beta_4\tau_{sat})} \quad \text{for} \quad t \geq \tau_{sat}, \quad (15)$$

where $\beta_3 = B_1$ and $\beta_4 = \sqrt{4B_2 - B_1^2}$.

III. Propagation Delay Model

Analytical expressions characterizing the output voltage and propagation delay of a CMOS logic gate, which include the effect of on-chip simultaneous switching noise, are presented for both a capacitive and resistive-capacitive load. The analytical results are also compared to both an analytical model which does not consider on-chip simultaneous switching noise and SPICE.

A. Capacitive load

Analytical expressions characterizing the output voltage of a CMOS logic gate driving a capacitive load based on an assumption of a fast ramp input signal are listed in Table I, where $f_{1,s} = \frac{f_{1,m}}{m}$ and $f_{2,s} = \frac{f_{2,m}}{m}$. K_3 and K_4 are determined from $V_o(\tau_{sat})$ and $V_o'(\tau_{sat})$. Note that both $\frac{f_{1,s}\tau_r}{C_L}V_{s,2}(t)$ in (16) and $\frac{f_{2,s}}{C_L}V_{s,3}(t)$ in (18) cause the output voltage to drop slowly during a high-to-low output transition. Therefore, the on-chip simultaneous switching noise affects the waveform shape of the output voltage and causes a change in the propagation delay of a CMOS logic gate driving a capacitive load.

The propagation delay of a CMOS logic gates t_P is typically defined as the time from the 50% V_{dd} point of the input to the 50% V_{dd} point of the output. The high-to-low propagation delay of a CMOS logic gate can be determined by (18) or (20) using a Newton-Raphson iteration. Since β_1 is greater than β_2 in (12), the output voltage in this region can be approximated as

$$V_o(t) = V_o(\tau_{sat})e^{-\frac{\beta_2}{2}(t-\tau_{sat})} \quad \text{for} \quad t \geq \tau_{sat}. \quad (21)$$

The drain-to-source saturation voltage is typically greater than $0.5V_{dd}$; therefore, the high-to-low propagation delay can be expressed as

$$t_{P_{HL}} = \frac{2}{\beta_2}ln\frac{2V_o(\tau_{sat})}{V_{dd}} + \tau_{sat} - \frac{\tau_r}{2}. \quad (22)$$

A comparison of the analytical propagation delay expressions with SPICE is listed in Table II for a high-to-low transition. It is demonstrated in Table II that the delay uncertainty caused by on-chip simultaneous switching noise increases with increasing input slew rate, parasitic inductance, and resistance of the power supply rails. The maximum error of the propagation delay based on the analytical expressions is within 5%, as compared to nearly 16% of SPICE when not considering on-chip simultaneous switching noise. The average improvement in accuracy is about 8%.

B. Resistive-capacitive load

In this discussion, the interconnect is modeled as a resistive-capacitive impedance. R_L is the load resistance driven by a CMOS logic gate. Analytical expressions characterizing the output voltage of a CMOS logic gate driving a resistive-capacitive load impedance are listed in Table III where $\beta_5 = B_3 + \sqrt{B_3^2 - 4B_4}$ and $\beta_6 = B_3 - \sqrt{B_3^2 - 4B_4}$. K_5 and K_6 are also determined from $V_o(\tau_{sat})$ and $V_o'(\tau_{sat})$. Both $\frac{f_{1,s}\tau_r}{C_L}V_{s,2}(t)$ in (23) and $\frac{f_{2,s}}{C_L}V_{s,3}(t)$ in (24) cause the output voltage to drop slowly during a high-to-low output transition for a resistive-capacitive load impedance. Therefore, the on-chip simultaneous switching noise affects the waveform shape of the output voltage, increasing the propagation delay of a CMOS logic gate driving a resistive-capacitive load impedance.

Based on the same assumption as for a capacitive load, the output voltage in this region can be approximated as

$$V_o(t) = V_o(\tau_{sat})e^{-\frac{\beta_6}{2}(t-\tau_{sat})} \quad \text{for} \quad t \geq \tau_{sat}. \quad (28)$$

If the drain-to-source saturation voltage is greater than $0.5V_{dd}$, the high-to-low propagation delay can be expressed as

$$t_{P_{HL}} = \frac{2}{\beta_6}ln\frac{2V_o(\tau_{sat})}{V_{dd}} + \tau_{sat} - \frac{\tau_r}{2}. \quad (29)$$

A comparison of the propagation delay based on these analytical expressions with SPICE is listed in Table IV for a high-to-low transition. The estimated propagation delay based on these analytical expressions is within 5%, while the error of the estimate which does not consider on-chip simultaneous switching noise can reach 18%. The average improvement in accuracy is about 10%.

IV. Conclusions

It is necessary to consider on-chip simultaneous switching noise when determining the propagation delay of a CMOS logic gate in a high speed synchronous CMOS integrated circuit. Analytical expressions characterizing on-chip simultaneous switching noise are presented in this paper. The effects of on-chip simultaneous switching noise on the waveform of the output voltage and the propagation delay of a CMOS logic gate are also discussed. The estimated propagation delay based on these analytical expressions is within 5% as compared to SPICE; the average improvement can reach 10% as compared to delay estimates

TABLE I

ANALYTICAL EXPRESSIONS CHARACTERIZING THE OUTPUT VOLTAGE OF A CMOS INVERTER DRIVING A CAPACITIVE LOAD

Operating region	Analytical expressions
$[\tau_n, \tau_r]$	$V_o(t) = V_{dd} - \frac{B_n \tau_r V_{dd}^n}{(n+1)C_L}\xi^{(n+1)} + \frac{f_{1,s}\tau_r}{C_L}V_{s,2}(t)$ (16) $V_{s,2}(t) = (\xi + \frac{e^{-\tau_1 \xi}}{\tau_1})c_0 + \frac{c_1}{2}\xi^2 + \frac{c_2}{3}\xi^3 + \frac{c_3}{4}\xi^4 + \frac{c_4}{5}\xi^5 + \frac{c_5}{6}\xi.$ (17)
$[\tau_r, \tau_{sat}]$	$V_o(t) = V_o(\tau_r) - \frac{B_n}{C_L}(V_{dd} - V_{TN})^n (t - \tau_r) + \frac{f_{2,s}}{C_L}V_{s,3}(t)$ (18) $V_{s,3}(t) = V_{s,1}(t - \tau_r) + \frac{V_s(\tau_r) - V_{s,1}}{\tau_2}(1 - e^{-\tau_2 (t - \tau_r)})$ (19)
$t \geq \tau_{sat}$	$V_o(t) = K_3 e^{-\frac{\beta_1 t}{2}} + K_4 e^{-\frac{\beta_2 t}{2}}$ (20)

TABLE II

COMPARISON OF HIGH-TO-LOW PROPAGATION DELAY WITH SPICE FOR A CMOS INVERTER DRIVING A CAPACITIVE LOAD INCLUDING THE EFFECTS OF ON-CHIP SIMULTANEOUS SWITCHING NOISE

Input Rise Time	Impedance of Ground Rail			Comparison of Propagation Delay				
				Simulation	Analytic Estimation			
τ_r	L	R	C	SPICE	Without SSN		With SSN	
(ps)	(nH)	(Ω)	(pF)	(ps)	(ps)	% Error	(ps)	% Error
200	1.0	5.0	0.1	182	172	5.5	183	1.1
		10.0	0.1	186	172	7.5	183	1.6
		15.0	0.1	190	172	9.5	186	2.1
		20.0	0.1	194	172	11.3	189	2.6
	2.0	5.0	0.1	186	172	7.5	183	1.6
		10.0	0.1	190	172	9.5	186	2.1
		15.0	0.1	194	172	11.3	189	2.6
		20.0	0.1	198	172	13.1	192	3.0
	3.0	5.0	0.1	191	172	10.0	187	2.1
		10.0	0.1	195	172	11.8	190	2.6
		15.0	0.1	199	172	13.6	192	3.5
		20.0	0.1	203	172	15.3	195	3.9
150	1.0	5.0	0.1	175	166	5.1	174	0.6
		10.0	0.1	180	166	7.7	177	1.7
		15.0	0.1	184	166	9.8	180	2.2
		20.0	0.1	189	166	12.2	183	3.2
	2.0	5.0	0.1	179	166	7.3	177	1.1
		10.0	0.1	184	166	9.7	180	2.2
		15.0	0.1	188	166	11.7	183	2.7
		20.0	0.1	193	166	14.0	185	4.1
	3.0	5.0	0.1	185	166	10.3	180	2.7
		10.0	0.1	188	166	11.7	182	3.2
		15.0	0.1	193	166	14.0	185	4.1
		20.0	0.1	197	166	15.7	188	4.6
Maximum error (%)					15.7		4.6	
Average error (%)					10.63		2.25	

which do not consider on-chip simultaneous switching noise. The analytical expressions presented in this paper provide an accurate timing model for repeater insertion, tapered buffer design, and related high performance design techniques for those high speed synchronous CMOS integrated circuits where on-chip simultaneous switching noise cannot be neglected.

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TABLE III

ANALYTICAL EXPRESSIONS CHARACTERIZING THE OUTPUT VOLTAGE OF A CMOS INVERTER DRIVING A RESISTIVE-CAPACITIVE LOAD

Operating region	Analytical expressions
$[\tau_n, \tau_r]$	$V_o(t) = V_{dd} - \frac{B_n \tau_r V_{dd}^n}{(n+1)C_L}\xi^{(n+1)} - R_L B_n V_{dd}^n \xi^n + \frac{f_{1,s}\tau_r}{C_L}V_{s,2}(t)$ (23)
$[\tau_r, \tau_{sat}]$	$V_o(t) = V_o(\tau_r) - \frac{B_n}{C_L}(V_{dd} - V_{TN})^n (t - \tau_r) + \frac{f_{2,s}}{C_L}V_{s,3}(t)$ (24)
$t \geq \tau_{sat}$	$V_o(t) = K_5 e^{-\frac{\beta_5 t}{2}} + K_6 e^{-\frac{\beta_6 t}{2}}$ (25) $B_3 = \frac{mR_{V_{ss}}C_L + R_{V_{ss}}C_{V_{ss}} + \frac{C_L(1+R_L\gamma_n)}{\gamma_n}}{R_{V_{ss}}C_{V_{ss}}\frac{C_L(1+R_L\gamma_n)}{\gamma_n} + mL_{V_{ss}}C_L + L_{Vss}C_{V_{ss}}}$ (26) $B_4 = \frac{1}{R_{V_{ss}}C_{V_{ss}}\frac{C_L(1+R_L\gamma_n)}{\gamma_n} + mL_{V_{ss}}C_L + L_{Vss}C_{V_{ss}}}$ (27)

TABLE IV

COMPARISON OF HIGH-TO-LOW PROPAGATION DELAY WITH SPICE FOR A CMOS INVERTER DRIVING A RESISTIVE-CAPACITIVE LOAD INCLUDING THE EFFECTS OF ON-CHIP SIMULTANEOUS SWITCHING NOISE

Input Rise Time	Impedance of Ground Rail			Comparison of Propagation Delay				
				Simulation	Analytic Estimation			
τ_r	L	R	C	SPICE	Without SSN		With SSN	
(ps)	(nH)	(Ω)	(pF)	(ps)	(ps)	% Error	(ps)	% Error
200	1.0	5.0	0.1	163	152	6.7	162	0.6
		10.0	0.1	167	152	9.0	165	1.2
		15.0	0.1	172	152	11.6	168	2.3
		20.0	0.1	176	152	13.6	171	2.8
	2.0	5.0	0.1	167	152	9.0	165	1.2
		10.0	0.1	171	152	11.1	168	1.8
		15.0	0.1	176	152	13.6	171	2.8
		20.0	0.1	180	152	15.6	174	3.3
	3.0	5.0	0.1	172	152	11.6	169	1.7
		10.0	0.1	176	152	13.6	172	2.3
		15.0	0.1	180	152	15.6	175	2.8
		20.0	0.1	184	152	17.4	177	3.8
150	1.0	5.0	0.1	157	146	7.0	156	0.6
		10.0	0.1	162	146	9.9	159	1.9
		15.0	0.1	166	146	12.0	162	2.4
		20.0	0.1	170	146	14.1	165	2.9
	2.0	5.0	0.1	161	146	9.3	159	1.2
		10.0	0.1	165	146	11.5	162	1.8
		15.0	0.1	170	146	14.1	165	2.9
		20.0	0.1	174	146	16.1	168	3.4
	3.0	5.0	0.1	166	146	12.0	162	2.4
		10.0	0.1	170	146	14.1	165	2.9
		15.0	0.1	174	146	16.1	168	3.4
		20.0	0.1	170	146	18.0	170	4.5
Maximum error (%)					18.0		4.5	
Average error (%)					12.61		2.38	