Speed and Noise Immunity Enhanced Low Power Dynamic Circuits

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Abstract — **Four different dynamic circuit techniques are proposed in this paper for lowering the active mode power consumption, increasing the speed, enhancing the noise immunity, and reducing the subthreshold leakage energy of domino logic circuits. A variable threshold voltage keeper circuit technique is proposed for simultaneous power reduction and speed enhancement of domino logic circuits. The threshold voltage of the keeper transistor is dynamically modified during circuit operation to reduce contention current without sacrificing noise immunity. The variable threshold voltage keeper circuit technique enhances circuit evaluation speed by up to 60% while reducing power dissipation by 35% as compared to a standard domino logic circuit. The keeper size can be increased with the proposed technique while preserving the same delay or power characteristics as compared to a standard domino circuit. The proposed domino logic circuit technique offers 14% higher noise immunity as compared to a standard domino circuit with the same evaluation delay characteristics.**

Forward body biasing the keeper transistor is also proposed for improved noise immunity as compared to a standard domino circuit with the same keeper size. It is shown that by applying forward and reverse body biased keeper circuit techniques, the noise immunity and evaluation speed of domino logic circuits are simultaneously enhanced.

A low swing domino logic technique is proposed to decrease the dynamic switching power without sacrificing noise immunity. With the proposed low swing domino logic circuit technique, active power consumption is reduced by up to 9.4% as compared to standard domino logic circuits. It is also shown that by applying a low swing contention reduction technique, the power savings can be further increased by 6.7% while the delay can be improved by 8.6%.

A circuit technique is proposed for reducing the standby leakage energy of domino logic circuits. The proposed circuit technique also enhances the delay and power characteristics of a domino circuit operating in the active mode. Sleep switch transistors are proposed to place an idle dual threshold voltage domino logic circuit into a low leakage state. The proposed circuit technique reduces the leakage energy by up to 207 times as compared to a standard low threshold voltage domino circuit. The sleep switch circuit technique exploits the full effectiveness of employing dual threshold voltage transistors to reduce the subthreshold leakage current by strongly turning off all of the high threshold voltage transistors. The proposed circuit technique reduces the leakage energy by up to 58 times as compared to a standard dual threshold voltage domino circuit. With the proposed circuit technique, a domino adder enters and leaves the standby mode within a single clock cycle. The energy overhead of the sleep switch circuit technique is low, justifying the activation of the proposed sleep scheme during idle periods as short as 539 clock cycles.

I. INTRODUCTION

Domino logic circuit techniques are extensively applied in high performance microprocessors due to the superior speed and area characteristics of domino CMOS circuits as compared to static CMOS circuits [1]-[4]. High speed operation of domino logic circuits is primarily due to the lower noise margins of domino circuits as compared to static gates. This desirable property of a lower noise margin, however, makes domino logic circuits highly sensitive to noise as compared to static gates. As on-chip noise becomes more severe with technology scaling and increasing operating frequencies, error free operation of domino logic circuits has become a major challenge [1]-[5].

Dynamic switching energy, the dominant component of the total energy consumed in current CMOS technologies, is quadratically reduced by lowering the supply voltage. Lowering the supply voltage, however, also degrades the circuit speed due to reduced transistor currents. The threshold voltages are scaled in order to reduce the degradation in speed caused by supply voltage scaling while maintaining the dynamic power consumption within acceptable levels [1]-[5]. Scaling the threshold voltage, however, degrades the noise immunity of domino logic gates [1], [5]. Moreover, exponentially increasing subthreshold leakage currents with reduced threshold voltages have become an important issue threatening the reliable operation of deep submicrometer (DSM) dynamic circuits [1]-[5]. Four different circuit techniques are proposed in this paper for enhancing the reliability or lowering the power consumption and evaluation delay of domino logic circuits.

In a standard domino logic gate, a tradeoff exists between reliability and high speed/energy efficient operation due to the contention current of a standard feedback keeper transistor [1], [2], [5]. A variable threshold voltage keeper circuit technique is proposed [1], [2] for simultaneous power reduction and speed enhancement of domino logic circuits. The operation of the proposed domino logic with a variable threshold voltage keeper (DVTVK) is described in Section 2.

Reducing the voltage swing at the output nodes of domino logic circuits is proposed to lower the dynamic switching power [3]. In a domino gate, the input signals are only applied to the NMOS transistors in the pull-down path, while a single pull-up PMOS transistor is driven by a separate clock signal. Therefore, a low swing signal that transitions between ground and a second sufficiently high voltage level to effectively turn on an NMOS transistor does not impose any static power consumption or

functional problems in domino logic circuits [3]. This proposed low swing domino logic circuit technique is presented in Section 3.

At reduced threshold voltages subthreshold leakage currents increase exponentially. The subthreshold leakage power is soon expected to dominate the total power consumed by a CMOS circuit [3], [6], [7]. Energy efficient circuit techniques aimed at lowering the leakage currents are, therefore, highly desirable. A circuit technique is proposed in this paper for lowering the standby leakage energy of a domino logic circuit. The operation of the proposed dual-V_t domino logic technique employing sleep switches (SLS) is described in Section 4. Some conclusions are offered in Section 5.

II. DOMINO LOGIC WITH VARIABLE THRESHOLD VOLTAGE KEEPER

A K input domino OR gate based on the proposed variable threshold voltage keeper (DVTVK) circuit technique [1], [2] is shown in Fig. 1. A representative waveform that characterizes the operation of the circuit is shown in Fig. 2.

The operation of the DVTVK circuit behaves in the following manner. When the clock is low, the pullup transistor is on and the dynamic node is charged to V_{DD1}. The substrate of the keeper is charged to V_{DD2} ($V_{DD2} > V_{DD1}$) by the body bias generator, increasing the keeper threshold voltage. The value of the high threshold voltage (high-V_t) of the keeper is determined by the reverse body bias voltage (V_{DD2} - V_{DD1}) applied to the source-to-substrate p-n junction of the keeper. The current sourced by the high-V_t keeper is reduced, lowering the contention current when the evaluation phase begins. A reduction in the current drive of the keeper does not degrade the noise immunity during precharge as the dynamic node voltage is maintained during this phase by the pullup transistor rather than by the keeper.

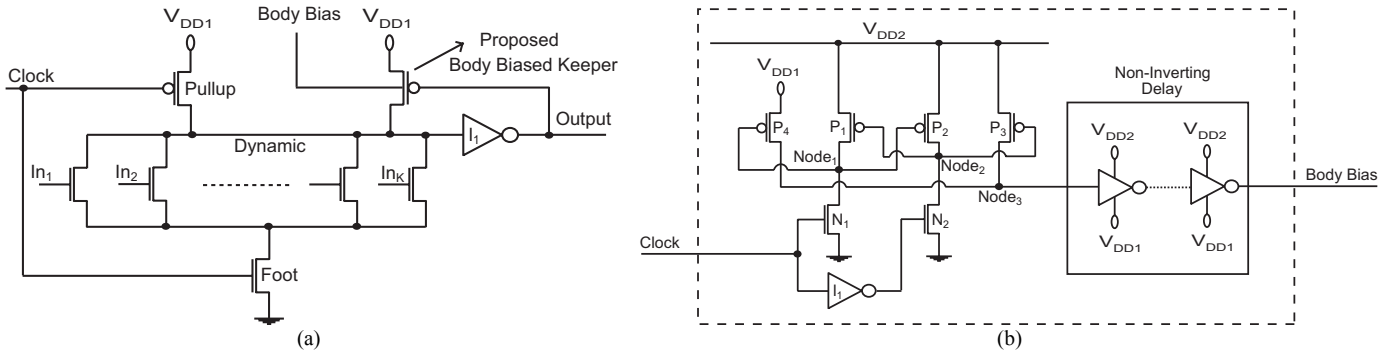

Fig. 1. The proposed variable threshold voltage keeper domino logic circuit technique. (a) A K input domino OR gate with a variable threshold voltage keeper. (b) The dynamic body bias generator.

When the clock goes high (the evaluation phase), the pullup transistor is cutoff and only the high-V_t keeper current contends with the current from the evaluation path transistor(s). Provided that the appropriate input combination that discharges the dynamic node is applied in the evaluation phase, the contention current due to the high-V_t keeper is significantly reduced as compared to standard domino logic. After a delay determined by the worst case evaluation delay of the domino gate, the body bias voltage of the keeper is reduced to V_{DD1}, zero biasing the source-to-substrate p-n junction of the keeper. The threshold voltage of the keeper is lowered to the zero body bias level, thereby increasing the keeper current. The DVTVK keeper has the same threshold voltage of a standard domino (SD) keeper, offering the same noise immunity during the remaining portion of the evaluation phase (assuming the SD and DVTVK keepers are the same size).

Four-bit multiple-output domino carry generators with the DVTVK and SD circuit techniques are compared in terms of the evaluation delay and power dissipation assuming the DVTVK and SD circuits have the same keeper size. The DVTVK technique operates at up to a 60% higher speed while consuming 35% less power as compared to SD. DVTVK also reduces the PDP by up to 74% as compared to SD. A temporary degradation in the noise immunity of DVTVK of less than 11% as compared to SD is observed when the keeper of the DVTVK is reverse body biased.

Since the contention current is significantly reduced with the proposed variable threshold voltage keeper technique, the keeper transistor in a DVTVK circuit can be sized larger, offering higher noise immunity with the same delay and power characteristics as compared to a standard domino logic circuit. The DVTVK and SD circuit techniques are compared in terms of the noise immunity that the two circuit techniques offer with the same evaluation delay, power dissipation, or power-delay product characteristics. For the same evaluation delay characteristics, DVTVK (with a zero biased keeper) offers 14.1% higher noise immunity as compared to SD. Under the same power dissipation conditions, DVTVK (with a zero biased keeper) improves the noise immunity by 8.9% as compared to SD. Similarly, under the same PDP conditions, DVTVK (with a zero biased keeper) offers 11.9% higher noise immunity as compared to SD.

Alternatively, forward body biasing the keeper after the worst case evaluation delay is proposed to improve the noise immunity characteristics as compared to SD. The threshold voltage of a forward body biased MOSFET is reduced, increasing the conduction current as compared to a zero body biased transistor with the same physical dimensions. Forward body biasing the keeper, therefore, improves the noise immunity characteristics as compared to a standard domino logic circuit with the same keeper size. The only difference in the dynamic body bias generator of the domino circuit with a forward biased keeper is that

V_{DD1} (as shown in Fig. 1) is replaced by a smaller supply voltage V_{DD3} ($V_{DD3} < V_{DD1}$). By applying a forward body bias of 0.7 volts to a keeper transistor, the noise immunity of an eight input footless domino OR gate is improved by 12.8% as compared to a standard domino logic circuit with the same keeper size.

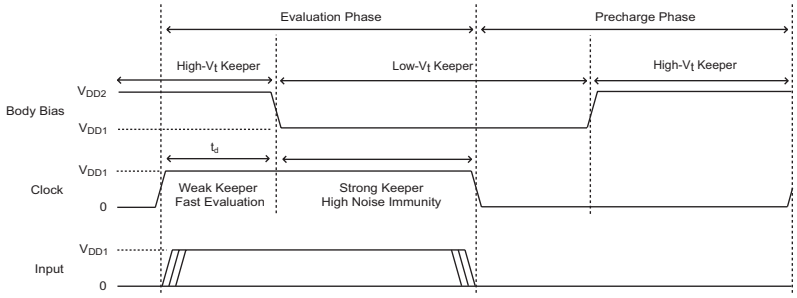

Fig. 2. Waveforms that characterize the operation of the proposed variable threshold voltage keeper circuit technique.

III. LOW SWING DOMINO LOGIC

Low swing circuit techniques are applied to domino logic circuits in order to reduce the dynamic switching power. Two low swing domino logic circuit techniques are proposed [3]. The first proposed low swing domino circuit with a fully driven keeper (LSDFDK) is shown in Fig. 3a. The proposed circuit technique reduces the voltage swing at the output node using the NMOS transistor (N6) as a pull-up transistor. The output voltage swings between ground and V_{DD} - V_{tn}. The keeper (P2) is driven with a full swing signal for improved noise immunity.

A reduced voltage swing keeper gate drive technique is proposed to improve the delay and power characteristics of domino circuits while maintaining robustness against noise. The second proposed low swing domino logic circuit with a weak keeper (LSDWDK) is shown in Fig. 3b. This technique reduces the contention current by lowering the gate voltage swing of a keeper transistor. The weak keeper is critical in low swing circuits since the effects of the contention current on the evaluation delay is worse due to the reduced gate drive of the pull-down network transistors. LSDWDK produces two different voltage swings. The output voltage swing is between ground and V_{DD} - V_{tn}. The gate voltage swing of the keeper (P2) is also modified. The gate voltage of P2 swings between $|V_{tp}|$ and V_{DD} (assuming $|V_{tp}| \leq V_{tn}$).

The proposed low swing domino logic circuits with fully driven keeper lower the active mode dynamic switching power by up to 9.4% and tolerate up to 2.6% more noise as compared to standard domino [3]. The proposed low swing domino logic circuits with a weakly driven keeper reduce the active mode dynamic switching power consumption by up to 12.4% as compared to standard domino [3].

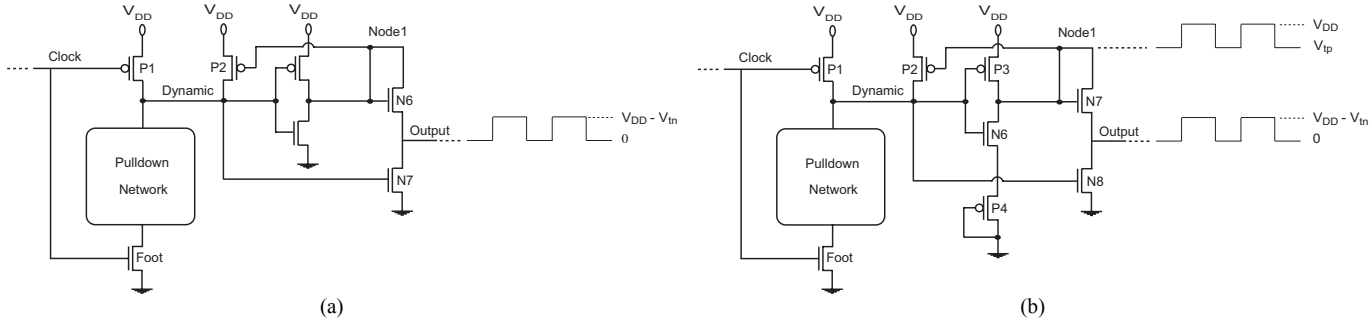

Fig. 3. The proposed low swing domino logic circuits. (a) Low swing domino with fully driven keeper (LSDFDK). (b) Low swing domino with weakly driven keeper (LSDWDK).

IV. SLEEP SWITCH DUAL THRESHOLD VOLTAGE DOMINO LOGIC

A low energy and delay overhead circuit technique is proposed to lower the subthreshold leakage currents in an idle domino logic circuit. The proposed circuit technique employs sleep switches to place a dual-V_t domino logic circuit into a low leakage state within a single clock cycle. Domino gates with the low-V_t, standard no-sleep dual-V_t, and sleep switch (SLS) circuit techniques are shown in Fig. 4.

A high-V_t NMOS switch is added to the dynamic node of a domino circuit as shown in Fig. 4c. The operation of this transistor is controlled by a separate sleep signal. During the active mode of operation, the sleep signal is set low, the sleep switch is cut-off, and the proposed dual-V_t circuit operates as a standard dual-V_t domino circuit. During the standby mode of operation, the clock signal is maintained high, turning off the high-V_t pull-up transistor of each domino gate. The sleep signal transitions high, turning on the sleep switch. The dynamic node of the domino gate is discharged through the sleep switch, thereby turning off the

high-V_t NMOS transistor within the output inverter. The output transitions high, cutting off the high-V_t keeper. After a sleep switch dual-V_t domino gate is forced to evaluate, the following gates (fed by the non-inverting signals) also evaluate in a domino fashion. After the node voltages settle to a steady state, all of the high-V_t transistors in the proposed circuit are strongly cut-off, significantly reducing the subthreshold leakage current. Note that this technique, requiring no additional gating on the input signals while strongly turning off all of the high-V_t transistors within a single clock cycle, is significantly more power, delay, and area efficient as compared to the techniques proposed in [6] and [7].

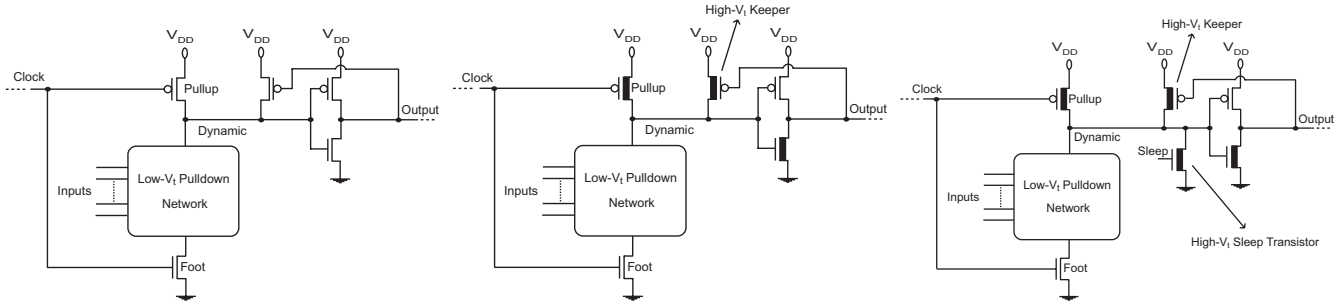

Fig. 4. Domino gates with the low-V_t, standard no-sleep dual-V_t, and sleep switch (SLS) circuit techniques. (a) Low-V_t domino gate. (b) Standard no-sleep dual-V_t domino gate. (c) Sleep switch (SLS) domino gate.

Eight-bit clock-delayed-domino carry-look-ahead adders based on the low-V_t, standard no-sleep dual-V_t, and sleep switch circuit techniques are evaluated. The sleep switch circuit technique reduces the leakage energy by up to 207 times as compared to a standard low-V_t circuit. The proposed circuit technique also reduces the active mode delay and power by up to 32% and 14%, respectively, as compared to a low-V_t circuit.

The sleep switch circuit technique exploits the full effectiveness of the dual-V_t transistors to reduce the subthreshold leakage current by strongly cutting off all of the high-V_t transistors. The sleep switch circuit technique reduces the leakage energy by up to 58 times as compared to a standard dual-V_t circuit. The energy overhead of the sleep switch circuit technique is low, justifying the use of the proposed scheme during idle periods as short as 539 clock cycles in order to lower the standby leakage energy.

V. CONCLUSIONS

A high speed, low power domino logic circuit technique is proposed. The proposed technique dynamically changes the threshold voltage of the keeper with a specific delay after the beginning of each operational phase (evaluation and precharge) of the domino circuit by varying the body bias voltage of the keeper transistor. Significant enhancements in speed and reductions in power are achieved when the keeper is sized for increased noise immunity.

Forward body biasing the keeper transistor is proposed to improve the noise immunity as compared to a standard domino circuit with the same keeper size. By dynamically forward and reverse body biasing the keeper transistor, the noise immunity, evaluation speed, power dissipation, and PDP characteristics of a domino logic circuit are simultaneously enhanced.

Low swing domino logic circuits with weakly driven keepers and fully driven keepers are proposed for power savings during the active mode of operation. The proposed low swing domino logic circuits can significantly reduce the active mode dynamic switching power consumption without degrading the noise immunity.

A circuit technique is proposed for minimizing the subthreshold leakage energy of domino logic circuits. The proposed circuit technique employs sleep switches and the selective placement of high threshold voltage transistors along the non-critical precharge paths in order to place an idle domino logic circuit into a low leakage state. The energy overhead of the sleep switch circuit technique is low, justifying the use of the proposed scheme during idle periods as short as 539 clock cycles in order to lower the standby leakage energy.

VI. REFERENCES

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