Predictions, Challenges, and Opportunities in CMOS Compatible On-Chip Optical Interconnect

Eby G. Friedman
Department of Electrical and Computer Engineering
University of Rochester, Rochester, New York 14627

***Abstract*— On-chip optical interconnect has been considered as a potential substitute for electrical interconnect. Predictions of the performance of CMOS compatible optical devices are made based on current state-of-art optical technologies. Based on these predictions, electrical and optical interconnects are compared for delay uncertainty, latency, power, and bandwidth density.**

I. Introduction

In deep submicrometer VLSI technologies, it has become increasingly difficult for conventional copper based electrical interconnect to satisfy the design requirements of delay, power, bandwidth, and delay uncertainty. One promising candidate to solve this problem is optical interconnect [1]. A comprehensive comparison between optical and electrical interconnects is described in this paper for different technology nodes. The paper is organized as follows. In section II, a delay-optimal design of RLC interconnect is presented. In section III, predictions of the performance characteristics of next generation optical devices are made based on current technology trends. In section IV, electrical and optical interconnect are evaluated for different design criteria. Some conclusions are offered in section V.

II. Scaling of Electrical Interconnect

The delay model of an RLC interconnect with repeaters described in [2] is used for the electrical interconnect analysis [3]. Three degrees of freedom (the wire width, and the number and size of the repeaters) are explored in the electrical interconnect design process to achieve the minimum delay. The minimum delay per unit length is approximately in the range of 20 to 22 ps/mm for all of the technology nodes of interest.

III. On-Chip Optical Data Path

Introducing optical interconnects into VLSI circuits requires compatibility with CMOS technology. Due to the absence of an efficient silicon-based laser, only those configurations that utilize an external laser as a light source are considered. A diagram of an optical interconnect system is shown in Fig. 1. Considering compatibility with a CMOS technology, a practical solution is a 1.5 μm wavelength light source with a silicon modulator and a SiGe or Ge photo-detector. Unlike electrical devices, optical devices are not readily scalable due to the light wavelength constraint. The performance and integration ability of optical devices, however, are expected to be further improved by technology inventions and structural optimization.

A transmitter is composed of an electro-optical modulator and a driver circuit. The design of a fast and cost efficient CMOS compatible electro-optical modulator is one of the most challenging tasks on the path towards realizing on-chip optical interconnects.

This research was supported by the National Science Foundation under Contract No. CCR-0304574.

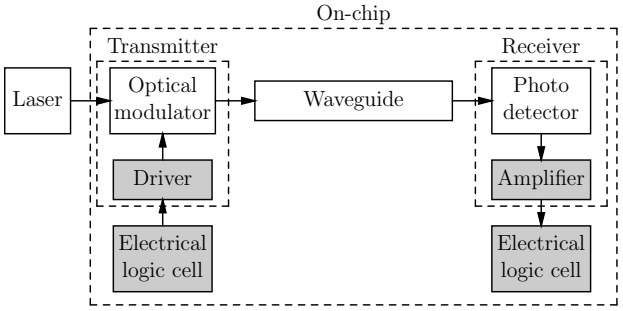

Fig. 1. An on-chip optical interconnect data path.

For a specific operating wavelength of $1.5\,\mu m$, low refractive index strip polymer waveguides are assumed with a core cross section of 1.5 μm$\times$1.5 μm. The core index and cladding index are 1.6 and 1.1, respectively. The mode effective index is 1.48.

The receiver has two components: a photo-detector and an amplifier. Interdigitated SiGe p-i-n or metal semiconductor metal (MSM) detectors are considered due to the fast response and reasonable quantum efficiency of these structures. The performance of future detectors is projected based on a model proposed by Averine *et al.* [4]. The detector response time is expected in the near future to drop significantly, from tens of picoseconds to a few picoseconds.

IV. Electrical vs. optical interconnects

Different criteria used in the design of the two interconnect systems described in sections II and III are compared, including delay uncertainty, latency, power dissipation, and bandwidth density. The interconnect length is 10 mm.

Delay uncertainty is caused by geometric process variations and environmental changes. Variations in the environment include power/ground noise, temperature fluctuations, and crosstalk coupling. All of the variations are assumed to be random with a normal distribution. The delay and 3σ value for different parts of a 1 cm optical data path are listed in Table I. A comparison of the standard deviation of the delay of the electrical and optical interconnect is shown in Fig. 2. The delay uncertainty of the optical interconnect is expected to be lower in future technology nodes. The delay uncertainty of the electrical interconnect, in contrast, is expected to slowly increase in future technology nodes due to the greater number of repeaters.

For data to be correctly latched at the receiving register, certain setup and hold constraints should be satisfied. The delay uncertainty is assumed to not exceed 80% of the clock period. Since no register-like device can be inserted into an optical data path, the delay uncertainty provides an upper bound on the optical channel bandwidth. As listed in Table II, the delay of the electrical interconnect remains approximately fixed for all technology nodes. The delay of the optical

TABLE I

DELAY AND 3σ VALUE OF A 1 cm OPTICAL DATA PATH.

Tech. node	90 nm		65 nm		45 nm		32 nm		22 nm	
	Delay (ps)	3σ (%)	Delay (ps)	3σ (%)	Delay (ps)	3σ (%)	Delay (ps)	3σ (%)	Delay (ps)	3σ (%)
Mod. driver	37.3	20.9	26.5	20.4	16.6	23.5	10.3	29.1	5.2	40.4
Modulator	40.0	67.0	40.0	51.0	40.0	41.0	40.0	32.0	40.0	27.0
Waveguide	49.3	1.1	49.3	0.8	49.3	0.5	49.3	0.2	49.3	0.1
Detector	2.5	5.6	1.1	21.9	0.6	14.1	0.5	9.3	0.4	7.1
Amplifier	34.0	10.6	13.5	23.8	8.7	17.6	5.7	15.8	3.4	15.0
Total optical	163.1	17.3	130.4	16.4	115.2	14.7	105.8	12.5	98.3	11.2

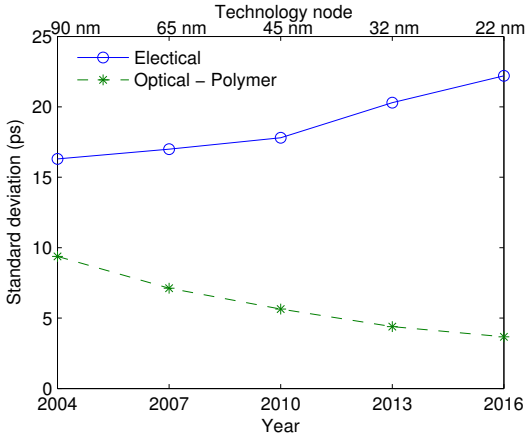

Fig. 2. Comparison of standard deviation of delays of electrical and optical interconnects.

interconnect, however, decreases with future technology nodes due to the higher performance of the electrical circuits in the modulator driver and receiver amplifier.

The power dissipated by the electrical and optical interconnect is compared in Table III. In optical interconnect, the power consumed by the transmitter dominates the power of the receiver. Both the electrical and optical interconnect power increases due to higher clock frequencies and greater leakage current.

Bandwidth density is an effective criterion for evaluating the ability to transmit data through a unit width. The maximum bit rate for a single interconnect is assumed to be the clock rate. Requiring the waveguide size to be larger than the optical mode size, the waveguide pitch is assumed to be 4 μm. Single wavelength optical interconnects are not beneficial if high bandwidth density is desired. The bandwidth of optical interconnects, however, can be significantly improved by introducing wavelength division multiplexing (WDM). The bandwidth density of several interconnects is compared in Fig. 3. For optical interconnect with WDM, the channel number in a waveguide is assumed to be one (1) at the 90 nm technology node, and to increase by four for each new technology node.

The critical length beyond which optical interconnect exceeds the performance of electrical interconnect is plotted in Fig. 4 for different design criteria. The lengths are normalized to the edge of the chip die dimension. The critical length is approximately one tenth of the chip edge length at the 22 nm technology node.

V. CONCLUSIONS

A prediction of the performance characteristics of future CMOS compatible optical devices is described. Based on this prediction, electrical and optical on-chip interconnects are compared for various design criteria at different technology nodes. Critical lengths beyond which optical interconnect becomes advantageous are presented. These lengths are well below expected chip die size dimensions.

TABLE II

DELAY (ps) OF ELECTRICAL AND OPTICAL INTERCONNECTS.

Technology node	90 nm	65 nm	45 nm	32 nm	22 nm
Electrical	311.9	313.2	291.3	312.0	317.8
Optical	238.9	173.3	145.4	127.7	114.9

TABLE III

POWER (mW) OF OPTICAL AND ELECTRICAL INTERCONNECTS.

Technology node	90 nm	65 nm	45 nm	32 nm	22 nm
Transmitter	0.9	1.9	3.4	5.9	11.2
Receiver	0.5	0.5	0.3	0.3	0.3
Total optical	1.4	2.4	3.7	6.2	11.5
Electrical	9.8	16.9	21.7	33.4	45.3

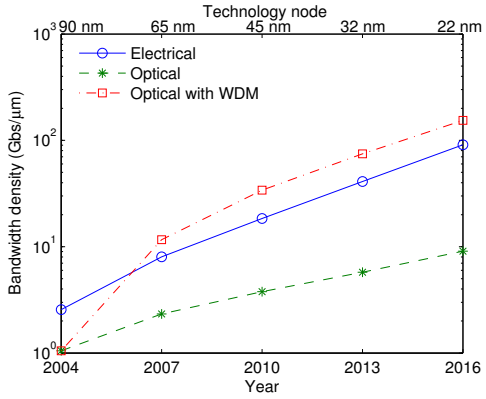

Fig. 3. Bandwidth density of electrical and optical interconnects.

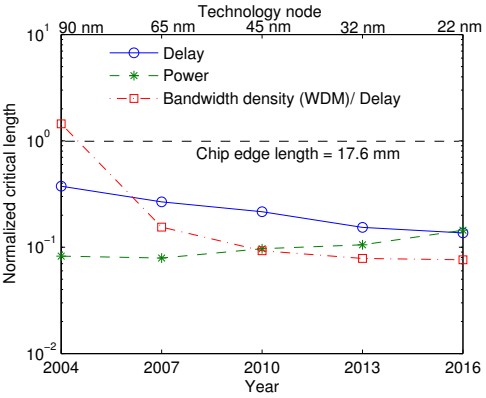

Fig. 4. Normalized critical length beyond which optical interconnect is advantageous over electrical interconnect.

ACKNOWLEDGMENTS

The author would like to acknowledge G. Chen, H. Chen, M. Haurylau, N. A. Nelson, D. H. Albonesi, and P. M. Fauchet for these research results.

REFERENCES

[1] P. Kapur, *Scaling Induced Performance Challenges/Limitations of On-Chip Metal Interconnects and Comparisons with Optical Interconnects*, Ph.D. Thesis, Stanford University, Stanford, California, 2002.

[2] G. Chen *et al.*, "Predictions of CMOS Compatible On-Chip Optical Interconnect," *Integration, the VLSI Journal*, Volume 40, Issue 4, pp. 434–446, July 2007.

[3] *The International Technology Roadmap for Semiconductors*, Semiconductor Industry Association, California, 2003.

[4] S. V. Averine, Y. C. Chan, and Y.L. Lam, "Geometry Optimization of Interdigitated Schottky-Barrier Metal-Semiconductor-Metal Photodiode Structures," *Solid-State Electronics*, Vol. 45, No. 3, pp. 441–446, March 2001.