A 0.8 Volt High Performance OTA Using Bulk-Driven MOSFETs for Low Power Mixed-Signal SOCs

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ABSTRACT

An ultra-low voltage rail-to-rail folded-cascode operational transconductance amplifier (OTA) based on a standard digital 0.18 µm CMOS process is described in this paper. A bulk-driven MOSFET technique is employed to facilitate a 0.8 volt power supply voltage. The gain of the OTA is increased by using auxiliary gain boosting amplifiers, which enable the OTA to achieve an open loop gain of 68 dB while consuming 94 µW, the highest gain achieved to date in bulk-driven amplifiers.

***Index Terms*— bulk driven MOSFET, fully differential OTA, gain boosting, CMFB.**

1. INTRODUCTION

The reduction in the minimum dimensions in VLSI technologies along with the trend of using small portable devices necessitates reduced power supply voltages. However, threshold voltages in future CMOS technologies may not decrease much below what is available today, making it difficult to design analog circuits with lower supply voltages.

A promising approach in low voltage analog circuits is the so-called "bulk-driven" MOSFET method [1]-[3]. In this method, the gate-to-source voltage is set to a value sufficient to form an inversion layer, and an input signal is applied to the bulk terminal. In this manner, the threshold voltage can be removed from the signal path.

One important drawback of the bulk-driven method is that the body transconductance is approximately five times smaller than the gate transconductance, resulting in a relatively low gain. This behavior is the primary reason for the low gain (around 45 dB) in previously reported bulk-driven amplifiers [3], [4]. In this paper, a 0.8 volt fully differential folded-cascode OTA is presented which employs the bulk-driven MOSFET method. Four common-source gain boosting amplifiers are used to increase the gain to 68 dB (which was 48 dB before gain boosting). This gain is the highest gain achieved to date in bulk-driven amplifiers.

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2. THE DESIGN OF THE AMPLIFIER

The core of the proposed OTA is illustrated in Figure 1. This circuit is based on a fully differential topology with two complementary input pairs. The output branch consists of common gate amplifiers with cascode current loads to increase the gain. A common mode feedback circuit is used with four auxiliary common source amplifiers.

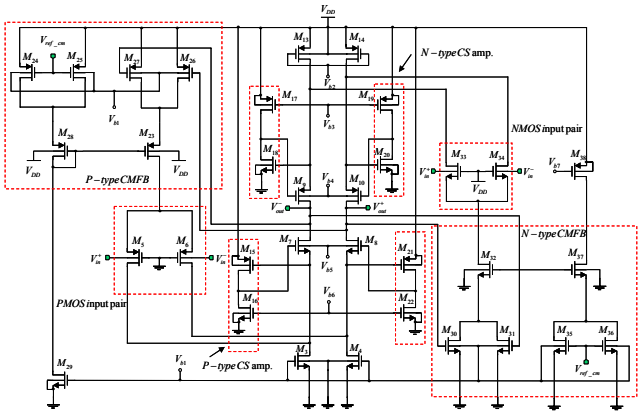

Figure 1. The amplifier core of an OTA

In the design of the proposed OTA, rail-to-rail operation is achieved using a pair of PMOS (M_5 and M_6) and NMOS (M_{33} and M_{34}) transistors at the input stage. This strategy supports rail-to-rail (0 volt to 0.8 volt) operation of the amplifier, thus the input common mode range (ICMR) is extended to the largest possible range.

The output branch of the OTA consists of two symmetric common gate (CG) amplifiers (M_7 and M_8). Both amplifiers have cascode current loads (M_9 and M_{13} and M_{10} and M_{14}) to increase the gain. The bias current is provided to M_7 and M_8 by the current sources M_3 and M_4, respectively, which also operate as current loads for the P-type input pair (M_5 and M_6). Note that a complementary structure is also implemented for the N-type input pair. M_{13} and M_{14} act as current sources for the N-type input pair.

Auxiliary common source (CS) amplifiers (M_{15}, M_{16}, M_{21}, and M_{22}, and M_{17}, M_{18}, M_{19}, and M_{20} shown in Figure 1) provide a target open loop gain of at least 60 dB. In this way, stacking multiple transistors in the output branch is avoided, providing more overdrive voltage to maintain the transistors in the saturation region, while simultaneously increasing the voltage gain. The output of the CS amplifier is connected to the gate of the CG amplifier so as to maintain an almost constant source voltage.

This source node is fed back as the input voltage to the CS amplifier. In this way, the local feedback action reduces the variations in the bias current when the source voltage of the CG amplifier changes, thereby increasing the output resistance.

A continuous CMFB circuit (M_{24}, M_{25}, M_{26}, and M_{27} and M_{30}, M_{31}, M_{35}, and M_{36} shown in Figure 1) is used to stabilize the output common mode level. In this circuit, transistors M_{24}, M_{25}, M_{26}, and M_{27} operate in the linear region, acting as voltage controlled resistors. When the DC operating point at the output differs from the target common mode voltage, a change in the tail current of the input pair occurs, resulting in an increment or decrement in the bias currents. This effect restores the DC operating point to the desired voltage level.

In order to ensure that the transistors operate at the correct bias points, fixed bias voltages are applied either to the gate or body of the transistors. Due to limited voltage headroom, simple current mirrors are used to generate the bias voltages (V_{b1}-V_{b7}), which operate with a reference current of 1 μA. A low sensitivity, supply voltage independent reference current circuit (not shown in the figure) is also incorporated in the design, which generates a stable 1 μA reference current for the bias circuit.

3. CIRCUIT LAYOUT

The layout of the OTA including the amplifier core, bias circuit, and the current generator is illustrated in Figure 2. A 0.18 μm CMOS twin-well TSMC process is used. Because both the PMOS and NMOS transistors are body biased, a twin-well technology is required to use the bulk-driven technique. Interdigitization and common-centroid methods have been applied to the layout so as to decrease mismatches among the transistors.

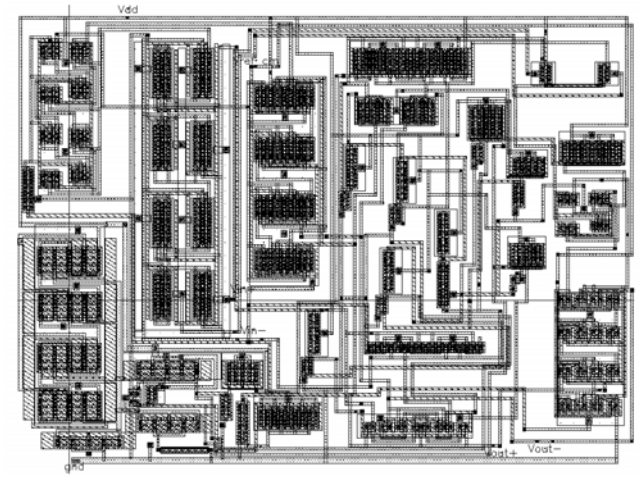

Figure 2. Physical layout of the OTA

4. OTA PERFORMANCE

The post-layout simulation results of the 0.8 volt OTA are listed in Table 1. The data listed in Table 1 shows that the OTA achieves both rail-to-rail ICMR and output swing. The OTA has an open-loop DC gain of 68 dB, a phase margin of 80°, and a unity-gain bandwidth of 93.3 MHz (see Figure 3), under a no load condition.

Table 1. Simulated performance of post-layout OTA circuit

Performance merit	Simulated value
V_{DD}	0.8 volts
V_{SS}	0 volts
DC gain	68 dB
Unity gain frequency	93.3 MHz
Phase margin	80°
Input Common Mode Range	0 V ÷ 0.8 V
Output voltage swing	≈700 mV
Power consumption	94 μW

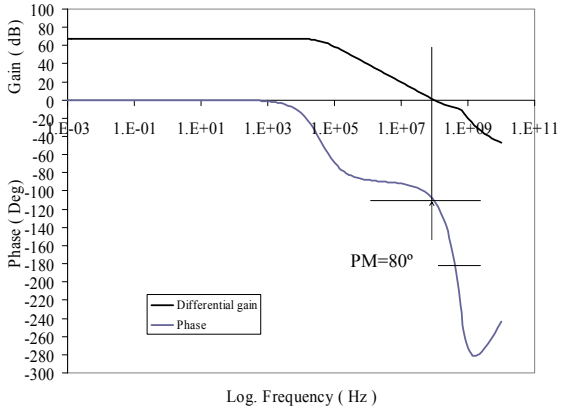

Figure 3. Open loop differential gain and phase vs. log frequency

5. CONCLUSIONS

The design of an ultra-low voltage, high performance folded-cascode OTA circuit in a standard digital CMOS process is reported in this paper. To accommodate a low power supply voltage (0.8 volt), the bulk-driven MOSFET approach is used. The low gain disadvantage of the bulk-driven technique is circumvented by employing gain boosting amplifiers, permitting the achievement of a gain of 68 dB.

6. REFERENCES

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