On-Chip Power Noise Reduction Techniques in High Performance SoC-Based Integrated Circuits

Mikhail Popovich, Eby G. Friedman
Department of Electrical and Computer Engineering
University of Rochester
Rochester, New York 14627
[nhlover, friedman]@ece.rochester.edu

Radu Secareanu, Olin L. Hartin
Freescale Semiconductor
MMSTL
Tempe, Arizona 85284
[r54143, lee.hartin]@freescale.com

Abstract— **Switching digital circuits produce current peaks which result in voltage fluctuations on the power supply lines due to the inductive behavior of on-chip and chip-to-package interconnects. A design technique is described in this paper to lower ground bounce in noise sensitive circuits. An on-chip noise-free ground is added to divert ground noise from the sensitive nodes. An on-chip decoupling capacitor tuned in resonance with the parasitic inductance of the interconnects provides an additional low impedance ground path. Ground bounce reductions of about 68% and 22% are demonstrated for a single frequency and random noise, respectively. The noise reduction is shown to depend linearly on the physical separation between the noisy and noise sensitive blocks. The dependence of ground noise on the impedance of the low noise ground is also discussed.**

The proposed technique exhibits a strong tolerance to capacitance variations. The efficiency of the noise reduction technique drops by several per cent for a $\pm 10\%$ variation in the magnitude of the decoupling capacitor. The proposed technique is shown to be effective for both single frequency and random voltage fluctuations on the ground terminal.

Index Terms— **Power distribution systems, power noise, ground bounce, decoupling capacitors, RLC impedances**

I. Introduction

Future generations of integrated circuit (IC) technologies are trending toward higher speeds and densities. The total capacitive load associated with the internal circuitry has been increasing for several generations of very large scale integration (VLSI) circuits [1-2]. As the operating frequencies increase, the average on-chip current required to charge and discharge these capacitances also increases, while the switching time decreases. As a result, a large change in the total on-chip current occurs within a brief period of time.

Due to the large slew rates of the currents flowing through the bonding wires, package pins, and on-chip interconnects, the ground and supply voltage can fluctuate (or bounce) due to the parasitic impedances associated with the package-to-chip and on-chip interconnects. These voltage fluctuations on the supply and ground rails, called ground bounce, ΔI noise, or simultaneous switching noise (SSN) [3], are further increased since a large number of the input/output (I/O) drivers and internal logic circuitry switch close in time to the clock edges. SSN generates glitches on the ground and power supply wires, decreasing the effective current drive of the circuits, producing output signal distortion, thereby reducing the noise margins of a system. As a result, the performance and functionality of the system can be severely compromised.

In the past, research on SSN has concentrated on transient power noise caused by current flowing through the inductive bonding wires at the I/O buffers. However, SSN originating from the internal circuitry has become an important issue in the design of very deep submicrometer (VDSM) high performance ICs, such as systems-on-chip (SoC), mixed-signal circuits, and microprocessors. This increased importance is due to fast clock rates, large on-chip switching activities and currents, and increased on-chip inductance, all of which are increasingly common characteristics of VDSM synchronous ICs.

Most of the work in this area falls into one of two categories: the first category includes analytic models that predict the behavior of the SSN, while the second category describes techniques to reduce ground bounce. A number of techniques have been proposed to reduce SSN. In [4], a voltage controlled output buffer is described to control the slew rate. Ground bounce reduction is achieved by lowering the inductance in the power and ground (P/G) paths by utilizing substrate conduction. An algorithm based on integer linear programming to skew the switching of the drivers to minimize ground bounce is presented in [5]. An architectural approach for reducing inductive noise caused by clock gating through gradual activation/deactivation units has been introduced in [6]. In [7], a routing method is described to distribute the ground bounce among the pads under a constraint of constant routing area. The total P/G noise of the system, however, is not reduced. Decoupling capacitors are often added to maintain the voltage on the P/G rails within specification, providing charge for the switching transients [8,9]. Recently, the reduction of ground bounce by bounce pre-generator circuits [10] and supply current shaping and clock frequency modulation [11] has been reported.

Signal integrity is a crucial issue in modern high perfor-

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mance, high complexity circuits and is becoming increasingly important as the minimum feature size of devices scales to 90 nm and below. A major component of the circuit noise is P/G noise. Design techniques to reduce P/G noise in mixed-signal power distribution systems is the primary focus of this paper. The efficiency of the proposed method is also analyzed based on physical parameters of the system. The paper is organized as follows. Ground noise reduction through the addition of a noise-free on-chip ground is described in Section II. The efficiency of the proposed technique as a function of the physical parameters of the system is investigated in Section III. Some specific conclusions are summarized in Section IV.

II. Ground Noise Reduction through an Additional Low Noise On-Chip Ground

An equivalent circuit of an SoC-based power delivery system is shown in Fig. 1. Traditionally, noisy digital circuits share the power supply voltage and the ground with noise sensitive analog circuits. If a number of digital blocks switch simultaneously, the current I_D drawn from the power distribution network can be significant. This large current passes through the parasitic resistance R^p_{Gnd} and inductance L^p_{Gnd} of the package, producing voltage fluctuations on the ground terminal (point A). As a result, ground bounce (or voltage fluctuations) appears at the ground terminal of the noise sensitive circuits.

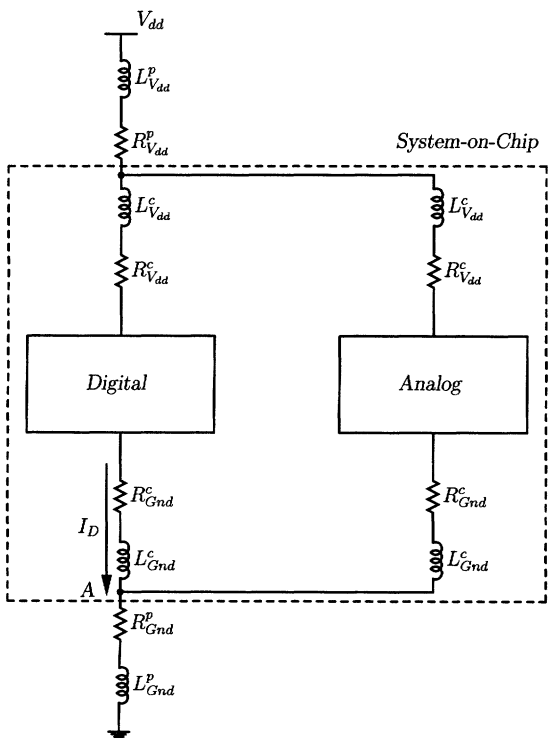

Fig. 1. An equivalent circuit for analyzing ground bounce in an SoC. The power distribution network is modeled as a series resistance and inductance. Superscripts p and c denote the parasitic resistance and inductance of the package and on-chip power delivery systems, respectively. The subscript V_{dd} denotes the power supply voltage and the superscript Gnd denotes ground.

To reduce voltage fluctuations at the ground terminal of the noise sensitive blocks, an on-chip low noise ground is added as shown in Fig. 2. This approach is based on a voltage divider formed by the impedance between the noisy ground terminal and the quiet ground terminal and the impedance of the path from the quiet ground terminal to the off-chip ground. The value of the capacitor is chosen to cancel the parasitic inductance of the additional low noise ground, *i.e.*, the ESL of the capacitor L_d and the on-chip and package parasitic inductances of the dedicated low noise ground L^3_c and L^3_p, respectively. Alternatively, the capacitor is tuned in resonance with the parasitic inductances at a frequency that produces the greatest noise reduction efficiency. The impedance of the additional ground path, therefore, becomes purely resistive and reaches a minimum.

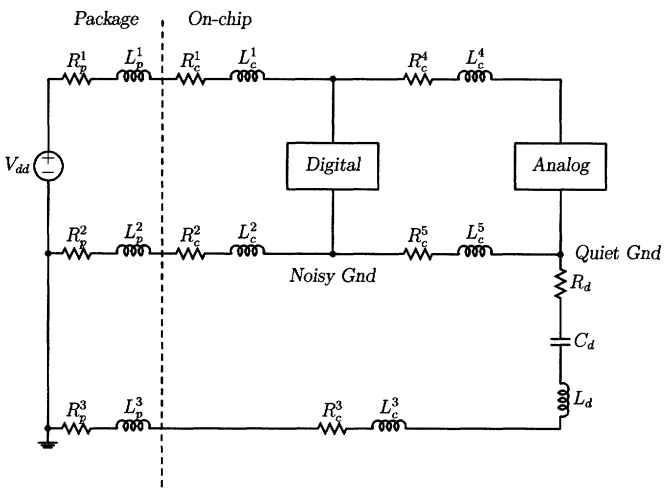

Fig. 2. Proposed ground bounce reduction technique. An effective series resistance (ESR) and effective series inductance (ESL) of a decoupling capacitor are modeled by R_d and L_d, respectively. R^5_c and L^5_c represent the physical separation between the noisy and noise sensitive blocks. The impedance of an on-chip additional ground is modeled by R^3_c and L^3_c, respectively.

The same technique can be used to reduce voltage fluctuations on the power supply. Based on the nature of the power supply noise, an additional ground path or power supply path can be provided. For instance, in the case of a voltage drop below the power supply level, an on-chip path to the power supply should be added. In the case of an overshoot, an additional ground path should be provided.

III. Dependence of Efficiency of Ground Bounce Reduction on the System Parameters

To determine the efficiency of the ground bounce reduction, a simplified circuit of the proposed technique is used, as shown in Fig. 3. The ground bounce caused by simultaneously switching within the digital circuitry is modeled as a voltage source. A sinusoidal voltage source with an amplitude of 100 mV is used to determine the reduction in ground bounce at a single frequency. A triangular voltage source with an amplitude of 100 mV and 50 ps rise and 200 ps fall times is utilized to model the reduction in ground noise.

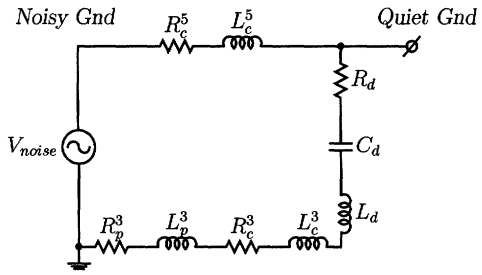

Fig. 3. Simplified circuit of the proposed technique. Ground bounce due to simultaneously switching the digital circuits is modeled by a voltage source. The *Noisy Gnd* denotes an on-chip ground for the simultaneously switching digital circuits. The *Quiet Gnd* denotes a noise-free ground for the noise sensitive circuits.

The dependence of the noise reduction on physical separation between the noisy and noise sensitive circuits is presented in subsection III-A. The sensitivity of the proposed technique to frequency and capacitance variations is discussed in subsection III-B. The dependence of ground noise on the impedance of an additional on-chip ground path is analyzed in subsection III-C.

A. Physical Separation between Noisy and Noise Sensitive Circuits

To determine the dependence of the noise reduction technique on the physical separation between the noise source and noise receiver, the impedance of the ground path between the noisy and quiet terminals is modeled as a series RL. Given the parasitic resistance and inductance per unit length, the RL impedance is varied for different unit lengths. The peak voltage at the quiet ground is evaluated using SPICE where the distance between the digital and analog circuits is varied from one to ten unit lengths. The reduction in ground bounce as seen from the ground terminal of the noise sensitive circuit for sinusoidal and triangular noise sources is listed in Table I.

TABLE I

GROUND BOUNCE REDUCTION AS A FUNCTION OF SEPARATION BETWEEN THE NOISY AND NOISE SENSITIVE CIRCUITS

R_c^5	L_c^5	V_{quiet} (mV)		Noise Reduction (%)	
(mΩ)	(fH)	Sinusoidal	Triangular	Sinusoidal	Triangular
13	7	90.81	97.11	9.2	2.9
26	14	82.99	94.68	17.0	5.3
39	21	76.30	92.63	23.7	7.4
52	28	70.54	90.55	29.5	9.5
65	35	65.53	89.36	34.5	10.6
78	42	61.16	88.06	38.8	11.9
91	49	57.33	86.93	42.7	13.1
104	56	53.94	85.93	46.1	14.1
117	63	50.91	85.05	49.1	15.0
130	70	48.23	84.28	51.8	15.7

$V_{noise} = 100\,\text{mV}$, $f = 1\,\text{GHz}$, $R_p^3 = 10\,\text{m}\Omega$
$L_p^3 = 100\,\text{pH}$, $R_c^3 = 100\,\text{m}\Omega$, $L_c^3 = 100\,\text{fH}$, $R_d = 10\,\text{m}\Omega$
$L_d = 10\,\text{fH}$, $C_d^{Sin} = 253\,\text{pF}$, $C_d^{Triang} = 63\,\text{pF}$

Note that the reduction in ground noise increases linearly as the physical separation between the noisy and noise sensitive circuits becomes greater. A reduction in ground bounce of about 52% for a single frequency noise source and about 16% for a random noise source is achieved for the ground line (of ten unit lengths) between the digital and analog blocks. Enhanced results can be achieved if the impedance of the additional ground is much smaller than the impedance of the interconnect between the noisy and noise sensitive modules. From a circuits perspective, the digital and analog circuits should be placed far from each other and the additional low noise ground should be composed of many parallel lines. Moreover, the additional ground should be placed close to the multiple ground pins.

Note that since the proposed technique utilizes a capacitor tuned in resonance with the parasitic inductance of an additional ground path, this approach is frequency dependent and produces the best results for a single frequency noise source. In the case of a random noise source, the frequency harmonic with the highest magnitude will be significantly lower in magnitude, thereby achieving the greatest reduction in noise. For example, based on a discrete Fourier transform (DFT), the second harmonic is selected in the case of a triangular noise source.

B. Frequency and Capacitance Variations

To determine the sensitivity of the ground bounce reduction technique on frequency and capacitance variations, the frequency is varied by ±50% from the resonant frequency and the capacitor is varied by ±10% from the target value. The range of capacitance variation is chosen based on typical process variations for a CMOS technology. The efficiency of the reduction in ground bounce for a sinusoidal noise source versus frequency and capacitance variations is illustrated in Figs. 4 and 5, respectively.

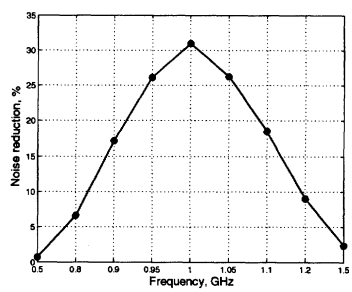

Fig. 4. Ground bounce reduction as a function of noise frequency. The ground noise is modeled as a sinusoidal voltage source.

Note that the noise reduction drops linearly as the noise frequency varies from the target resonant frequency. The noise reduction is slightly greater for higher frequencies. This phenomenon is due to an uncompensated parasitic inductance of the ground connecting the digital circuits to the analog circuits. As a result, at higher frequencies, the impedance of the ground path of a power delivery network increases, enhancing the noise reduction efficiency. In general, the proposed technique results in greater noise reduction efficiency at higher frequencies. As illustrated in Fig. 5, the reduction in ground bounce is almost insensitive to capacitance variations.

The efficiency of the proposed technique drops by about 4% as the capacitance is varied by $\pm 10\%$.

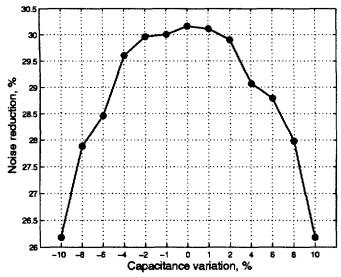

Fig. 5. The efficiency of the reduction in ground bounce as a function of capacitance variations. The ground bounce is modeled as a sinusoidal voltage source.

C. Impedance of an Additional Ground Path

As described in Section II, the proposed scheme for reducing ground bounce utilizes a voltage divider formed by the ground of an on-chip power distribution system and an additional low noise ground. To increase the efficiency of the proposed technique, the voltage transfer function of the voltage divider should be lowered, permitting a greater portion of the noise voltage to be diverted from the die through the additional ground. As demonstrated in subsection III-A, placing noisy and noise sensitive blocks distant from each other lowers the ground bounce at the ground terminal of the analog circuits. The ground noise can also be reduced by lowering the impedance of the low noise ground. The parasitic inductance of the additional ground is canceled by the capacitor tuned in resonance to the specific frequency. The impedance of the additional ground is therefore purely resistive at the resonant frequency. The noise reduction efficiency for different values of the parasitic resistance of the low noise ground is listed in Table II.

TABLE II

GROUND BOUNCE REDUCTION FOR DIFFERENT VALUES OF PARASITIC RESISTANCE OF THE ON-CHIP LOW NOISE GROUND

R_c^3	V_{quiet} (mV)		Noise Reduction (%)	
(mΩ)	Sinusoidal	Triangular	Sinusoidal	Triangular
100	60.54	87.88	39.5	12.1
80	56.52	86.57	43.5	13.4
60	51.67	84.98	48.3	15.0
40	45.79	83.03	54.2	17.0
20	38.59	80.60	61.4	19.4
10	34.37	79.15	65.6	20.9
5	32.08	78.37	67.9	21.6

$V_{noise} = 100\,\text{mV}$, $f = 1\,\text{GHz}$, $R_p^3 = 10\,\text{m}\Omega$, $L_p^3 = 100\,\text{pH}$
$L_c^3 = 100\,\text{fH}$, $R_c^5 = 80\,\text{m}\Omega$, $L_c^5 = 40\,\text{fH}$, $R_d = 10\,\text{m}\Omega$
$L_d = 10\,\text{fH}$, $C_d^{Sin} = 253\,\text{pF}$, $C_d^{Triang} = 63\,\text{pF}$

Note from Table II that by reducing the parasitic resistance of an on-chip low noise ground, the ground bounce can be significantly lowered. Noise reductions of about 68% and 22% are demonstrated for sinusoidal and triangular noise sources, respectively. The results listed in Table II are determined for an average resistance and inductance of the on-chip power distribution ground of five unit lengths (see Table I). Thus, the ground bounce can be further reduced if the analog and digital circuits are placed at a greater distance from each other. Even better results can be achieved if the parasitic resistance of the package pins R_p^3 and decoupling capacitor R_d are lowered. From a circuits perspective, the on-chip low noise ground should be composed of many narrow lines connected in parallel to lower the parasitic resistance and inductance. A number of package pins should be dedicated to the noise-free ground to lower the package resistance. Finally, a decoupling capacitor with a low parasitic resistance (ESR) should be used.

IV. CONCLUSIONS

A design technique to reduce ground bounce in SoC and mixed-signal ICs is presented in this paper. An additional on-chip ground is provided to divert ground noise from the sensitive analog circuits. The proposed technique utilizes a decoupling capacitor tuned in resonance with the parasitic inductance of an additional low noise ground, making the technique frequency dependent. The reduction in ground bounce is, however, almost independent of capacitance variations. Noise reductions of 68% and 22% are demonstrated for a single frequency and random ground noise, respectively. The noise reduction efficiency can be further enhanced by simultaneously lowering the impedance of the additional noise-free ground and increasing the impedance of the ground path between the digital (noisy) and analog (noise sensitive) circuits.

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